IBM®

Customer Engineering
Manual of Instruction

700

Series Data Processing Systems
Component Circuits

Book A. General Theory
Book B. 701-704-709 Components
Book C. 702-705 Components
Book D. Auxiliary Equipment
Book E. Appendix

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FOREWORD

This manual is written at a level that assumes the reader has a background of basic electronics. The text material is not written from a standpoint of design but rather from a standpoint of the circuit understanding that is necessary for servicing. Where design information is deemed necessary, it is included. For those who feel a need for review, the Appendix (Book E) contains formulas and procedures necessary for simple computations of voltage levels and currents flowing in the circuits. Book E also contains some design procedures for those who want more material on this subject.

Data-processing machines, such as the 700 series machines, contain many thousands of individual electronic components (resistors, capacitors, inductors, electron tubes, crystal diodes, and so on). Together, they form the "nerve system" of the calculator. Because of the complexity of showing the miles of circuits that make up these machines, the logic block method of circuit layout is used. Logic blocks simplify circuit tracing and trouble shooting. Each logic block represents an individual circuit. Each circuit has a specific function in the area where it is used. With the logic block method, circuits are easily identified and the location of each component is easily found. The following pages contain the logic blocks of component circuits, the circuit schematics, their purpose, how the circuits function, the inputs, and the resultant nominal outputs of these circuits. Given voltage levels and wave forms are suggested values only, as loading conditions affect individual circuits in the machine.

This manual is divided into five main books.

Book A contains information that is pertinent to all component circuits and should be studied before investigating any individual circuit. The location procedure is described early in the manual so that it may be reviewed with each circuit until it is fully understood.

Book A also describes circuits that are popularly called basic or standard circuits. Because these circuits are most commonly used, a thorough study of them helps the customer engineer in understanding the remaining circuits. For this reason, they are explained in greater detail than circuits that are merely modifications of the standard circuits.

Book B contains information about the pluggable unit panels, the systems block diagrams and the MF neon locations peculiar to the 701, 704, and 709 machines. It also has a complete listing of component circuits assigned to the 701, 704, and 709 systems except power supply and transistor components. Every circuit listed in this book is cross-referred to the "4" pages of machine systems, e.g., inverter I (section 2.01.01, Book B) is the same as 4.01.01 and key trigger T_K (section 2.02.05, Book B) is the same as 4.02.05. Wherever advisable, the reader is referred to Book A for a more detailed description of the circuit.

Book C contains information about the 702 and 705 systems' pluggable unit panels, edge connectors, circuit locations and panel designations.

Also, this book contains a complete listing of component circuits except power supply components. The basic circuits are duplicated here, with the reader referred to Book A for a complete description. This duplication is made so that circuits listed in this section can have cross reference to the "C" pages of machine systems. ("C" pages contain circuit schematic and standard pluggable unit wiring procedure.) An example is the inverter I (section 2.01.01, Book C) which is the same as C.01.01 and key trigger T_K (section 2.02.04, Book C) which is the same as C.02.04. Circuits that appear in isolated areas such as memory or drum alone are briefly discussed here but full discussion of their usage is found in the respective machine manuals.

Book D contains information and the component circuits for the 700 series auxiliary equipment. The machines described in this book are the 720 Printer, the 760 Control and Record Storage Unit, the 774 Tape Data Selector, and the 777 Tape Record Coordinator.

The Appendix, Book E, contains detailed component specifications, basic electrical formulas, samples of logic block layouts, and a sample of design procedure.

NOTICE

The text and illustrations included in the following pages have been prepared for teaching purposes and as an aid for learning the component circuits of the 700 series machines. All material was prepared from information relative to production at a given level. Engineering changes may alter exact timings, logic blocks or component values; therefore, the customer engineer is advised not to use this information alone as a reference manual or servicing aid.

ABBREVIATIONS

The following abbreviations are used throughout this manual. Component circuits block designations (such as I for inverter) are not included in this list.

A	all (cycles)	inst	instruction
a	ampere	I/O	input/output
AC	alternating current	K	kilo (10^3) (usually refers to ohms)
adr	address	Kc	kilocycles
amp	amplifier	L	inductor
bksp	backspace	lt	left
C	capacitor	meg	megohms (10^6)
C	cycle	m	milli (10^{-3})
CB	circuit breaker	MF	main frame
CF	core frame	MQ	multiplier quotient
CP	card punch	Ω	ohm
CPU	central processing unit	op	operation
CT	cycle time	Pr	printer
CS	core storage	Q	quotient
ctr	counter	R	resistance
DC	direct current	rewd	rewind
DF	drum frame	RI	read-in
e	voltage	rt	right
E	execute (time)	Rd	read
EC	edge connector	S (sec)	seconds
EOF	end of file	sw	switch
EOR	end of record	stg	storage
f	farad	tgr	trigger
h	henry	u	micro (10^{-6})
I	current	uu	micro-micro (10^{-12})
I	instruction	v, V	volt
intlk	interlock	Wr	write

Component Circuits

Book A. General Theory

CONTENTS

CONTENTS (continued)

1.00.00 GENERAL INFORMATION

1.01.00 DEFINITION OF TERMS

Certain terms in the circuit descriptions must be clarified or defined, e.g., "standard cathode follower" or "standard inverter." All circuits are standard but the basic ones (such as AND, OR, I, K, T, and SS) are the most commonly used. Others may be merely modifications of these basic circuits or entirely different circuits; they are popularly called "special circuits," used in a very few applications.

The term "tube" may refer to one or both sections of a dual tube, but the term is not used unless the reference is clear in the text. The terms "left tube" and "right tube" refer to the placement of the components on the schematic. They are not to be confused with the terms "front" and "back" that are used to denote the physical placement of the tube socket on the pluggable unit.

The voltage levels of the pulses and input/output lines fall into two general classifications: signal level and plate level (section 1.05.00). The terms "rise" and "fall" refer to the transition of a pulse. Rise or fall time is usually the time required for a pulse transition to reach 80 percent of its final value (from ten percent to 90 percent). Rise and fall time of a pulse is expressed in volts per microsecond (millionth of a second). Pulse width is measured at a point halfway between voltage levels.

Electron flow (- to +) is assumed in all circuit descriptions. Increasing the absolute potential gradient across a capacitor is called charging the capacitor. When this gradient decreases, the capacitor is discharging. During some types of transitions, the polarity of the voltage across the capacitor reverses; therefore, the terms "charge" and "discharge" as defined above may be confusing. In these cases assume that one terminal of the capacitor is connected to a steady voltage which is always more negative than the opposite terminal. If this assumption is made, the above definitions of charge and discharge still apply. For example, if the voltage at one terminal of a capacitor changes from -30 volts to +10 volts and the opposite terminal is grounded, assume then that the capacitor has been charged. It discharges when the voltage returns to -30 volts.

1.02.00 PLUGGABLE UNIT

The pluggable unit acts as the carrier for most of the component circuitry (tubes, resistors, capacitors, and so on) in the 700 series systems (Figures A1a and A1b). The unit has eight tube sockets, although it need not have the full complement of eight tubes. Filament terminals of all tube sockets are wired.

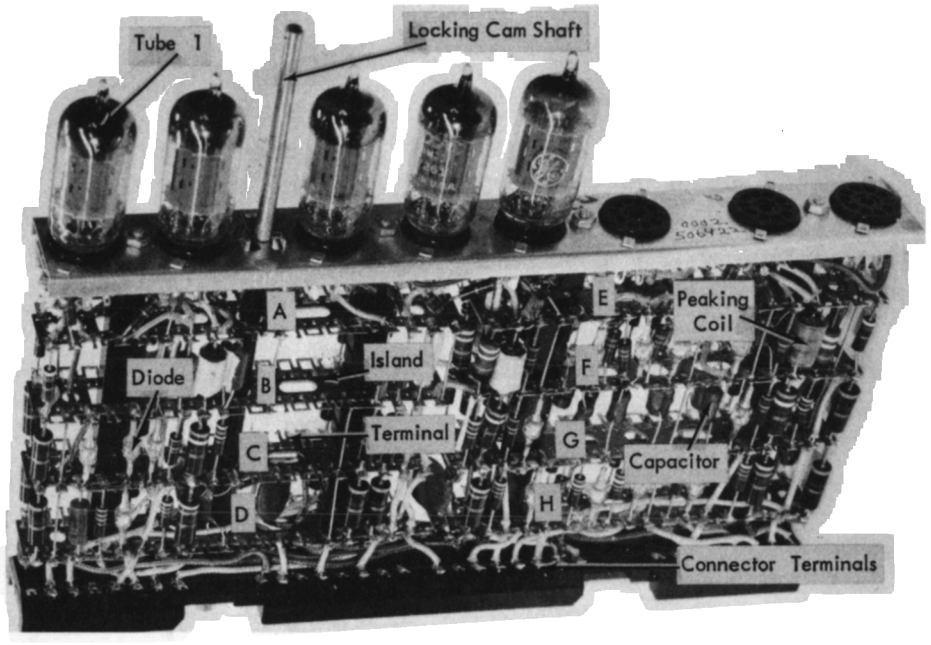


FIGURE A1a. PLUGGABLE UNIT

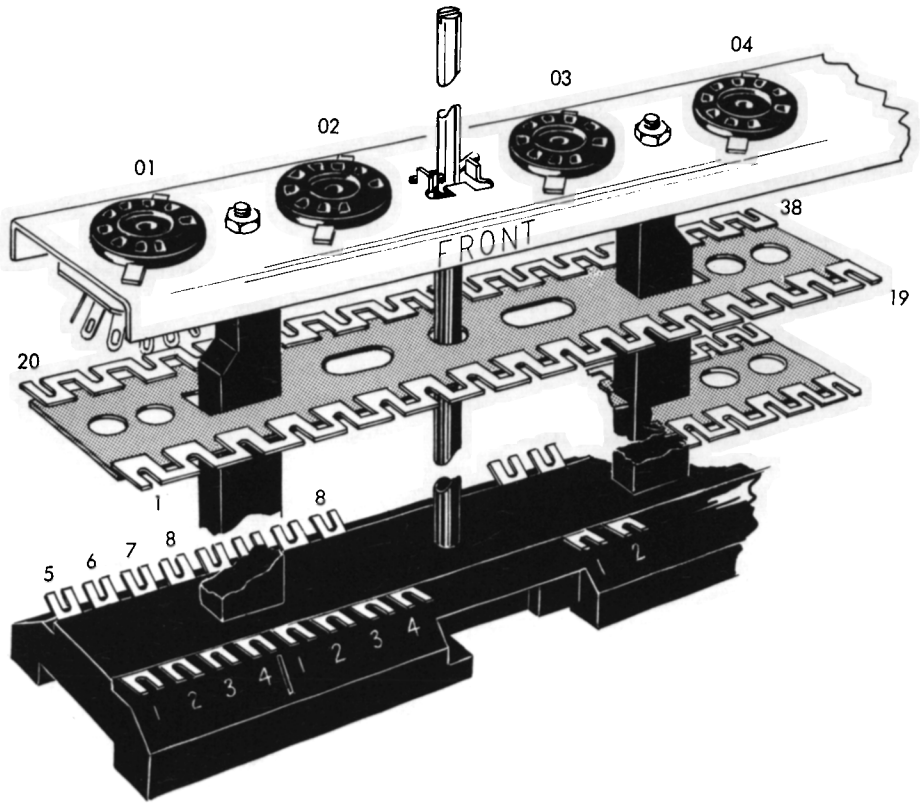


FIGURE A1b. PLUGGABLE UNIT

Mounted within the pluggable unit are eight terminal strips each consisting of 38 solder terminals or lugs. The terminals are numbered 1-19 on the front of the unit and 20-38 on the back. The terminals are initially shorted together and cut open to make the terminals individual. This procedure eliminates the need for jumpers. The terminal strips are called islands and are located by their corresponding positions in the unit (A through H). The circuit components are mounted between these islands.

Directly beneath each tube position, at the base of the unit, is a group of connector terminals labeled 1 through 8. These terminals are internally connected to the male knife connectors beneath the base. The unit connects to a female receptacle that has solder lugs extending out on the wiring side of the panel (panel pins). There are eight panel pins for each tube position. The panel pins are used for the entry of service wiring (voltage supplies) and signal wiring to the unit.

The locking-cam shaft extends through the unit and is used to seat the unit into its female connector. The unit is aligned to the connector; rotating the shaft with a pluggable unit wrench cams the unit downward to lock it in place. The contacts on the female connector are aligned vertically in such a way that the negative voltages are applied before the positive voltages when the unit is installed. The reverse is true when the unit is removed. However, it is wise to drop DC voltages before removing or installing pluggable units.

Each machine systems index section has a pluggable unit location chart for each panel on the machine. This chart includes unit part numbers. Standardization of units is retained wherever possible. Thus, the same units may have components used on one machine and unused on another.

1.03.00 PLUGGABLE UNIT LOCATION

All panels that contain pluggable units use the coordinate reference system for locating specific points on the panel. The vertical axis is labeled with upper case letters A-Z, omitting I and O. The horizontal axis is labeled with numbers 01-40, the number of columns depending upon the specific unit. Thus, the intersection of a horizontal and a vertical notation locates a specific section of the panel. Location is given to any pluggable unit in the panel by giving the column and alphabetic location of the first tube of the unit. With eight tube positions per unit, the first tube locations can be only A, J, or S. Because the islands are lettered and the island terminals are numbered, any component on a unit can be located. Panel pins receive their location from the tube socket that is in line with the pin group.

1.04.00 PULSE SKETCHES AND WAVE FORMS

Sketches and wave form drawings are included to aid circuit explanation. For drawing convenience, pulse sketches are shown in many cases as a square wave, although the perfect square wave (zero rise and fall time) does not exist. Actual rise and fall time is usually several tenths of a microsecond. Distortion effects of a circuit on an incoming pulse are occasionally overemphasized to show graphically what is causing the distortion. Also, poor input pulses are used to show pulse-shaping and level-setting characteristics of a circuit.

The same circuit can operate differently throughout the machine because of variables such as stray capacitance, output loading, and variations in component tolerances.

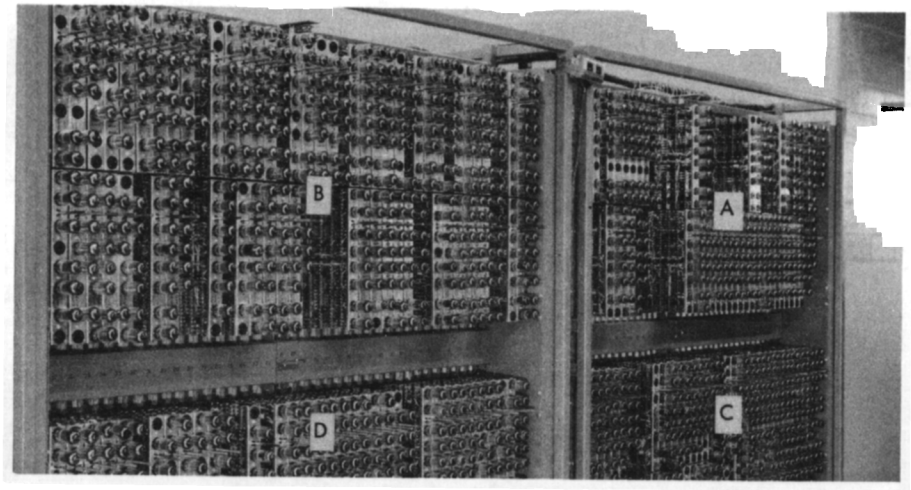


FIGURE A2. PANELS A-D

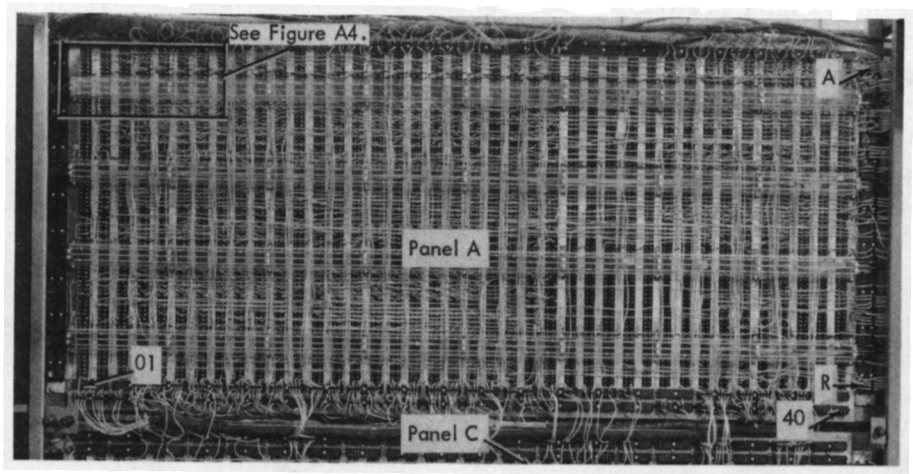


FIGURE A3. PANEL A (WIRING SIDE)

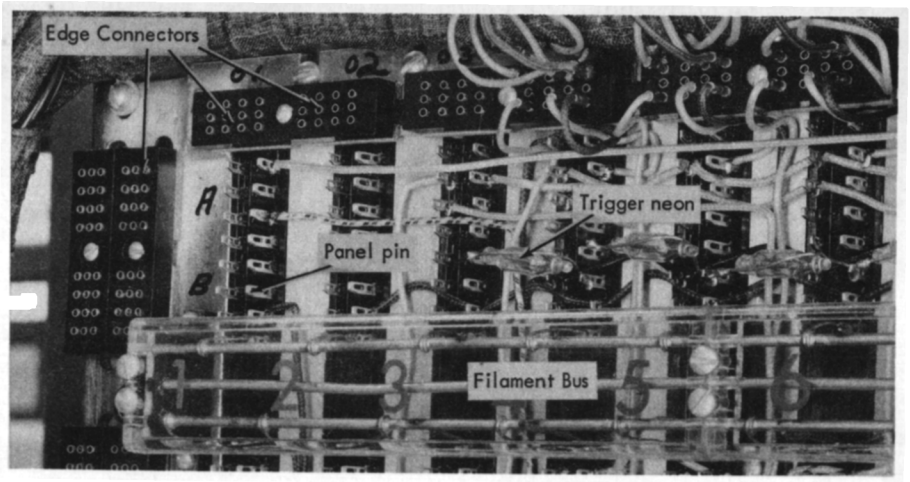


FIGURE A4. PANEL WIRING

1.05.00 INPUT/OUTPUT LEVELS

The voltage levels of pulses and information lines fall into two classifications: signal level and plate level. Signal levels are developed at divider outputs while plate levels are developed at full plate, tapped plate, or tapped divider outputs.

Signal level limits are usually +10 to -30 volts, with certain circuits requiring variations. In high-speed computer circuits, the effect of line capacitance to ground is detrimental. Therefore, the voltage swing above and below ground was chosen as a minimum satisfactory level. Circuits are controlled by the input rise from -30 to +10 volts, the fall from +10 to -30 volts (± shift inputs), or the steady up or down level. The rate of change from one voltage level to another must usually be fast (60 volts/microsecond). Some circuits have adverse effects on the voltage shift; they damp or cut down the amplitude, slow the shift time, or cause general distortion. Other circuits overcome these faults with their pulse-shaping and level-setting characteristics.

Because plate levels are about 100 volts, they are noted as plate levels in the system pages. This notation is an aid to proper sensitivity settings on the oscilloscope or voltmeter. Plate level outputs are used for economical component usage. They perform the same duty as signal levels.

1.06.00 CRYSTAL DIODES

Crystal diodes rather than vacuum tube diodes are used in the machine wherever possible. The small crystal diodes have an obvious advantage in size over their counterpart in vacuum tubes; they have the added advantage of not needing a filament or heater, thus reducing power requirements and wattage loss in heat. Because the number of diodes employed is large, these are distinct advantages. Many watts are saved by their use and thousands of unwanted BTU's of heat are avoided. The symbol used for the crystal diode is shown below with plate and cathode labeled.

Crystal diodes are divided into various classes depending on their back and forward resistance and upon their ability to pass current. Back resistance is the DC resistance exhibited by a diode when the cathode is more positive than the plate. With the cathode more positive than the plate, the diode is theoretically cut off. Forward resistance is the opposite of this, or the resistance exhibited by a diode when the plate is more positive than the cathode. Diode specifications and identification markings, as well as theory and construction, are listed in the Appendix (sections 1.01.05 and 1.02.04, Book E).

1.07.00 ELECTRON TUBES

The three most commonly used tubes in the 700 series are the 6211, 5965 and 5687. The tubes are listed in the order of their usage in the system. The 6211 is most used because it has the lowest filament current requirements and the 5687 is used only where maximum power is needed. The three tubes are 12.6v dual triodes with center tapped filaments so that either a 6.3 v or 12.6v filament supply can be used.

The filament transformers are center tapped to either ground or a minus voltage. The AC value is thereby superimposed on different DC levels. Keeping the filament supply at a certain DC level minimizes the potential difference between cathode and heater (a manufacturer's tube specification). In sensitive amplifier circuits, this procedure also is used to prevent the cathode from being positive with respect to the filament and causing current flow from filament to cathode. Detrimental noise would be introduced into the amplifier circuit. See Figure E10 for the filament wiring lay-out. Note that the panel pins are different for each voltage level; thus, a 6v pluggable unit is inoperative in a 12v pluggable unit socket, preventing damage to the filaments. The four tube groups are fed by the filament bus in such a manner as to have the filament current travel the same bus bar distance regardless of the tap-off position. Therefore, the filament supply voltage is uniform along the complete length of the bus bar.

In most tube circuits, the status of the tube is either cut off or in full conduction, and full conduction is usually only two-thirds of recommended maximum current. In other circuits, where maximum current is exceeded, the duty cycle is very short. The duty cycle is based on a time of 30 seconds. Thus, a ten percent duty cycle indicates that the tube is operating or conducting about three seconds out of every 30 seconds. The individual durations of conduction are usually in the order of fractional parts of a microsecond and the average of these durations meets the above specifications. Because of the two basic conditions (conducting or cut-off), the cut-off bias is frequently used in circuit description.

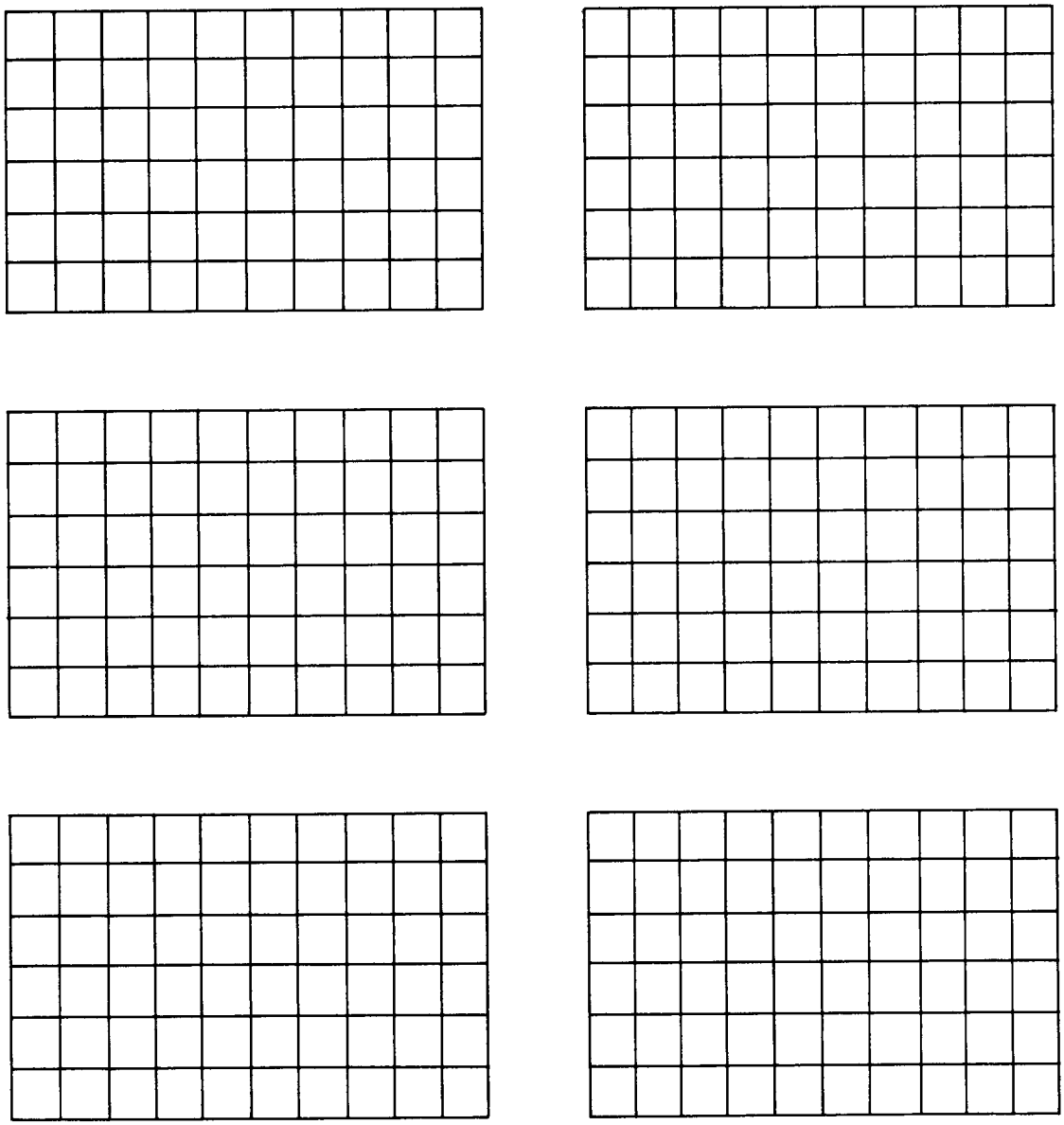
These voltages are:

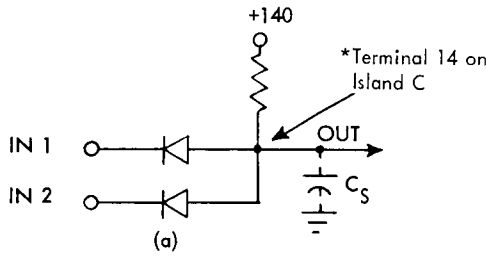
6211	-8.5 volts
5965	-6.5 volts
5687	-13 volts

Most tubes contain a 150-ohm parasitic suppression resistor in the grid circuit. Omission on the circuit schematic does not imply that this resistor is missing. In circuit design, modifications are made to insure proper operation with tubes falling in the classification 25 percent weak to 20 percent hot. Other tube specifications are listed in the Appendix.

1.08.00 CIRCUIT DELAYS

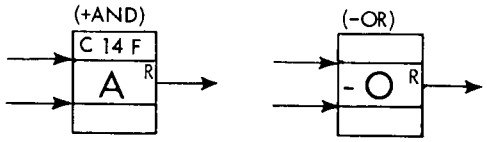
A characteristic of many tube circuits is the delays that are produced. Delay is defined as the time elapsing between the beginning of a voltage shift at a grid and the beginning of a resultant shift at the plate. Because a positive input pulse starts from a level of about -15 to -30 volts and must rise to the cut-off point for the tube before any conduction occurs, the time required to rise to this point appears as delay in the output. Conversely, any time required for an input pulse to fall from the nominal +10v level (where grid current flows) to ground (where grid current ceases) also appears as a delay in the output. Therefore, the slower the voltage transition at the grid, the more delay produced at the plate. This delay can be approximated as roughly one half of the rise or fall time of the input pulse. Delay of a circuit should not be confused with rise and fall time characteristics.

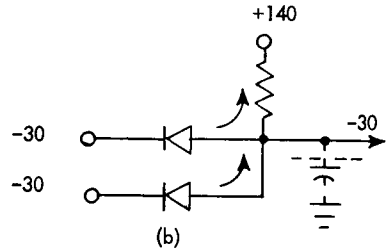




(a)

* Point B is terminal 14 on island C.





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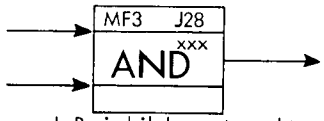
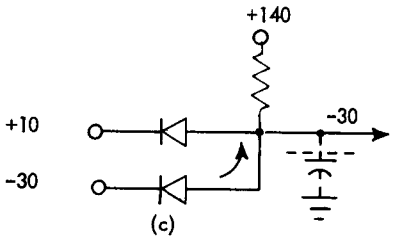


xxx Is R_L in kilohms returned to + 220 volts for a + AND circuit in the 704 system



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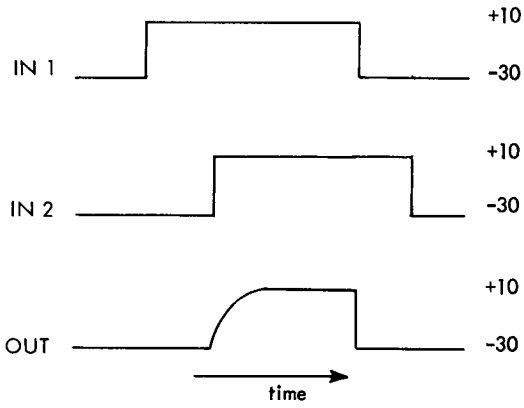

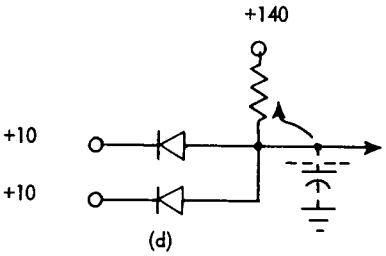

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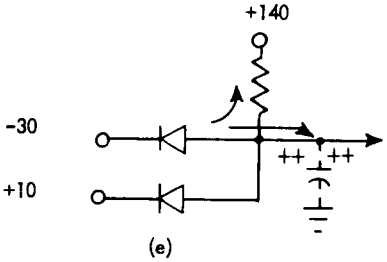

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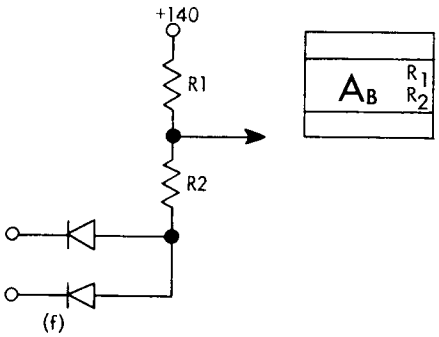


(f)

FIGURE A5. + AND (-OR) CIRCUIT

2.00.00 STANDARD CIRCUITS

The circuits in this section are popularly called standard or basic circuits because of their frequent usage in the system. The circuits are kept in one section as an aid to a thorough understanding of their operation and early application to machine logic.

2.01.00 + AND (-OR) CIRCUIT

The +AND circuit in Figure A5 is the first of four basic diode circuits used. Diode circuits form the basis for switching, decoding, adder, sampling and control circuits. They are economical because they use few components and require no vacuum tubes.

The circuit configuration for the +AND and the -OR are identical. The polarity designations are adopted in order to work with negative logic, that is, the recognition of the absence as well as presence of information. Logical operation of these two circuits is as follows:

+AND circuit requires all inputs to be plus for a plus output.

-OR circuit gives a minus output if any input is minus.

Each description holds true for either circuit because the circuits are identical. However, the logical usage is different. The +AND insures that both inputs are up before the output comes up, while the -OR gives a minus output as long as any input is down.

Figure A5f is the logic block and circuit configuration for the tapped-output AND circuit A_B. Thus, an output higher than +10 volts is obtainable. The information in the upper portion of the logic block locates the junction point of the two resistors. This point is the tap. It represents the output of the A_B.

2.01.01 Circuit Description

Figure A5a shows the junction point of the diodes and the resistor (R). This point is always used to locate diode circuits within pluggable units. Resistor (R) limits current and controls the rise time of the output. C_S represents input capacity of the circuit being driven and stray wiring capacity.

If both inputs are at -30 volts, the polarity is correct for both diodes to conduct (Figure A5b). The resultant current flow through R causes a voltage drop across it to maintain a level of about -30 volts. Because of the diode's forward resistance of 100 ohms, the voltage at the junction will be -29.04 volts. For practical purposes, the output is -30 volts and C_S is discharged.

If input 1 changes instantaneously to +10 volts, diode 1 is cut off because the cathode is more positive than the plate (Figure A5c). Diode 2, with -30 volts on its cathode, maintains conduction and the output remains unchanged. There is a small amount of current flowing through diode 2 to the +10v source, but its effect is negligible.

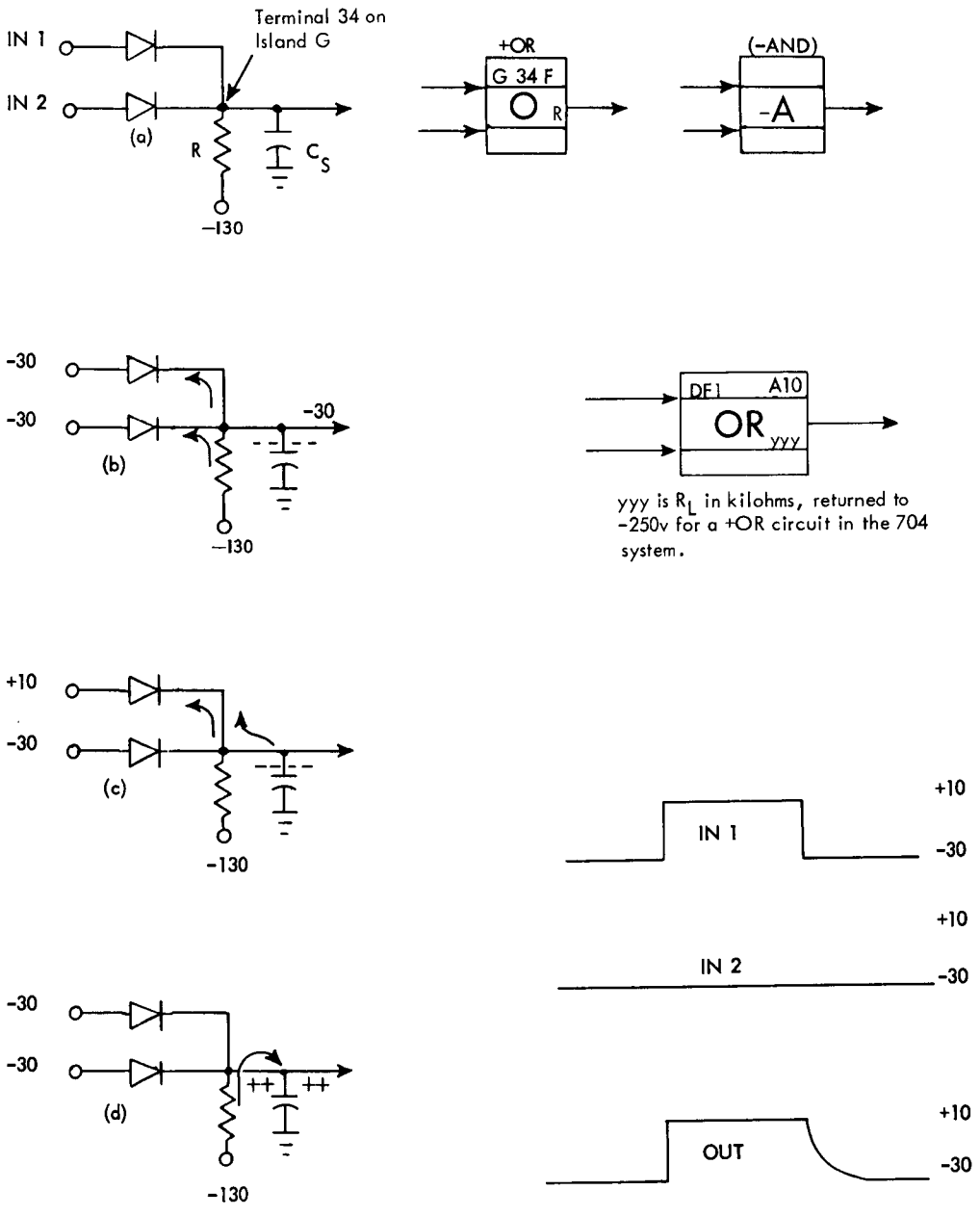


FIGURE A6. +OR (-AND) CIRCUIT

When input 2 changes to +10 volts, diode 2 is cut off because C_S momentarily is holding the output at -30 volts (Figure A5d). C_S has to charge through R to +140 volts and this delays the rise of the output level. The voltage level at the junction starts heading for +140 volts but, as soon as +10 volts is reached, the diodes go back into conduction. The output is now +10 volts and C_S is charged to +10 volts.

When input 1 falls to -30 volts, diode 1 conducts harder, discharges C_S, and diode 2 is cut off (Figure A5e). The output follows the input down to -30 volts and C_S is discharged. When input 2 falls to -30 volts, diode 2 goes back into conduction to help maintain the -30 volts output.

The action of an AND circuit may be summarized as follows: The output voltage of an AND circuit approximately equals the most negative input voltage. This statement is true regardless of the number of inputs.

2.01.02 Rise/Fall Time

The fall time of an AND circuit usually follows the input. However, the rise time depends upon the time constant of an RC circuit and is delayed. In circuit design where the value of C_S and the desired rise time is known, this formula determines the value of the limiting resistor. By transient analysis the formula for calculating rise time is:

Rise Time	$t = \begin{matrix} 0.17RC \ (701\text{-}704) \\ 0.27RC \ (702\text{-}705) \end{matrix}$
-30 volts to +10 volts	R in megohms
	C in uuf (C_S)
	t in usec

2.02.00 +OR (-AND) CIRCUIT

The circuit configurations for +OR and the -AND circuits are identical. Logical operation of these two circuits is:

+OR circuit gives a plus output, if an input is plus.

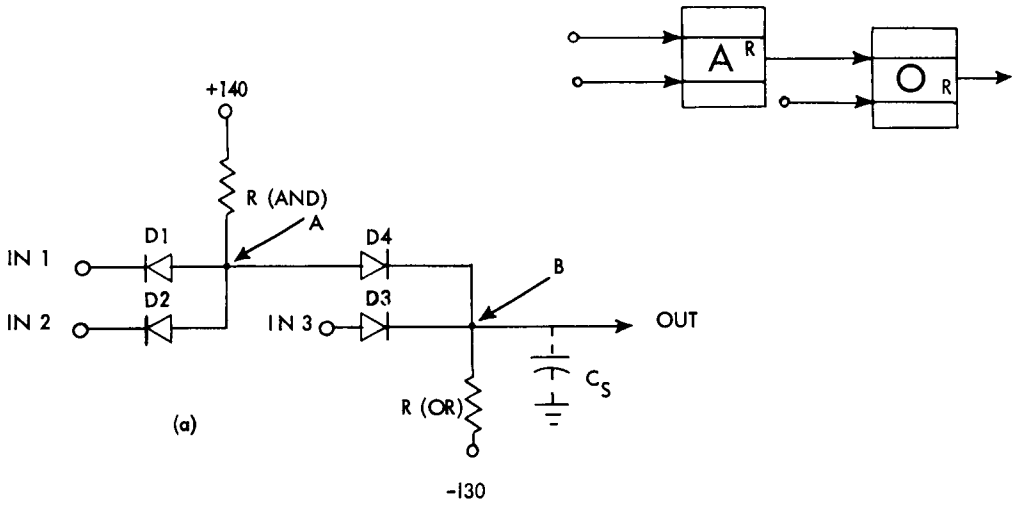
-AND circuit requires that all inputs be minus for a minus output.

Therefore, the +OR circuit differs from the +AND circuit in that it needs only one input up to bring the output up.

2.02.01 Circuit Description

If both inputs are at -30 volts, the polarity is correct for both diodes to conduct (Figure A6b). The voltage drop across the limiting resistor sets the output level at about -30 volts and C_S is discharged.

If either input rises to +10 volts, that leg conducts harder and provides a charge path for C_S (Figure A6c). The other diode cuts off and the output follows the input



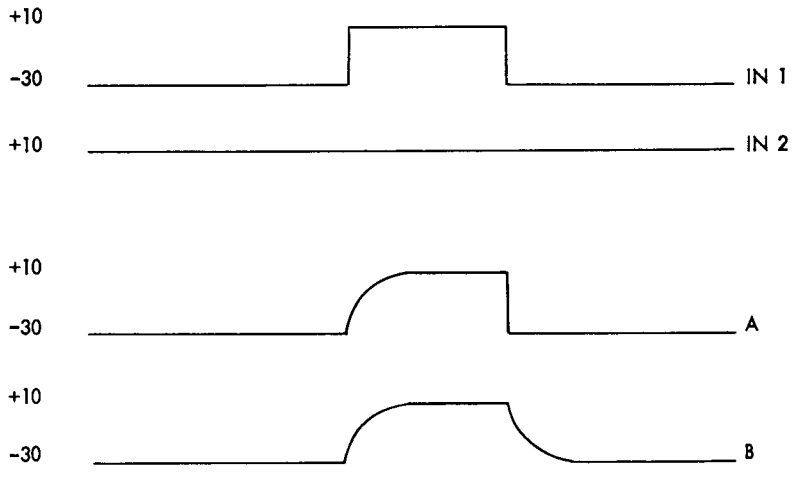


FIGURE A7. + AND DRIVING + OR

in rising to +10 volts. It is normal for only one input to an OR circuit to come up at a time.

When the input that was up at +10 volts drops to -30 volts, C_S momentarily is still charged to +10 volts, and the input diode is cut off (Figure A6d). This means that the fall time of the output is delayed because C_S maintains a plus voltage until it is discharged through R. The RC_S time constant controls the fall time of the OR output. The input diodes again conduct when the level at the junction reaches a point slightly more plus than -30 volts.

The action of an OR circuit is summarized as follows: The output voltage of an OR circuit approximately equals the most positive input voltage.

2.02.02 Rise/Fall Time

The rise time of an OR circuit usually follows the input. However, the fall time is now the affected part of the output and depends upon an RC delay. Fall time of an OR circuit is computed by the following formula:

Fall Time	$t = \begin{matrix} 0.17RC \text{ (701-704)} \\ 0.34RC \text{ (702-705)} \end{matrix}$
+10 volts to -30 volts	R in megohms C in uuf t in usec

2.03.00 +AND CIRCUIT DRIVING +OR CIRCUIT

Throughout the system, AND/OR circuits are tied together to form a network that decodes, adds or multiplies. A common situation is: AND circuits drive OR circuits. The circuit configuration is shown in Figure A7a.

2.03.01 Circuit Description

Assume the following initial status:

Inputs 1 and 3 at -30 volts
Input 2 at +10 volts

The voltage at point A is about -30 volts because D1 conducts through R (AND). Parallel current also flows up through R (OR), through D4, and through R (AND). The parallel current does not affect the voltage level at point A because D1 controls the level. Point A, being at -30 volts, sets the output level at -30 volts; C_S is discharged.

Input 1 is changed to +10 volts, D1 and D2 are momentarily cut off because C_S holds the output at -30 volts. D4 conducts; as point B starts to rise, D3 is cut off. Neglecting the effect of diode back resistances, the output rises exponentially from -30 volts toward a voltage determined by the DC voltage division between R (AND) and R (OR). This is the DC voltage that would be present at the output if diodes D1, D2, and D3 were disconnected from the circuit. (Design practice sets this level at about +20 volts). C_S charges toward this voltage and is clamped at +10 volts by the input. Note that if R (AND) was too large, the diodes would remain cut off and the output would never reach +10 volts.

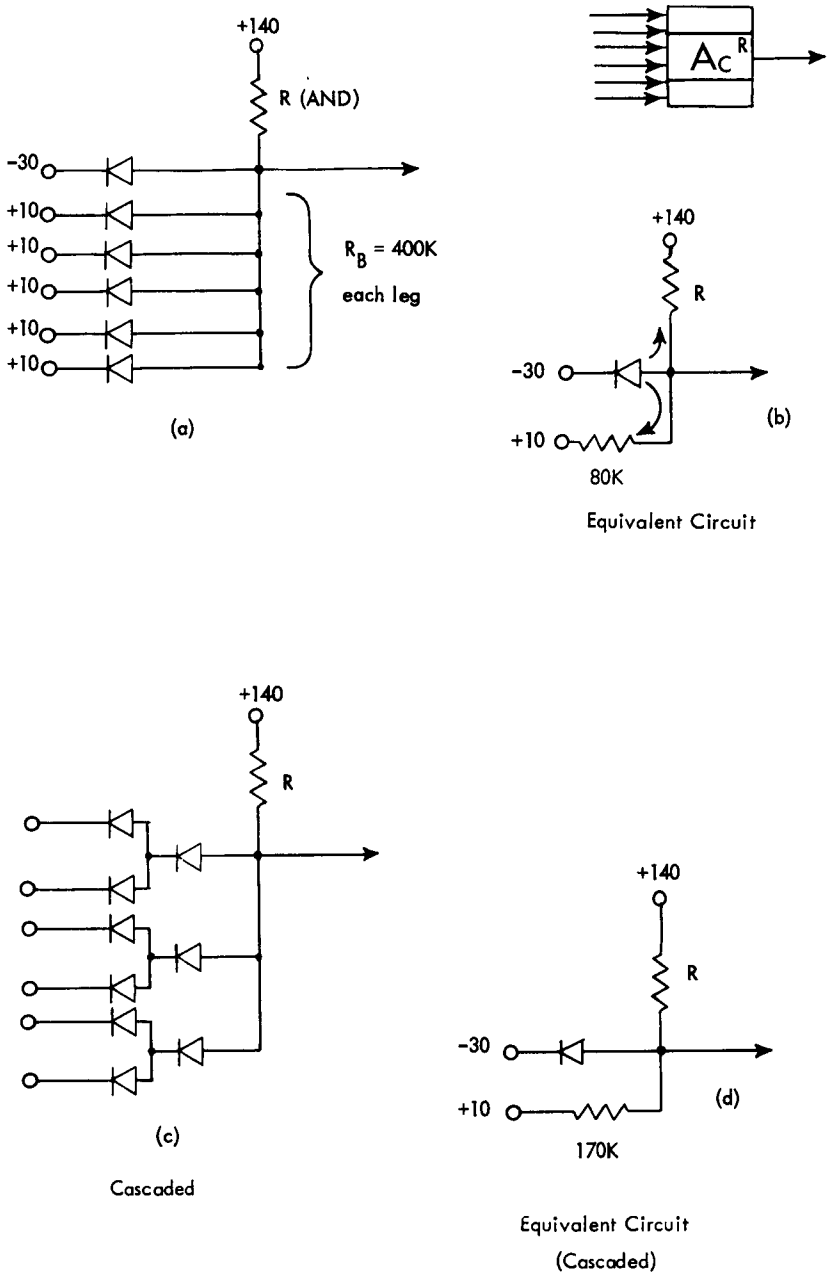


FIGURE A8. CASCADED +AND CIRCUIT

When either input 1 or 2 falls to -30 volts, the respective diode conducting causes point A to fall immediately to -30 volts. D4 is cut off because point B cannot change until C_S discharges. Normal OR circuit fall-time delay takes place and the output falls exponentially to -30 volts.

2.03.02 Rise/Fall Time

It has been shown that the output of a +AND driving a +OR combines the rise/fall time delays of both circuits. However, the rise time formula listed in section 2.01.00 does not apply here. The formula is based on the percentage of the total circuit voltage the output has to swing. For example, the rise time for a +AND circuit is given as t = 0.27RC. The 0.27RC comes from universal time constant curve (Figure 89). The voltage limits in the +AND are +140 volts and -30 volts for a total of 170 volts. The output swing is 40 volts. Thus the percent of output switch is 40/170 or 23.5 percent. This percent of transition intersects the curve at 0.27RC (time constant) and hence, the rise time formula. In the case of the AND/OR, the total equivalent voltage that the output sees has to be computed by Thevenin's Theorem (section 1.01.01, Book E). By computing the fraction $40/E_{eq}$ + 30 volts) and by using the curve in Figure E2, the number of time constants (t/T) corresponding to this fraction can be found. With this value use the following formula to compute the rise time of the AND/OR combination:

Rise Time	$t=R_{eq}$ C t/T
-30 volts to +10 volts	R in megohms
	C in uuf
	T in usec

The fall time of a +OR circuit driving a +AND circuit can be computed in a similar manner.

2.04.00 DIODE CASCADING

The back resistances of the diodes in AND/OR circuits act as a load on the driving circuits. When this effective back resistance is too low, the driving source (another diode circuit or cathode follower) cannot supply enough current to maintain proper down levels or maintain required rise/fall times. Diode AND/OR circuits with 5, 6, and 7 inputs are used and these circuits present the problem of lowered effective back resistance.

A six input AND circuit is shown in Figure A8 before and after cascading. Back resistance of an AND circuit is especially important when only one input is at -30 volts and is maintaining the output down level. This condition is shown in Figure A8a. Assume that each diode has a back resistance value of 400K. Each input that is at +10 volts can be represented as a resistor of 400K because each of these diodes is cut off. Five resistors of 400K in parallel give an equivalent resistance value of 80K as shown in Figure A8b. Therefore, the 80K acts as additional load to the -30v driving source.

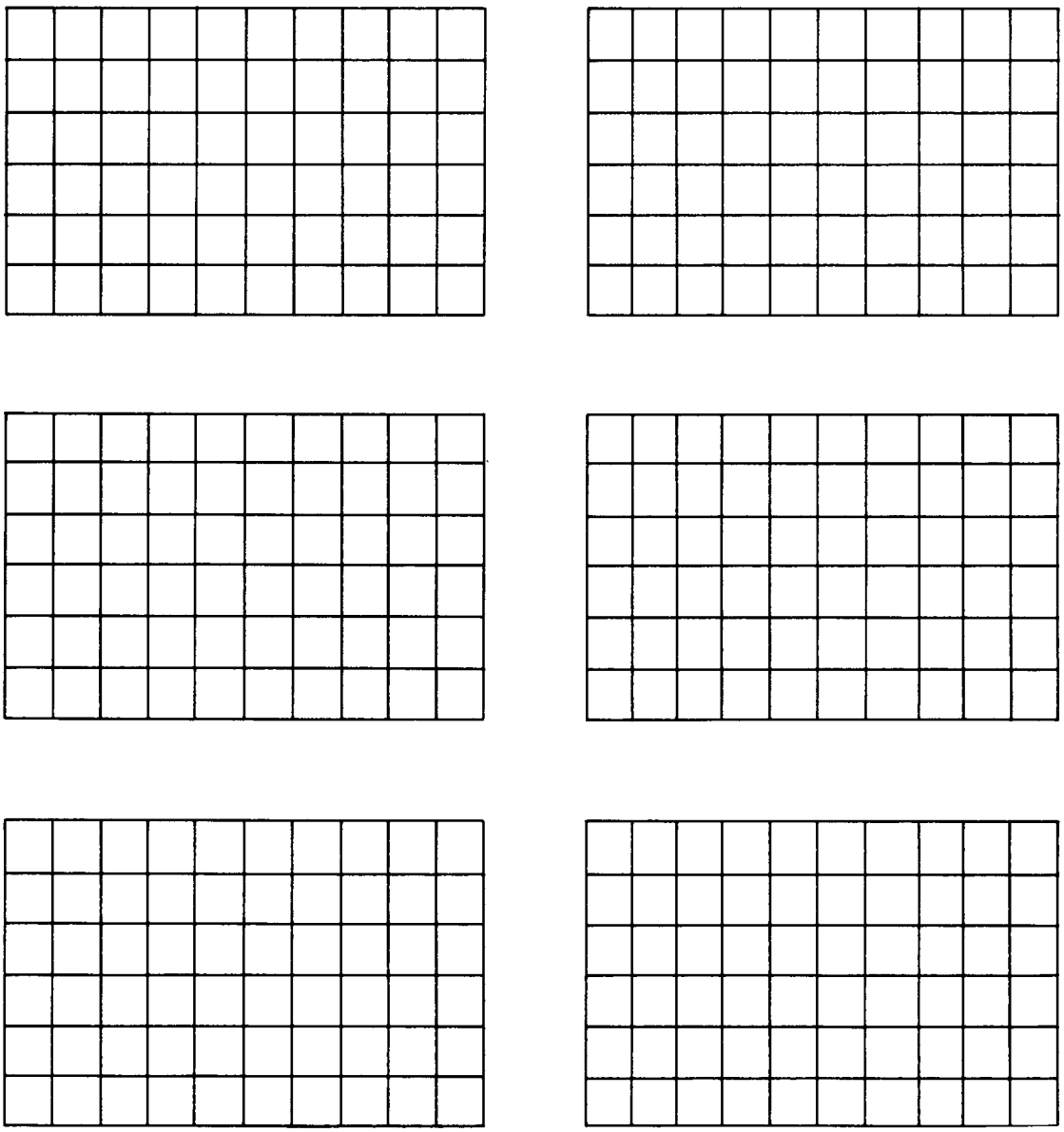
When a diode is placed in series with each pair of input diodes (A8c), effective back resistance is increased to 170K (A8d). The driving source now sees almost twice as much resistance offered by the inputs. Cascading cuts down the current requirements for this circuit. If the -30v input is a high impedance source (such

as an OR circuit), excess current drawn by cut-off diodes can raise the down level. Low impedance sources are also limited as to the amount of current that can be supplied to a positively returned load.

Multiple input OR circuits present the same problem when all inputs are down at -30 volts except one. The one leg rising to +10 volts must handle the charging current from C_S and the cut-off diodes. The lowered back resistance of the cut-off diodes affects rise time and cascading increases the needed back resistance.

The original design of AND/OR circuit networks determines whether cascading saves tubes or simply represents a waste of diodes.

Cascaded AND/OR circuits are designated A_C and O_C, respectively, in logic blocks. An example of AND/OR usage is shown in the Appendix and in the illustration "12 to 6 Translator."



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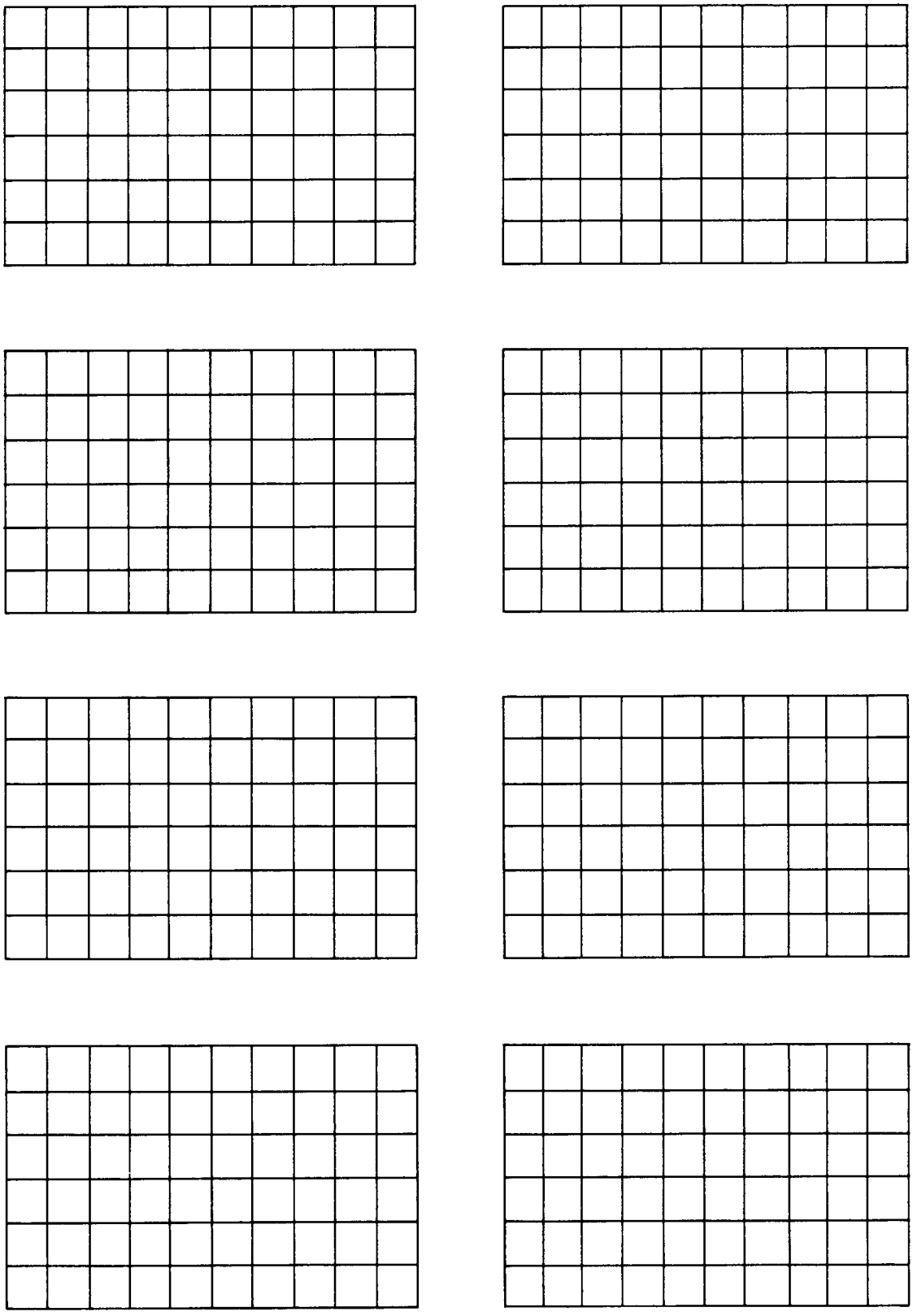


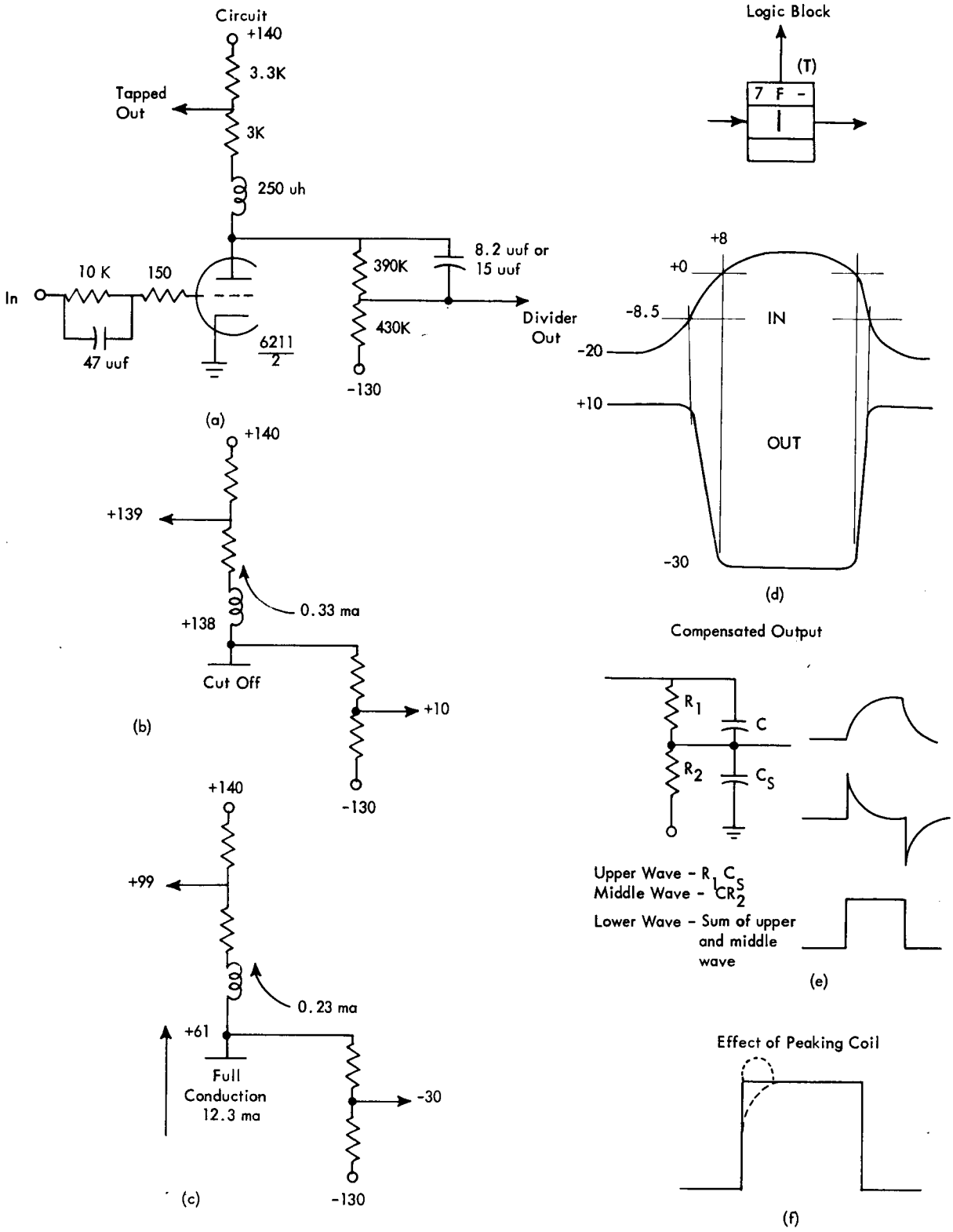


FIGURE A9. STANDARD INVERTER

2.05.00 INVERTER (I) (I_K)

The standard inverter in the 700 series is the high-speed inverter (Figure A9). The inverter circuit produces a negative shift at its plate when a positive shift is applied to the grid, and a positive shift at its plate when a negative shift is applied to the grid. This property makes it useful in inverting logical conditions, such as changing binary zeros to binary ones. The inverter is also a level setter and pulse shaper because of its amplification properties.

The large resistance in the plate circuit gives a large voltage swing, but does not slow down the signal transition appreciably. The coil in the plate circuit speeds the rise of the plate voltage. When the tube is cut off, the coil produces a voltage which for a short time makes the plate more positive than it would be without the coil. The coil causes a slight overshoot in this rise of the plate voltage but has practically no effect upon the fall time of the circuit. The effect of this coil on the voltage at the plate is shown in Figure A9f. The lower dotted line represents the voltage without the coil; the upper overshoot represents the voltage produced by the coil. The resultant shape of the voltage shows the tendency to square the rise; this results in a fast-rising voltage at the plate. The 10K resistor and its by-pass capacitor are used for grid current limiting when a low impedance driving circuit is used. The inverter has a nominal rise time of 0.2 usec (microsecond) and a fall time of 0.25 usec. An I_K is the same circuit but uses one half of a 5965 tube.

2.05.01 Circuit Description

The minimum input requirements are +5 volts and -13 volts. Assume that the input voltage is -20 volts. The tube is well beyond cut-off because cut-off bias is -8.5 volts for a 6211. The divider output is at +10 volts because 0.33 ma are flowing through the divider circuit (Figure A9b). The DC resistance of the coil (25 ohms) is disregarded.

When the input rises to +5 volts or higher, the tube is in full conduction (Figure A9c). With a load of 6.3K, tube current is found to be about 12.3 ma. Grid current keeps the grid slightly above ground. The current flowing through the plate load causes the voltage at the plate to drop to +62 volts. However, the divider circuit is tied to the plate and the +62v level. Divider current drops to 0.23 ma and this current adds to the tube current through the plate load. The voltage at the plate is lowered to +62 volts and the divider output is -30 volts. Although this method of calculating plate current is an approximation, its simplicity overrules the small error involved.

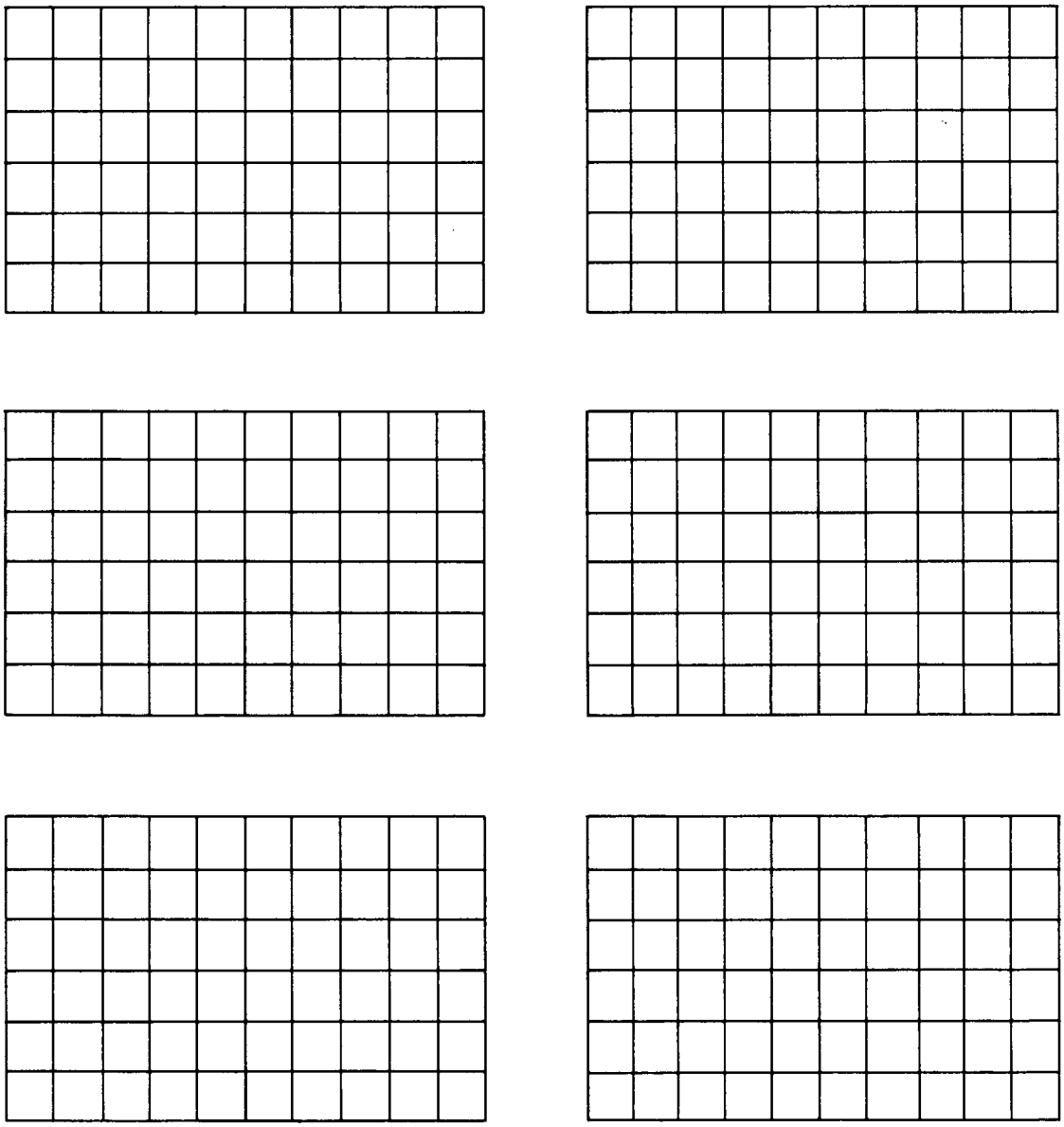
The level-setting characteristic of the inverter circuit is shown in Figure A9d. Because the circuit is fully operated by only a portion of the input pulse, the amplification of the tube resets the levels of the pulse. Pulse shaping is aided by both the amplification and the action of the peaking coil.

2.05.02 Compensated Output

The circuit produces a fast rise and fall at the plate. This voltage shift must be fed to the next circuit where stray capacitance acts upon the shift. Figure A9e shows that if C_S is charged through R_1, the output wave form is distorted. However, by adding a compensating capacitor C, the wave form produced by CR2 adds to the

output. Thus C_S has a fast charge path and the output more nearly represents the voltage shift at the plate. The compensating capacitor is 8.2 uuf or 15 uuf depending on the input capacity of the next circuit.

The divider output is high impedance and must feed a cathode follower directly (high impedance input). The voltage for a tapped plate swings from +139 volts to +99 volts, and at the divider output from +10 volts to -30 volts.



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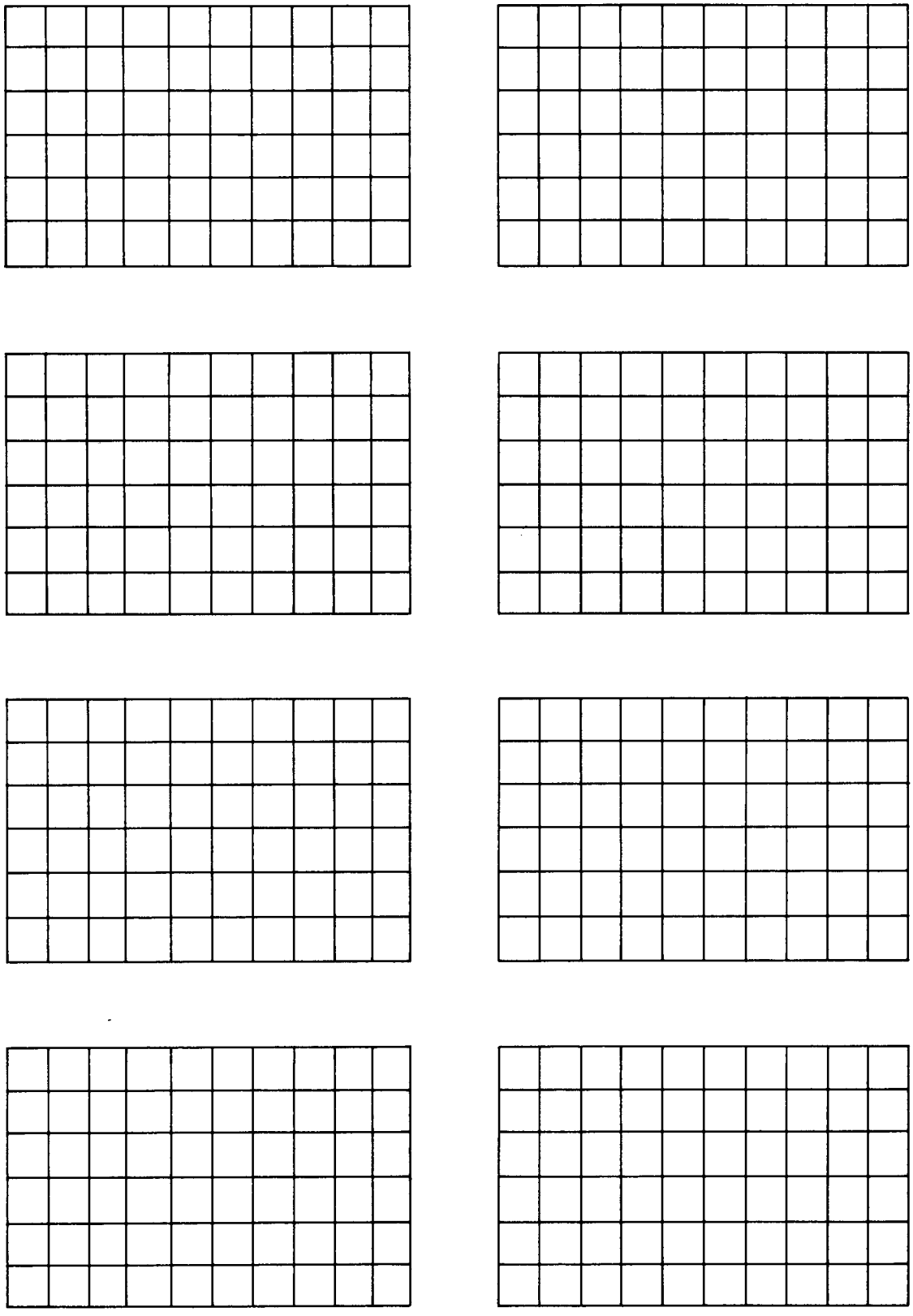
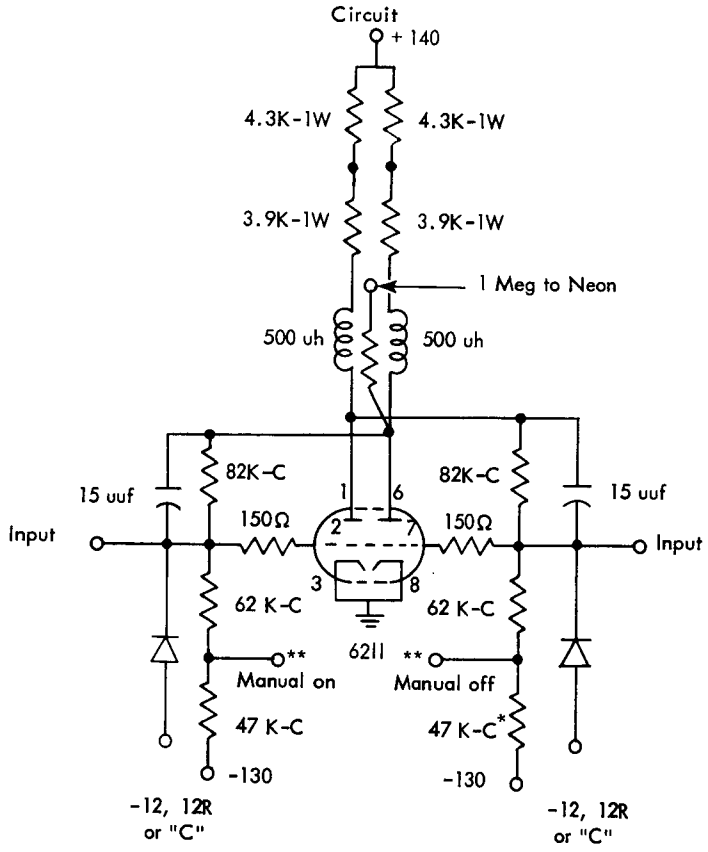
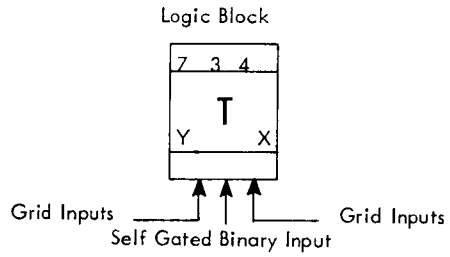






7= Tube Number
3= Manual On Pin
4= Manual Off Pin
Y= Reset On
X= Reset Off

Notes:

* Alphabetic suffix denotes that resistors are tolerance mached.

** If manual reset is not used, combine the 62K and 47K resistors into one 110K resistor.

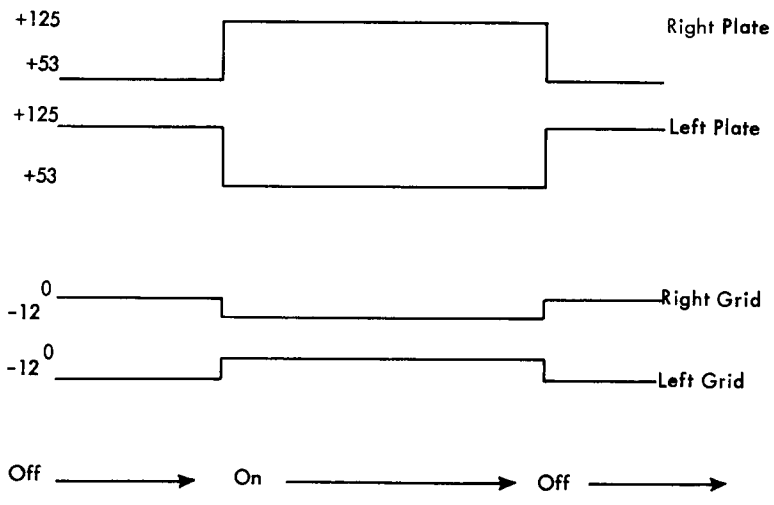


FIGURE A10. HIGH SPEED TRIGGER (T)

2.06.00 TRIGGER (T)

A trigger is a bistable multivibrator; that is, it remains in either one of two stable states until an external signal forces it to assume the other state. This forcing action is called triggering or flipping; another name for the trigger circuit is "flip-flop." The bistable property of a trigger makes it useful as a storage device. It is used in registers, counters, and gate-forming circuits.

2.06.01 On and Off Convention for Triggers

A trigger is said to be on when its left tube is conducting. Therefore, the left side is called the "on-side," and the right side is the "off-side." In the "on" state, the left grid is up, the right plate is up, the right grid is down, and the left plate is down (Figure A10). If a trigger is used for storing binary information, it is storing a one when on and a zero when off.

2.06.02 General Trigger Circuit Operation

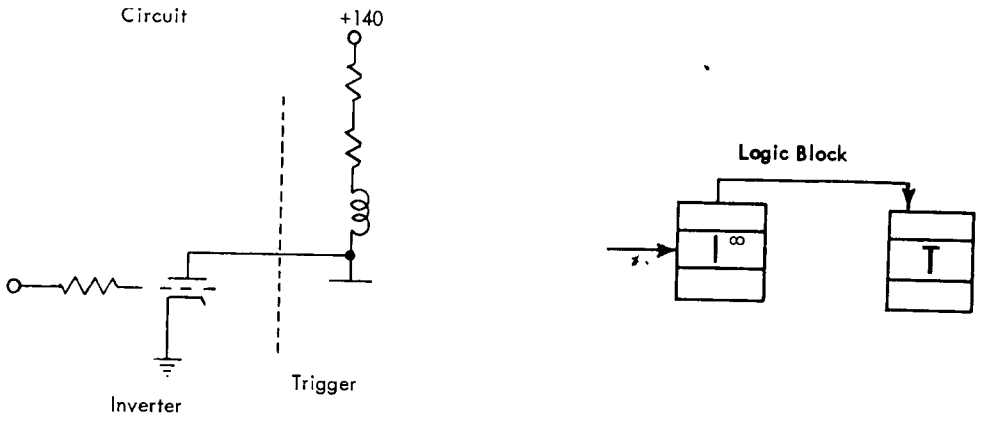
Basically, a trigger circuit resembles two inverter circuits in that each plate output is coupled to the opposite grid. In one stable state, the left tube is in full conduction (about 9.5 ma) while the right tube is cut off. In the other state, the right tube is in full conduction while the left tube is cut off. To change from one state to another, an external signal must be applied to a sensitive point in the trigger circuit.

For example, assume that the right tube is conducting (trigger off). The right plate is down; that is, its voltage is considerably less than +140 volts, while the left plate is up (near +140 volts). One method of flipping this circuit is to apply a negative pulse to the right grid. Because the right tube is conducting, grid current keeps the grid at about zero volts. The negative input pulse causes the right tube to cut off; consequently, the right plate voltage rises. This rise is then coupled through the plate-to-grid voltage divider (cross coupling circuit) to the left grid, pulling this grid voltage up toward ground. The left tube then begins to conduct, pulling its plate voltage down. This shift at the plate of the left tube is coupled back to the right grid and reinforces the initial action. The cross coupling circuits speed the regenerative action and the circuit stabilizes with the right side cut off and the left side in full conduction. The input pulse can now be removed without reflipping the trigger, because conduction on the left side holds the right side cut off.

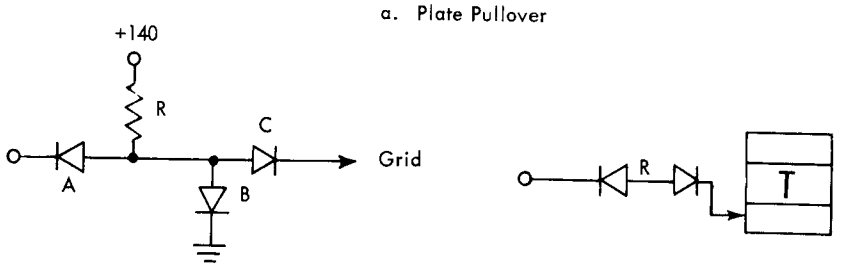
The trigger can also be flipped by applying a positive pulse to a non-conducting grid or by lowering the plate voltage of a cut-off side through an external circuit. In any case, an input pulse must initiate a regenerative action to cut off the conducting tube and bring the non-conducting tube into full conduction.

2.06.03 Specific Components in a Trigger

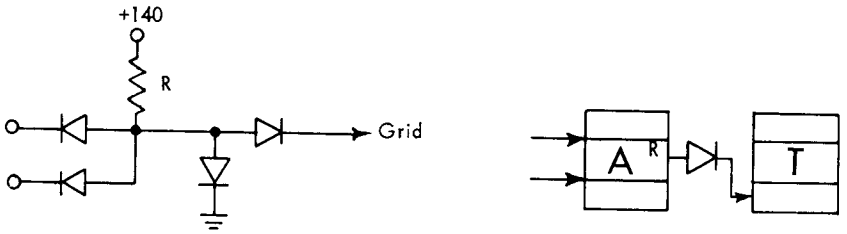
Each plate is coupled to the opposite circuit through a compensated voltage divider. High-speed operation is obtained with the aid of the peaking coils in each plate circuit. The plate circuit may contain one resistor or two from which a reduced plate voltage swing may be taken as an output.



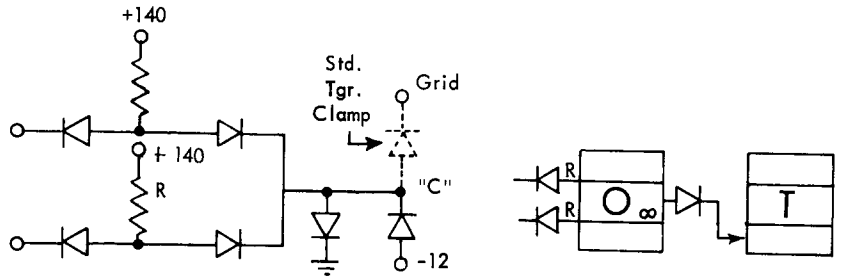
a. Plate Pullover



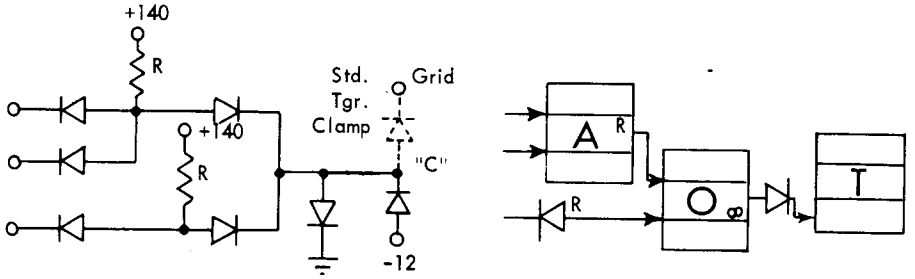
b. Single Leg AND Input



c. +AND Input



d. +OR Input



e. +OR Fed by Single Input and a +AND

FIGURE A11. TRIGGER INPUTS

To prevent delay in the flipping of a trigger caused if the down grid voltage is far below cut-off, the grids are clamped by diodes. The plate of the diode is a -12v power supply. Any attempt to lower the grid voltage below -12 volts causes the clamp diode to conduct harder. With this procedure, the grids need to rise only a few volts to start conduction.

2.06.04 Electronic Reset

Because either side of a trigger can go into conduction when power is first applied, a provision must be made to establish a specific status. The trigger may be reset with the output of the reset cathode follower (K_R) applied at the desired reset point. The reset cathode follower is usually preceded by either the pulse forming inverter (I_{PF}) or a single shot (SS). The reset point is the plate of the -12v clamp diode. The reset cathode follower provides -12v as a clamp voltage and changes to zero volts for reset. Bringing the plate of the clamp diode to ground forces a non-conducting grid up; that side of the trigger goes into conduction. The reset pulse lasts long enough to insure that the regenerative action is complete. The notation of reset is placed in the title section of the logic block (Figure A10). The notation on the left indicates "reset on" and on the right indicates "reset off." A trigger may have several resets, but only one takes place at a time. The origin of the reset is marked on the Systems page.

Triggers may also be reset by the output of other triggers but in this case, they are pulled over (Book A, section 2.06.06) in the usual manner rather than by applying the pulse to the reset point. All triggers with the letter X in either the right or left-hand corner (depending on whether the trigger is to be reset off or on) are reset by "power on reset" through a reset cathode follower.

2.06.05 Manual Reset

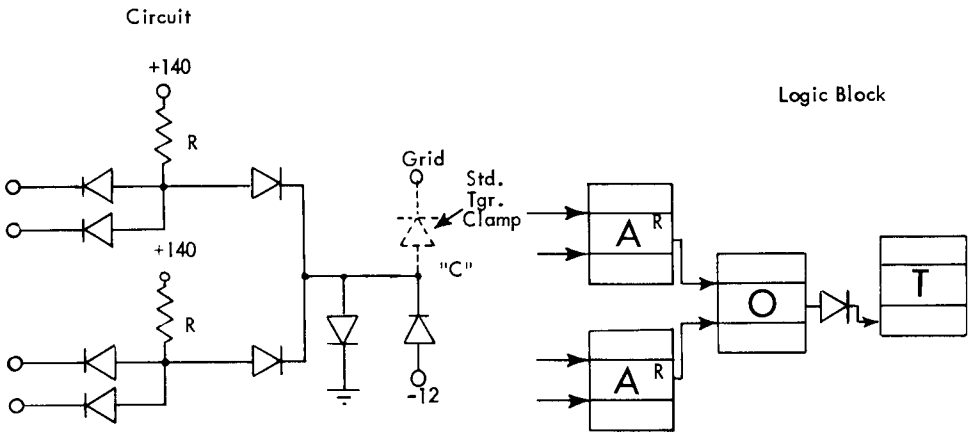
A manual method of flipping helps to test the trigger circuit. The points in Figure A10 marked "manual on" or "manual off" are wired to pins on the panel. If a trigger is on and the manual-off pin on the panel is touched by a tweaking probe, the trigger is flipped off. The tweaking probe is merely a line connected through a by-passed, high-impedance resistor to ground. The ground connection pulls the tweak points (manual points) up toward ground, thus providing a positive shift at the grid to flip the trigger. Tweaking the manual-on point turns the trigger on if it was initially off.

2.06.06 Inputs to a Trigger

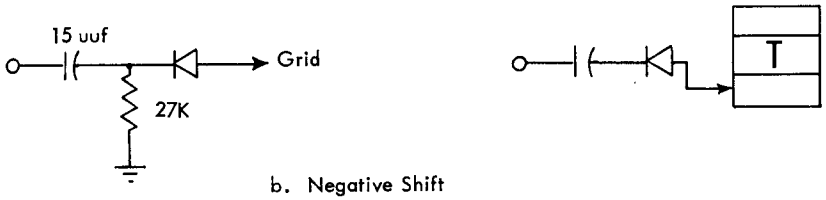
Figures A11-A14 show several inputs to a trigger circuit. These are explained as follows:

Plate Pullover Input

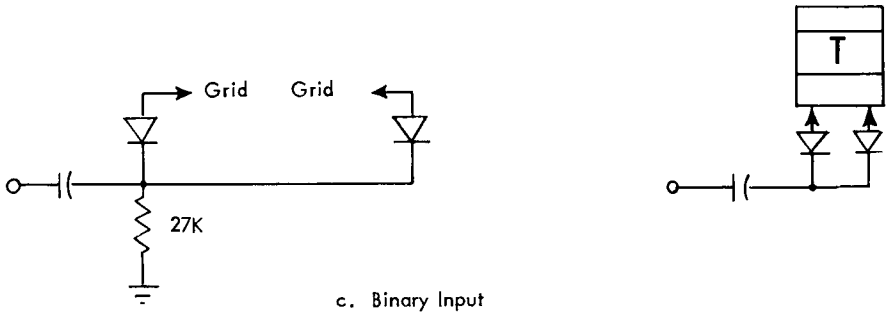
The simplest input is the plate pullover type (Figure A11a). The plate pullover input is merely an inverter whose plate is connected to a plate of the trigger circuit. The plate load of the inverter is the plate resistor of the trigger. When a positive pulse is applied to the grid of a pullover inverter tube connected to an up plate of a trigger, the negative shift at the plate caused by conduction through the plate resistor of the trigger causes the trigger to flip. As long as the input to the pullover inverter



a. +OR Circuit Fed By 2 +AND Circuits



b. Negative Shift



c. Binary Input

FIGURE A12. TRIGGER INPUTS (cont'd)

remains positive, no external signal on any other input to the trigger can flip it. That is, the plate pullover method exhibits holding action. If the inverter were connected to a down plate of a trigger, then the application of a positive gate to the pullover inverter grid would not affect the trigger in any manner other than producing a holding action.

DC Inputs

Several AND/OR circuit configurations are used as DC trigger inputs. All are grid inputs and they exert holding action on the trigger when the DC input is up. Each circuit contains a clamp diode to prevent driving the grid above ground. Although normal AND/OR circuit outputs swing between +10 volts and -30 volts, the ground clamp and the -12v grid clamp keeps the swing between 0 volts and -12 volts.

A typical application is the one-legged AND circuit feeding the trigger (Figure A11b). Assume that the input is -30 volts and the grid is non-conducting (-12 volts). The base of the limiting resistor is -30 volts and diode C is cut off. As the input rises to +10 volts, the base of the resistor rises to zero and is held at that point by the ground clamp, diode B. Diode C starts to conduct at -12 volts and continues to conduct, forcing the grid up. The tube conducts; the trigger flips and is held in this status by the holding action of the input circuit. When the input drops to -30 volts, the voltage at the base of the resistor falls to -30 volts also. Because the trigger grid stays at zero volts (conducting), diode C cuts off as soon as the input passes zero volts on the fall. Only the holding action has been removed and the trigger does not flip back until impulsed by a different input.

The same operation takes place when the OR circuit block feeds the trigger (Figure A11d). The infinity sign in the block means that the return resistor for the OR circuit is in the grid circuit of the trigger. In all cases, the diode closest to the trigger block indicates the polarity of the pulse operating the trigger.

Figure A11d shows the normal clamp diode used as an input. An additional diode is added for clamp and reset purposes. Usually the clamp diode is used as an input when several input circuits are tied to the same grid. This procedure increases the impedance of the grid circuit in the same manner as cascading in AND/OR circuits. This increased impedance is necessary to prevent unbalancing the grid circuits and producing unstable triggering.

Negative Shift Input

The negative shift input (Figure A12b) is an AC input and does not exhibit holding action. The negative facing diode blocks a positive shift and allows a negative shift to cut off the tube. Because of the RC circuit involved, recovery time of the input circuit is a necessary consideration. A notation, such as 0.2 usec, may be placed near a shift input to denote the recovery time. The notation 0.2 usec means that the input must be positive for 0.2 usec before a negative transition begins. The RC circuit must recover (time out) to transmit the full shift to the grid.

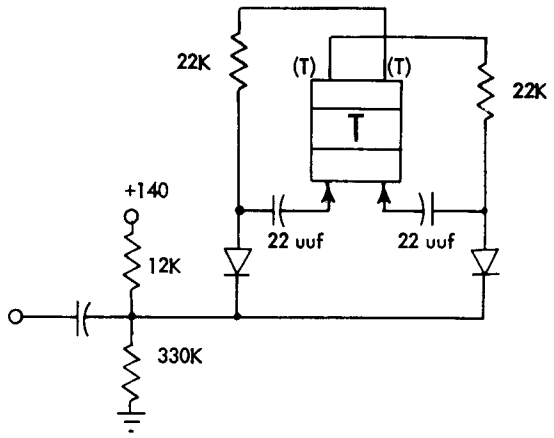


FIGURE A13. SELF GATED BINARY INPUT

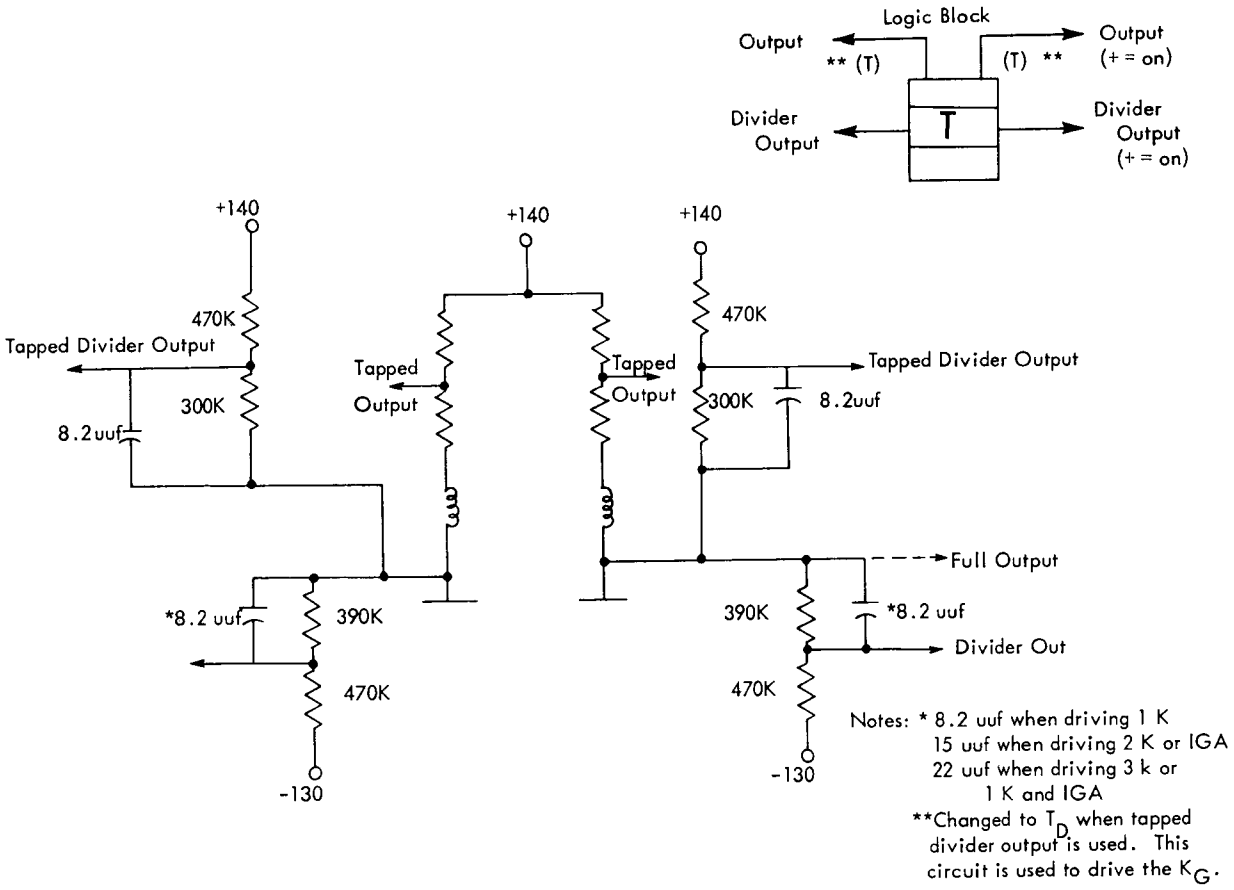


FIGURE A 14. TRIGGER OUTPUTS

Binary Input

The binary input is a negative shift input to a trigger and allows it to be flipped regardless of its previous state (unless it is being held by another circuit). A binary input is indicated when the same signal is applied to both the left and right grid (Figure A12c). For example, if the trigger is off and it is fed a pulse through a binary input, the trigger is flipped on. If another pulse is then applied to the binary input, the trigger is flipped off.

One grid is initially at ground, and the other is about -12 volts. The negative shift begins at ground and pulls the conducting grid negative. The first twelve volts of the negative shift cannot affect the cut-off grid because the binary input diode connected to that grid is cut off. By the time this diode is ready to conduct, the regenerative action initiated by the negative shift on the opposite grid produces a positive shift at the formerly cut-off grid.

If the differentiated spike is narrow enough and not excessively large in amplitude, it does not interfere with the positive shift at the formerly cut-off grid. However, if it is too wide or too large in amplitude, it may interfere with the positive shift, causing the trigger to flip back to its initial state. For this reason, the binary input should not be fed a pulse of very great amplitude.

Self-Gated Binary Input

The most widely used binary input to a trigger is the self-gated binary. It is used when pulse amplitude and width would affect a normal binary input. The circuit is shown in modified block form in Figure A13. When the ordinary binary input exhibits self-gating action for the first 12 volts of the negative input shift, the self-gated input exhibits this property for the full pulse amplitude because of the different voltage levels maintained at the input diodes.

The voltage at the junction of the 12K and the 330K resistors is about +135 volts. When the input is a -30v shift, the voltage at the diode junction is then +105 volts. Now the potential at the junction of the diode, the 22K resistor and the 22-uuf capacitor of the conducting side of the trigger, is about +132 volts. The potential at this same point on the cut-off side is about +94v. Thus, the diode on the cut-off side cannot conduct while the one on the conducting side conducts. The conducting grid is brought down; this side ceases to conduct while the cut off grid is brought up to ground and starts to conduct.

The driving circuit may be either a standard cathode follower with the minimum load or a standard 6211 inverter tap or trigger tap. The inputs are 25v to 35v negative shifts. The input fall time must be less than 0.25 microsecond for a 25v input and less than 0.4 microsecond for a 35v input. Recovery of the input network limits the frequency of operation to 150KC maximum (with minimum input signal). The trigger output rise time is 0.35 microsecond; the fall time, including delay, is 0.2 microsecond.

2.06.07 Input Requirements for the Trigger

The following are minimum requirements for flipping a trigger with various inputs:

Plate Pullover: standard inverter input.
DC: lower level -20 volts to -30 volts; upper level +5 volts to +15 volts.
Minus Shift: 25v minus shift; 60 volts/usec minimum slope.
Binary input: 25v minus shift; 60 volts/usec minimum slope.

2.06.08 Outputs from the Trigger

There are four types of outputs from a trigger (Figure A14). The full plate swing of either plate may be used, or the plate resistor may be tapped when a smaller swing is needed. Generally, this tapped output is used for feeding binary inputs of other triggers. A standard signal level may be obtained from a voltage divider connected to either plate. If the divider is not used, it is not wired into the circuit. When driving a plate-level cathode-follower K_G (702-705 components only), a special divider from the trigger plate to +140 volts is used. The output of this tapped divider (TD) is about the same as the tapped plate.

2.06.09 Voltage Levels in the Trigger

The following are nominal voltage levels in a high-speed trigger:

Full plate: +53 volts and +125 volts (divider connected).
Tapped plate: +94 volts to +132 volts (divider connected).
Divider output: -30 volts to +10 volts.
Grid: Tends to go down to -25 volts but is clamped by diode at -12 volts.
Tends to go up to +17 volts but is grid-clamped at about ground.
Manual reset points: -74 volts to -79 volts.

When the voltage divider is not connected to the plate output, the upper plate level is +125 volts, and the lower level is only a few volts higher than the +53 volts. A trigger may produce some delay and gives a nominal rise time of 0.35 usec and fall time of 0.3 usec.

2.06.10 Block Representation of the High-Speed Trigger

A single trigger may have many outputs; it may have different inputs to the same grid or the same type of inputs to opposite grids. A grid input may be shown in either lower corner. A self-gated binary input is indicated merely by a straight line drawn into the middle of the bottom of the block. Diodes closest to the trigger block indicate the polarity of the voltage affecting the trigger.

A tapped output is represented by a line coming out of the top of the block near one side and with a T placed next to the line. Full plate outputs are represented similarly with no T. The divider output is drawn from the side of the block. When the divider is changed to drive a plate level cathode follower, a TD is placed next to the line at the top of the block.

2.06.11 Special Features

To indicate the state of a trigger, a neon is usually connected through a one-meg-ohm resistor to the right plate. The neon is mounted on the panel and is returned to ground. It is lit when the trigger is on. A trigger circuit always uses the half tubes in the same envelope. If a manual reset is not used, the 62K and 47K resistors are combined into one 110K resistor (grid return). Values of compensating capacitors are changed in the same manner as in the inverter.

2.06.12 Application of Triggers

Trigger Registers

Trigger registers are frequently used as temporary storage throughout the 700 series An example of a four-position register is shown in Figure A15. The register is reset by opening the -250v bias at the off-side. It may also be reset by "reset register." When this line goes positive, it resets the triggers off through the +DC inputs to the off-side of each trigger. The triggers store the information fed to the inputs. At read-in-register time, the input lines are sampled at the AND circuits across the bottom of Figure A15. If any of the AND outputs goes positive, the trigger tied to it through a +DC input is turned on. This information is stored here until the next reset time. The output of the register is available from cathode followers tied to the off-side plates of the triggers.

Leslie Ring

As shown in Figure A16, the on-side grids of alternate triggers are connected together and each set is connected to opposite sides of binary connected trigger (T_A). The input to the ring is fed to the binary trigger, the negative shift at the on-side plate is fed to T_1, turning T_1 off. Note that at T_2, there is now a negative pulse turning the trigger on while a positive shift to the on-side grid is not seen by the trigger, since the negative-shift input is being used. With the next negative shift to the binary trigger, the trigger goes off, sending a negative shift to T_2 and T_4. This negative shift turns T_2 off. The fact that T_2 is going off gives a negative shift to T_3, turning it on. Again, note that T_3 is being hit only at the off-side grid. The ring steps around in like manner until the last trigger goes off. If the output of the last stage is not fed back to close the loop, the ring stops when the last trigger goes off.

Trigger Counters

Pulses can be accumulated in binary triggers in the form of trigger counters. As shown in Figure A17a, the counter is reset with all the triggers off. The input is fed to the first stage only. As the first negative shift is fed to the input, the first stage goes on, making its off-side plate go plus. This pulse shift is fed to the second stage with no effect. As the second negative shift at the input turns the second stage on. Note at this time that only when a trigger goes off does it affect the following stage. With a third impulse, the first stage is turned on, leaving the first and second stages on and the third stage off. With the fourth negative shift at the input, the first trigger goes off, feeding a negative shift to the second stage, and turning it off. As the second stage goes off, the negative shift from its off-side

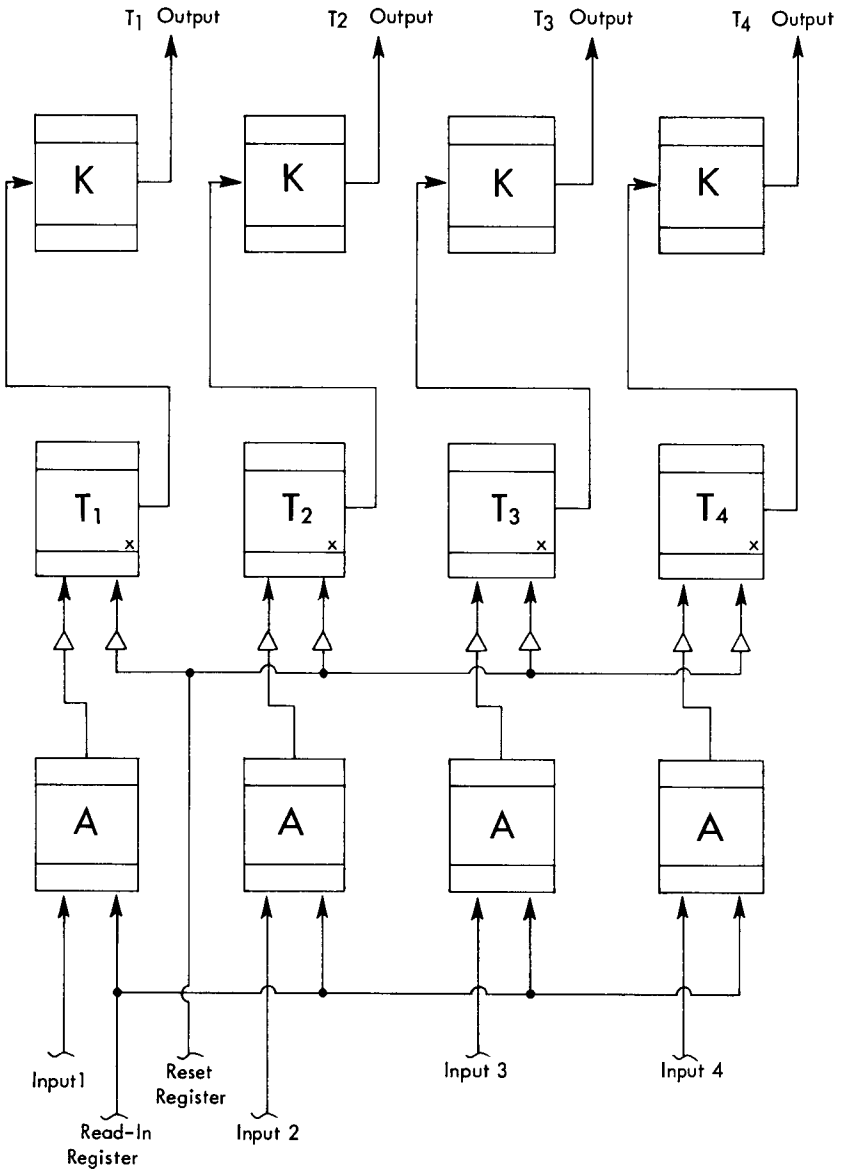


FIGURE A15. TRIGGER REGISTER

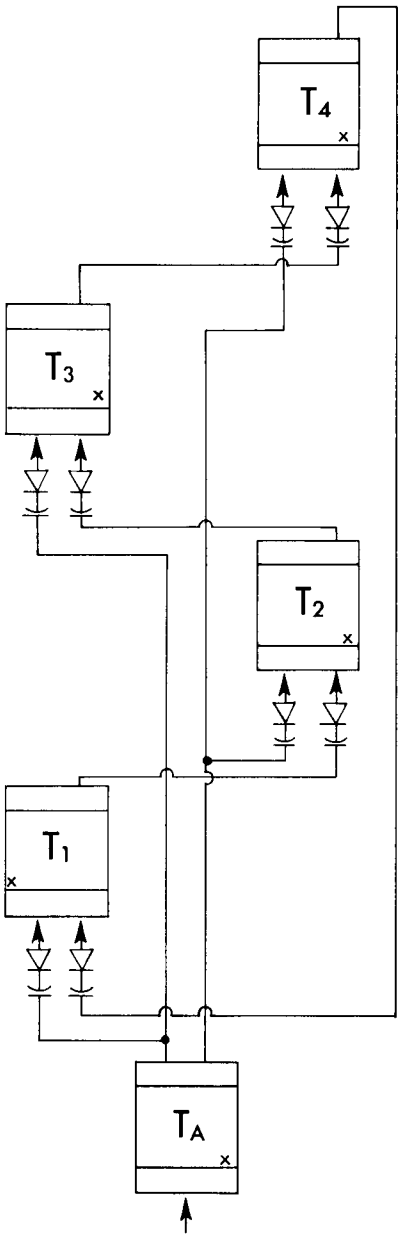


FIGURE A16. LESLIE RING

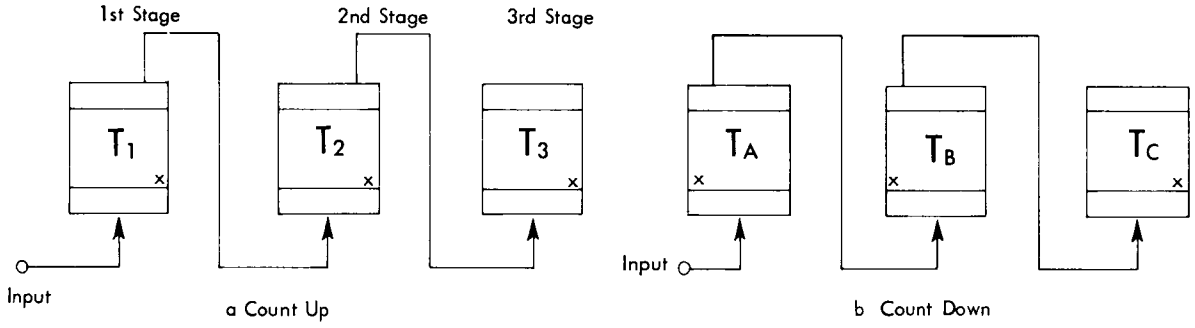
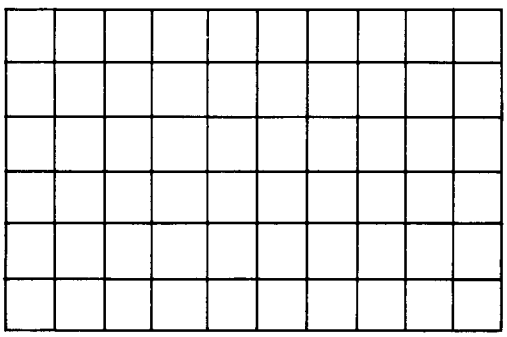


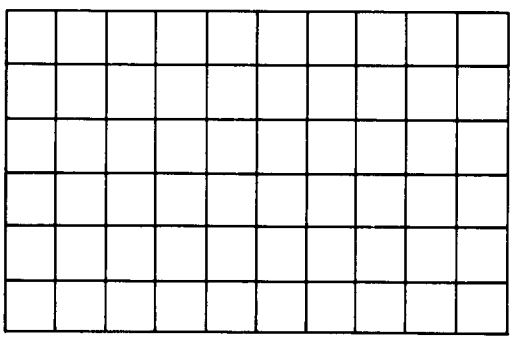
FIGURE A17. TRIGGER COUNTERS

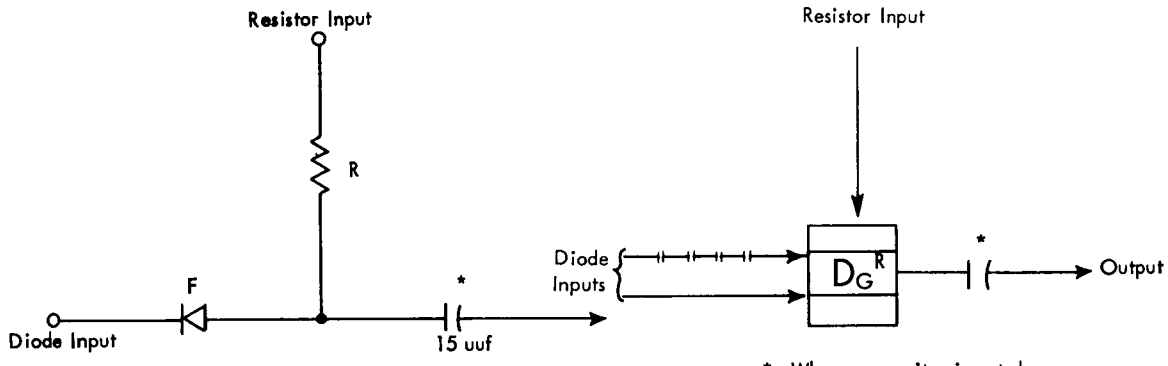
plate turns the third stage on. By correlating the triggers that are on with the number of pulses fed to the system, the first stage may be said to represent one, while the second stage represents two, and the third stage represents four. At this time, we have fed four pulses to the counter and have turned on the third stage indicating the sum of the input pulses. With the fifth pulse, the first stage again goes on, leaving the third stage on and indicating the accumulation of four and one.

As the counter accumulates, it may be shown that the sixth pulse would turn on the second stage. Likewise the seventh pulse turns the first stage on, leaving the equivalent of four, two, and one in the counter. With the eighth pulse, all positions are turned off, restoring out counter to its original condition. This counter is said to be an octonary counter. Similarly, counters with various radices (base numbers) may be constructed. To achieve this, various forms of blocking and feed-back circuits are used when the radix of the counter is not an integral power of two. The illustration discussed above is sometimes called a "count-up" counter. There is application in the 704 for "count-down" counters. Such a configuration is shown in Figure A17b. In this application the counter is usually set up to some predetermined value, and pulses are subtracted from this value. Let us say that by some means the counter is reset, as indicated by the X's in Figure A17b. This would put a 3 in the counter. To subtract 1 for each input pulse, the counter goes to zero with three pulses. The first pulse to the counter turns the first stage off. Using the output from the on-side, note that there is no further action in the counter since a positive shift from the on-side of the first stage has no effect on the binary input of the second stage. As the next pulse comes in, the first stage is turned on. This gives a negative shift to the second stage, turning the second stage off. The third pulse turns the first stage off leaving the counter with all zeros. The output of the triggers is tested to determine when the counter goes to zero, thereby indicating when a predetermined number of pulses has been sensed.

Note that the count-up and count-down counters are basically alike, but the carry from stage to stage is taken from opposite plates. A reason for using the count-down counter is that the counter does not have its "ripple-down" just before it registers zero. The term "ripple-down" pertains to the action of a count-up counter when all the triggers of the counter are on and the next pulse must turn each of the triggers off in succession. Ripple-down also describes the action in a count-down counter when all the triggers are off and the next pulse turns each stage on. Since it takes a definite time to flip a trigger, the time is accumulative in ripple-down and a considerable delay is introduced in the system.



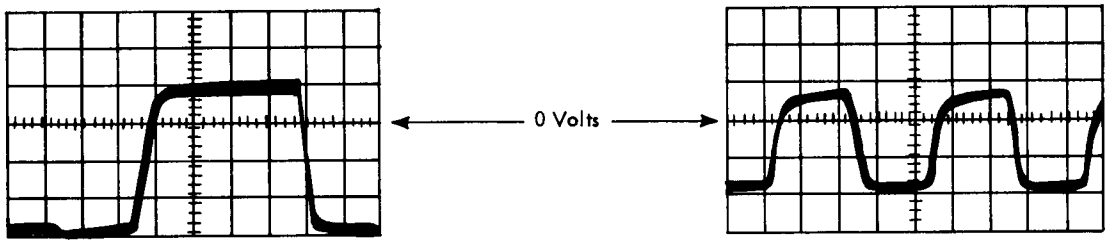




(a) Circuit

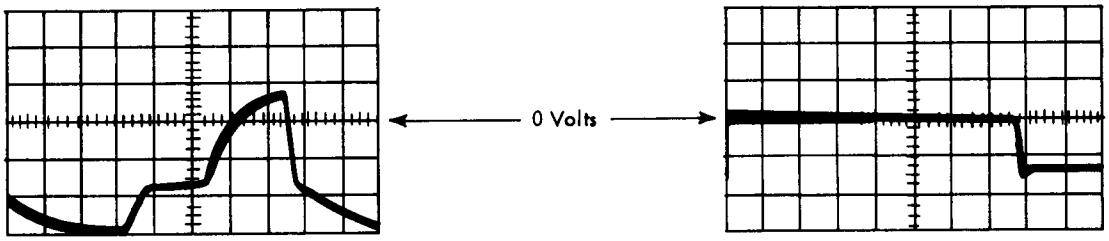
* Where capacitor is not shown with block symbol it is not in the circuit.

(b) Logic Block



Resistor Input

Diode Input



Junction Point

Output (Trigger Grid)

(c) Waveforms

1 usec/sd 10 v/sd

FIGURE A18. DIODE GATE - D_G

2.07.00 DIODE GATE (D_G)

The diode gate acts somewhat in the same manner as an AND circuit and is used to flip a trigger. It is used where speed of operation is not essential.

2.07.01 Circuit Description

The upper end of the 39K resistor is connected to a circuit (such as a divider output of a trigger) that will supply a nominal +10v to -30v gate pulse. The diode input is the output of a special cathode follower that gives a +10v to -14v pulse. The prerequisite for proper operation is that the gate input overlap the diode input.

A typical operation is shown in Figure A18. All the pictures have the same time relationship. The diode input shows two +8v to -18v pulses (an example of normal circuit variations, hence the usage of "nominal"). The gate of +9 volts to -30 volts is going to select or "gate" one of the pulses at the diode input. The junction point is initially at about -30 volts and the diode is cut off. As the gate rises to +9 volts, the junction point rises exponentially to -18 volts and is held at that point by the diode's going into conduction. As the diode input rises to +8 volts, the diode again is cut off and the junction point rises exponentially toward +9 volts. The capacitor is now charged. When the diode input falls to -18 volts, the diode's conducting provides a discharge path for the capacitor and the junction point falls sharply to the diode input level of -18 volts. The diode maintains this voltage level until the gate falls. When the gate falls, the diode cuts off and the junction point falls exponentially to -30 volts. The sharp fall from +9 volts to -18 volts is coupled through the capacitor to the trigger grid. The negative shift forces the grid from 0 volts to -12 volts (held by -12v grid clamp) and causes the trigger to flip off. The trigger was turned on by a different circuit.

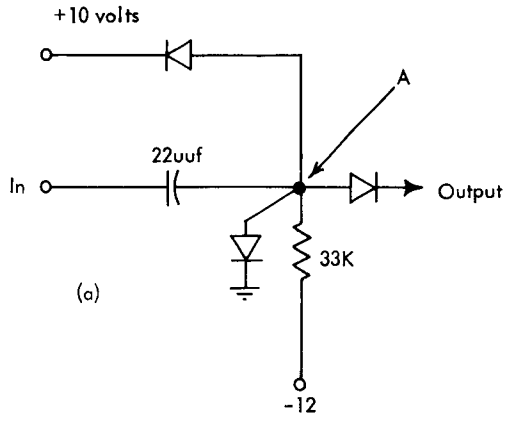
The above description has shown that coincidence of the gate and diode input is necessary for the diode gate to flip the trigger. The exponential rise and fall at the junction point do not affect the trigger.

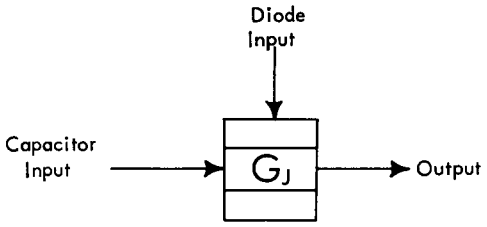
2.07.02 Variations

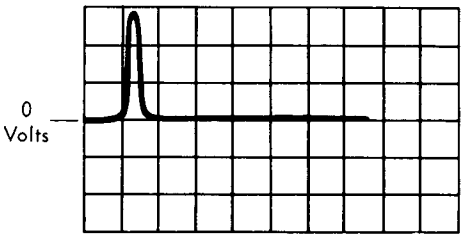
A second diode input may be added (broken line, Figure A18b) to the circuit. The D_G must then have coincidence of all inputs to operate; a negative shift into either diode input causes a negative shift output.

The resistor input can be fed from a trigger tap at plate level. The diode input must be fed from a special plate level cathode follower to give the same voltage relationship as previously described.

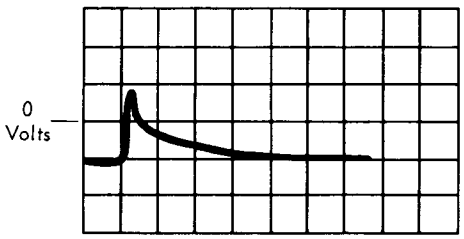
The capacitor is shown outside the diode gate block. When it is not shown outside the block, it is not in the circuit. There are special cases in the drum where the output of a diode gate is fed directly to the grid of a cathode follower. In this case, the circuit acts as an AND circuit. However, the capacitor can be placed in the output of the cathode follower for AC coupling purposes. In all diode gate blocks, the upper section contains the location of the junction point.



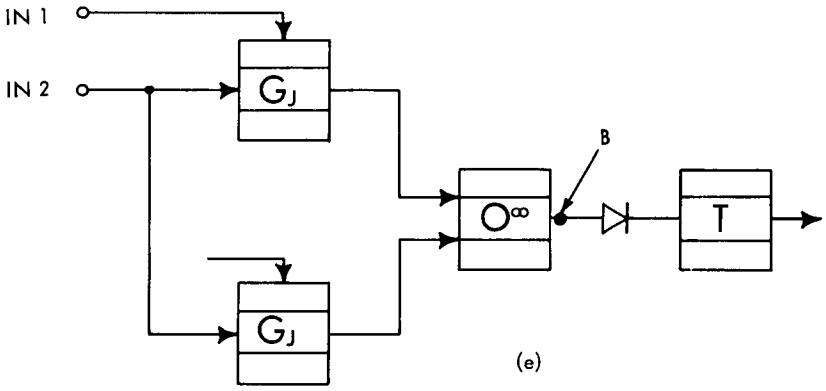




b. Capacitor Input 20V/sd 1 usec/sd



c. Point B 10V/sd 1 usec/sd



Center line = 0 volts

d. Point A 10V/sd 1 usec/sd

FIGURE A19. DIODE GATE - G_J

2.08.00 DIODE GATE (G_J)

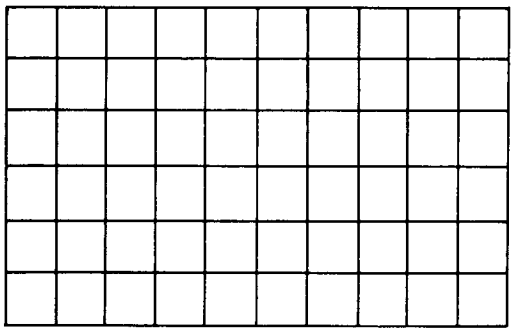
The diode gate G_J serves a purpose similar to that of the diode gate D_G. It is a gated input circuit and flips a trigger with a positive shift. The circuit appears in certain registers in CPU. The G_J operates faster than the D_G.

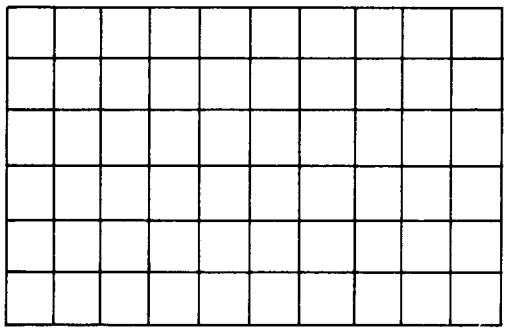
2.08.01 Circuit Description (Figure A19)

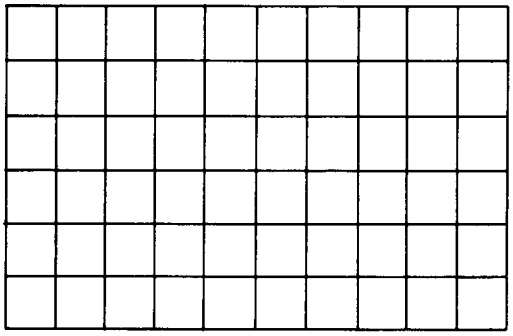
The diode input is a +10v to -30v gate from a cathode follower, while the input to the 22-uuf capacitor is a sharp 55v + pulse, originating in the wave-form generator peaker (PKR_Z). This pulse is applied to a cathode follower that drives the capacitor input. When the input to the diode is -30 volts the output is approximately -30 volts, and the +55v pulse at the capacitor input is swamped out by the heavily conducting input diode. However, when the input to the diode is +10 volts, the diode is cut off because the plate is at about -12 volts. The 55v pulse now causes the output to swing from -12 volts up to ground.

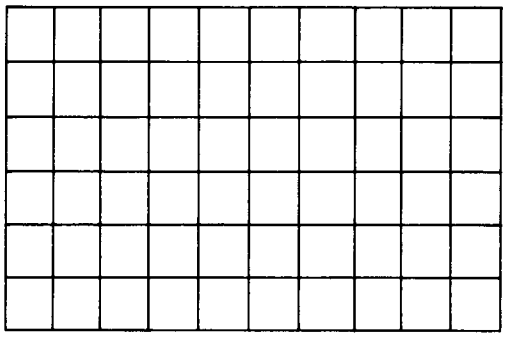
Figures A19b, A19c and A19d show typical wave forms. A steady +10 volts is at the diode input. Figure A19e shows the points where the wave forms are located. Point A is the junction point of the diode gate (A19a).

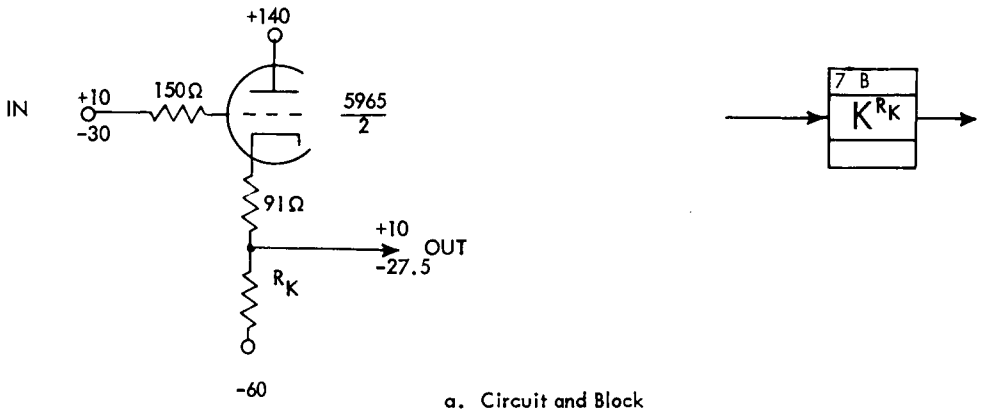
The ground clamp tends to prevent overdriving the trigger grid positive. The input diode to the trigger block isolates the negative shift of the input pulse. The value of the return resistor is 33K and is not shown in the logic block. As in other diode circuits, the upper section of the block contains the location of the junction point.



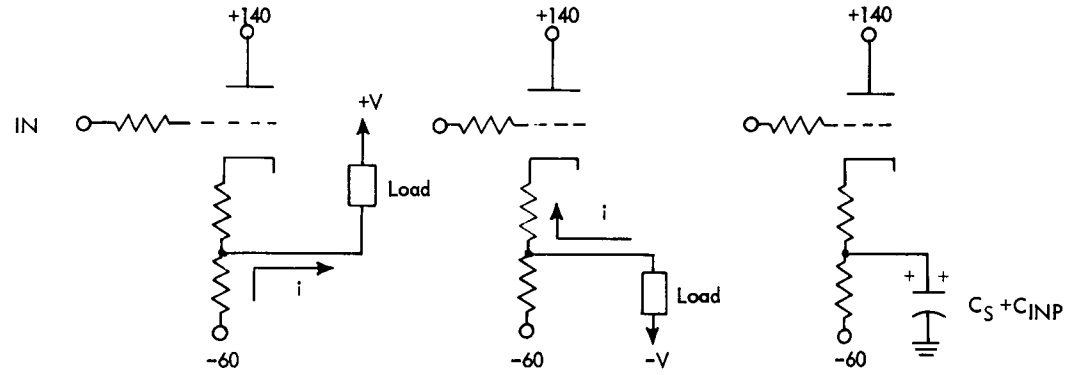




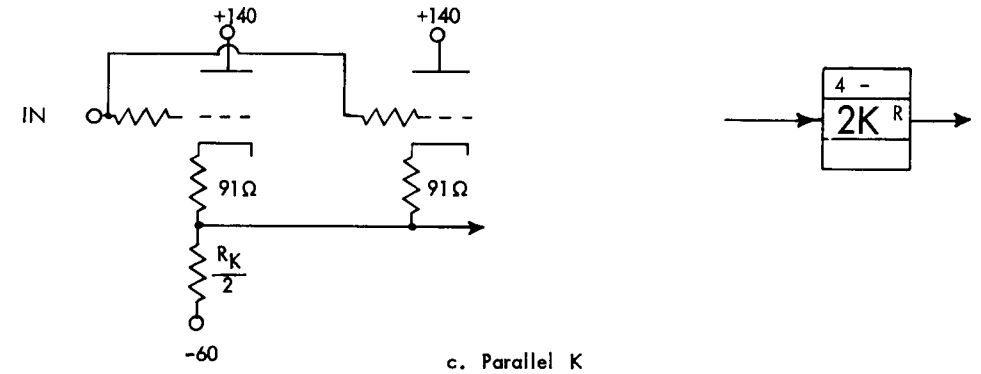




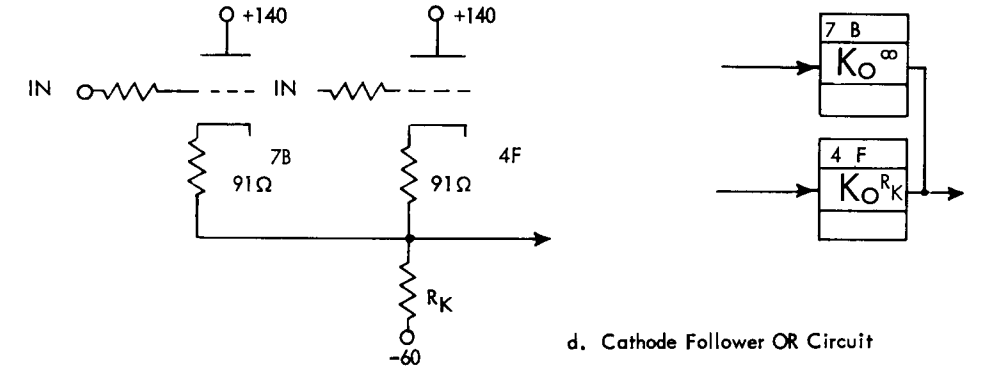
a. Circuit and Block



b. Loading Conditions



c. Parallel K



d. Cathode Follower OR Circuit

FIGURE A20. STANDARD CATHODE FOLLOWER

2.09.00 CATHODE FOLLOWER (K)

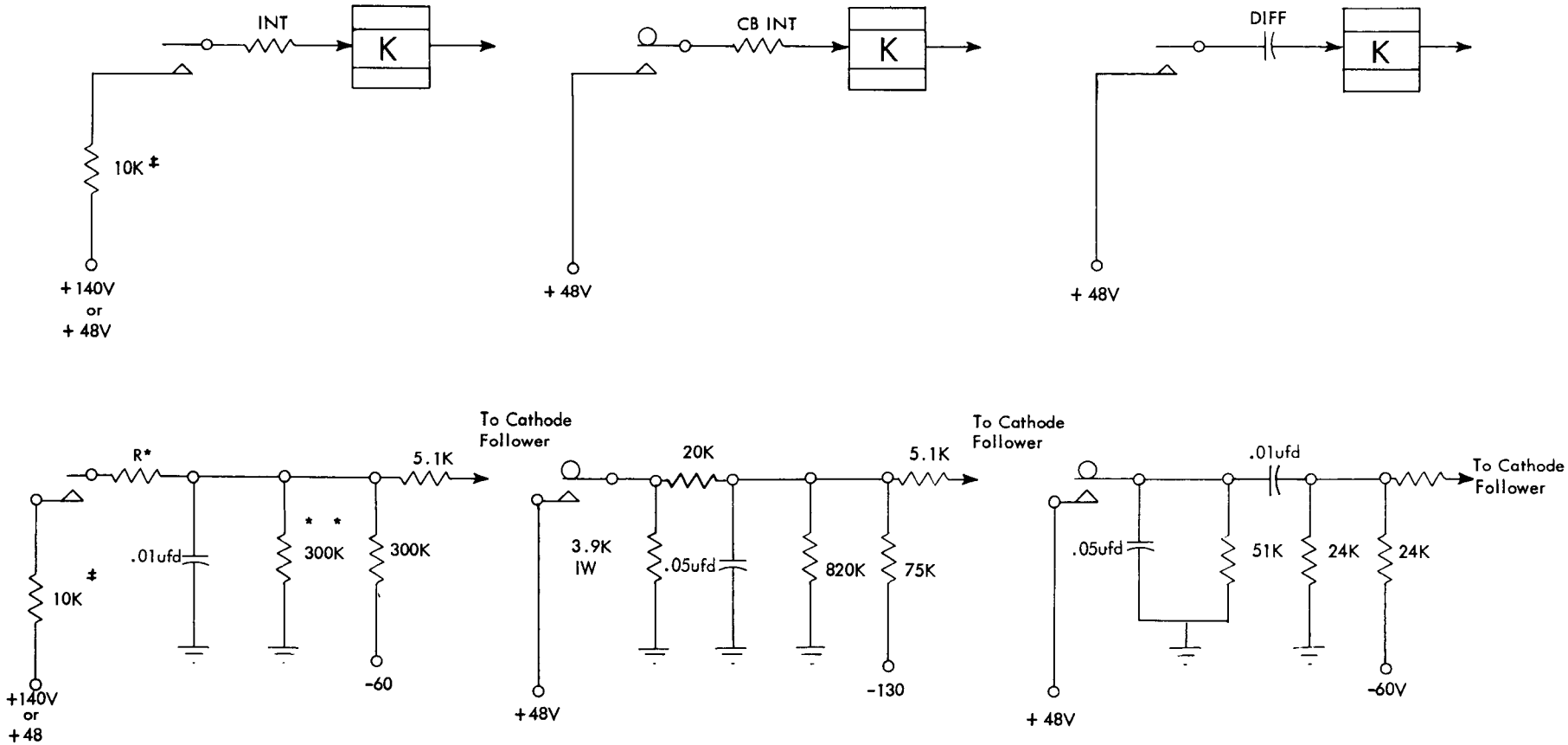
The basic powering circuit in the 700 series is the cathode follower K (Figure A20). Cathode followers have many characteristics that promote their wide use in calculators. They are primarily power amplifiers and, therefore, are used for supplying a stable voltage level for driving resistive loads such as diode AND-OR circuits or capacitive loads such as wiring capacitance. Their high input impedance and low output impedance make them useful for impedance matching and isolation. They do not invert a signal, but they do attenuate a signal.

2.09.01 Circuit Description

To understand thoroughly the natural actions of a cathode follower, the self-biasing characteristics of the circuit should be understood. The plate, with +140 volts, is always calling for more current. The controlling grid is calling for more current as long as the effective bias is positive, is neutral when the bias is zero, and completely resists the plate command when the effective bias reaches -3 volts (-30 volts on the grid). The grid takes control at -1v bias, when the input is +10 volts. The reason for the different stable points of bias voltage at the two different input levels is readily understood by noting the effective plate voltage in both cases. Because the effective plate voltage is only 129 volts with +10 volts on the grid, only one volt bias is needed. With an effective plate voltage of 167 volts (-30 volts on the grid), more bias (-3 volts) is needed to overcome the effect of the plate.

The tube conducts in such a manner as to tend to regulate itself, that is, not to allow an appreciable voltage change from grid to cathode. If the tube current increases, the tube tends to cut itself off as the cathode tends to rise. This cut-off action tends to decrease the current. If, on the other hand, the current tends to decrease, the cathode potential tends to fall, thus increasing the current flow. This type of self-regulation is called inverse voltage feed-back.

Current through the tube causes a voltage drop across the 91-ohm dropping resistor. With the input at +10 volts, this drop should about equal the grid-to-cathode rise, so that the output voltage is also +10 volts. If the input signal should drop to -30 volts, then the output voltage would also drop. Note from the tube characteristics that a change in current through the tube, which accompanies the change in voltage across the load, increases the negative grid bias to about three volts. With this bias and this current, the drop across the 91-ohm bias resistor changes from the one volt to about one-half volt. This means that the drop across the dropping resistor can no longer compensate for the grid-to-cathode rise, and the output will now be more positive than the input. The voltage rise in a cathode follower is about one tenth of a volt per volt change in signal level with the minimum cathode load in the circuit. As the cathode resistor is increased, the value of the lower level can be expected to increase also (about one volt per 3K increase in cathode resistor). The gain of a cathode follower operating class A is about 0.9.



* R = 130K for +48V input
R = 430K for +140V input

** 390K to give a -34V down level

‡ The 10K resistor may be removed when it is desired to pass more than 0.26ma through the contacts

INT, C.B. INT, or DIFF. may be used with K, K_X or K_P

FIGURE A21. CONTACT INTEGRATING AND DIFFERENTIATING INPUTS TO CATHODE FOLLOWERS

2.09.02 Positively Returned Resistive Load

If the cathode follower load is resistive and is returned to a positive voltage, the current for the load must be supplied from the -60v supply through the cathode resistor (Figure A20b). Because the tube regulates itself, this load current is taken away from the tube. As load current increases, tube current decreases. Design limits the minimum current through the tube to 1.5 ma. Therefore, a single cathode follower (5965 tube) can supply 10.5 ma without materially affecting voltage level (low impedance output).

2.09.03 Negatively Returned Resistive Load

A load that is returned to a minus supply voltage is effectively paralleled with R_K (Figure A20b). Therefore, any current demands of the load must be met by the tube. A value of R_K is chosen so that, in parallel with the load, the total impedance is such that both currents together will not exceed 12 ma.

2.09.04 Capacitive Load

Let the loading become capacitive and the situation changes somewhat (Figure A20b). Assume that a capacitance is connected from the output to ground. If the grid now shifts from +10 volts to -30 volts, what are the conditions? Because the voltage across the capacitance cannot change suddenly, the cathode is held at +10 volts while the grid shifts to -30 volts. The tube is cut off for a time. The output voltage drops at a rate determined by the RC path of the capacitance and the load resistor. After the voltage has dropped far enough, the tube starts to conduct again. When the input again shifts to +10 volts the capacitance is charged by the current through the tube. Usually the input capacitance from succeeding stages is such that the RC time constants encountered are comparable to rise and fall time of the input. Therefore, the extremes of cut-off and very heavy conduction to charge the capacitance are not encountered, and the output follows the input. If the RC time constant is such as to cause the above mentioned extremes, the output does not follow the input but depends on the RC time constant. This condition appears as output distortion.

2.09.05 Parallel Cathode Follower

The use of more than one cathode follower in parallel helps to minimize the voltage rise of the down level through the circuit with a given load. Paralleling the cathode followers also provides more current for the line charging purposes to speed output voltage shifts. In addition, the paralleling lowers the effective cathode resistance, allowing faster discharging of line capacitance. Each tube can use one R_K or the value of R_K can be divided by the number of tubes paralleled. When cathode followers are paralleled, the connections are made at the grid parasitics and the output (Figure A20c). The number of half tubes in parallel precedes the symbol K in the block diagram, thus a whole tube cathode follower is symbolized by 2K. Parallel cathode followers are more susceptible to parasitic oscillation than are most of the other circuits or unparalleled cathode followers.

2.09.06 Cathode Follower OR Circuit

Frequent use is made of a cathode follower to act in the same manner as a diode input to an OR circuit. Two or more cathode followers are tied together as shown in Figure A20d. Because they each use the same return resistor, any input rising to +10 volts causes the output to come up (OR circuit operation). The components of a diode OR circuit and a separate cathode follower are saved by this method because all input lines to the diode OR circuit would need powering. The block notations of a cathode follower OR circuit are K_O or K with infinity signs (∞) in all blocks but one.

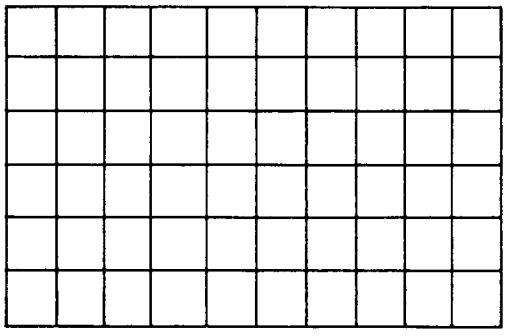
2.09.07 Cathode Follower Inputs

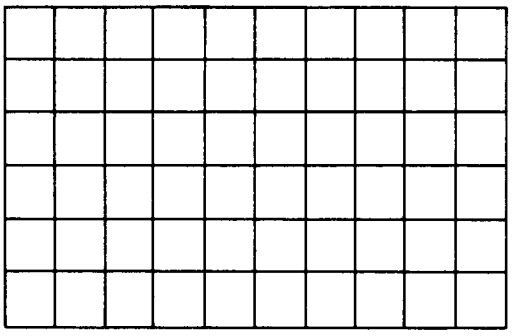
Figure A21 shows several special input circuits and their logic block notations. Special integrated and differentiated inputs are used whenever mechanical devices such as relays or circuit breakers are used to control voltage levels or activate circuits.

2.09.08 Summary

The following points summarize the operation of the standard cathode follower:

1. Power amplifier
2. No inversion
3. High-input, low output impedance
4. Self regulation (inverse voltage feedback)
5. Attenuation--gain about 0.9
6. Class A operation (normally)
7. Rise in down level
8. R_K set to not exceed current limitations of tube and set fall time of capacitive load





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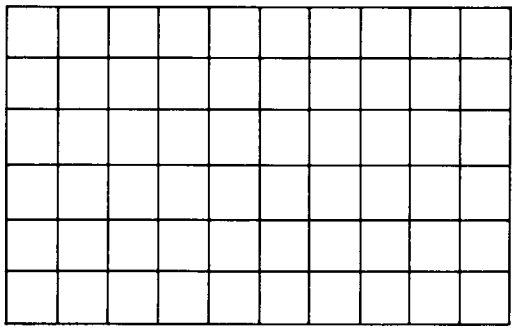
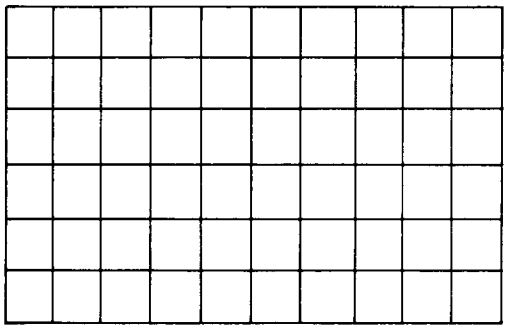
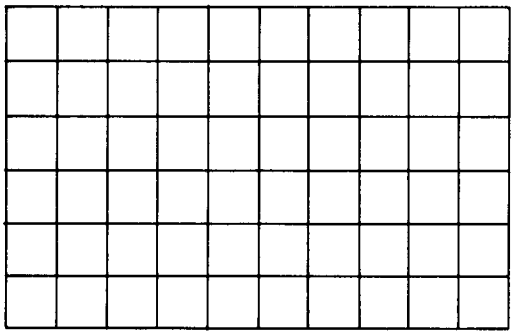
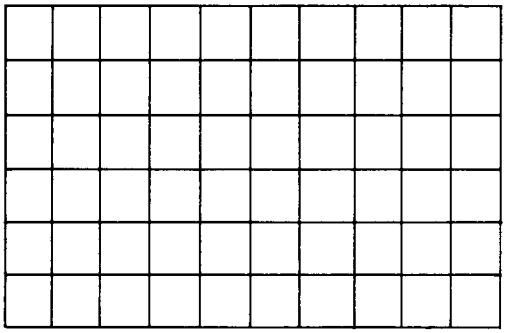
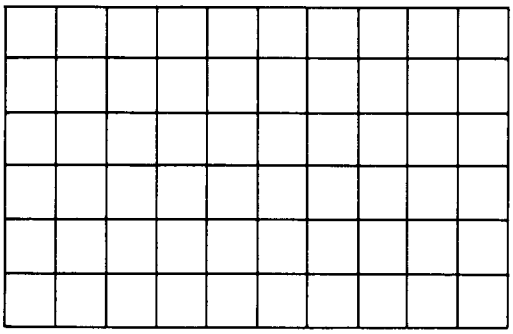
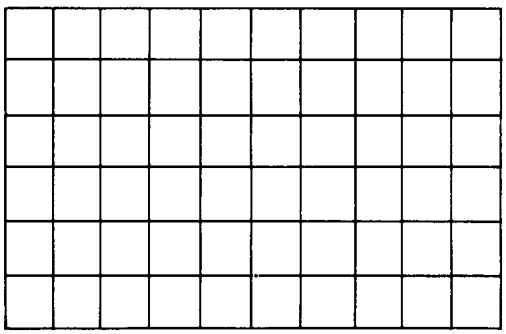


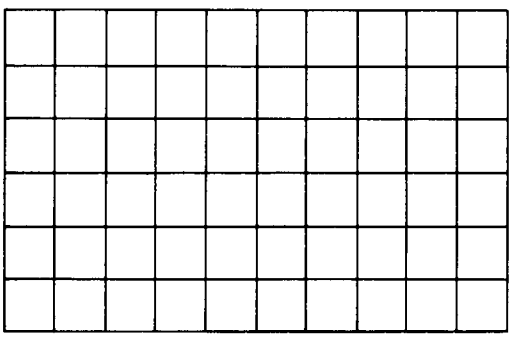


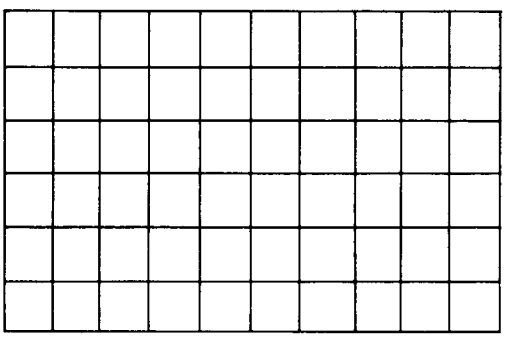


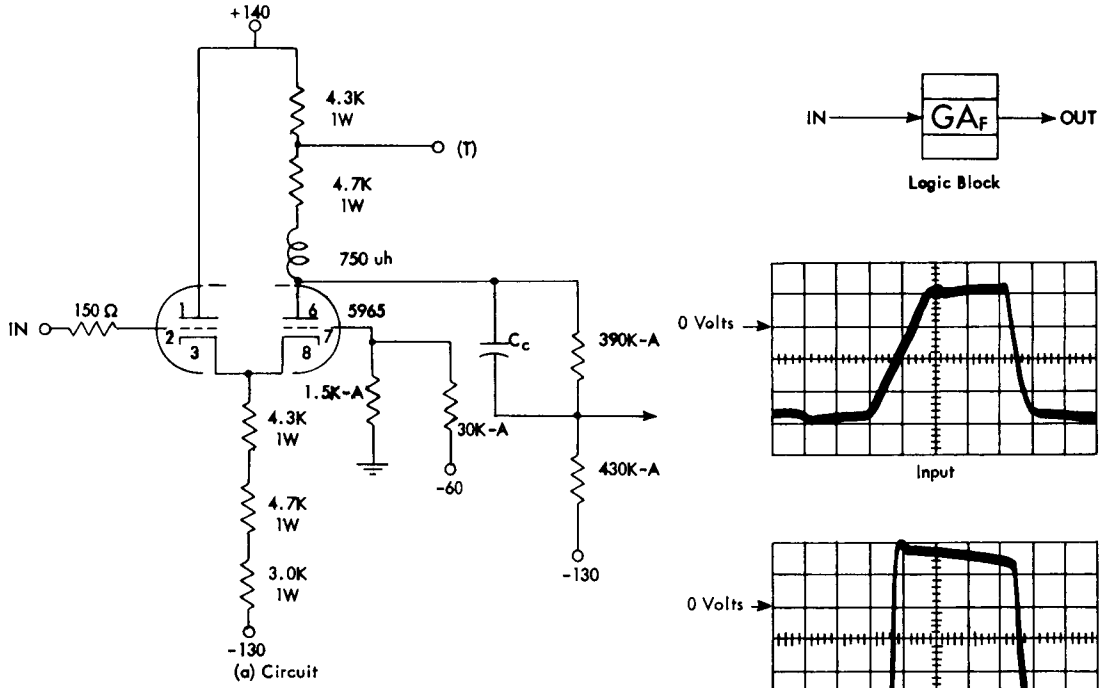


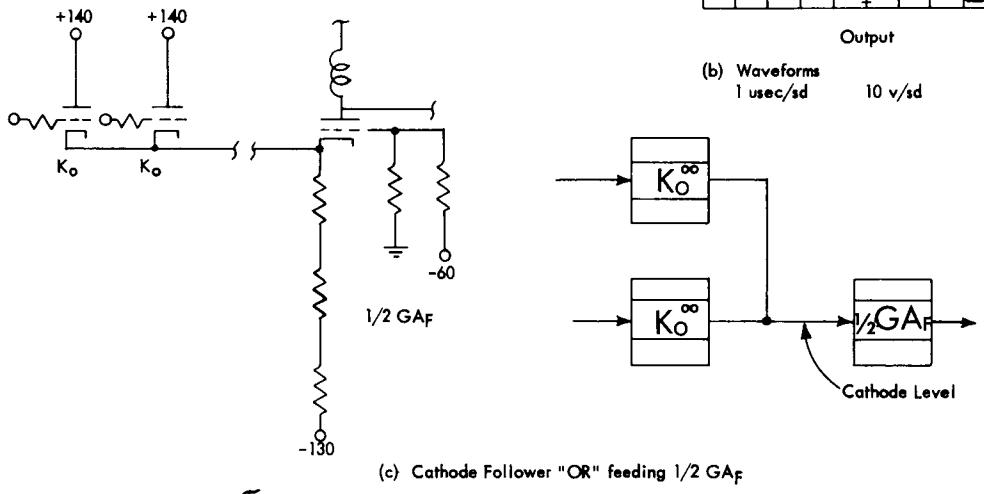












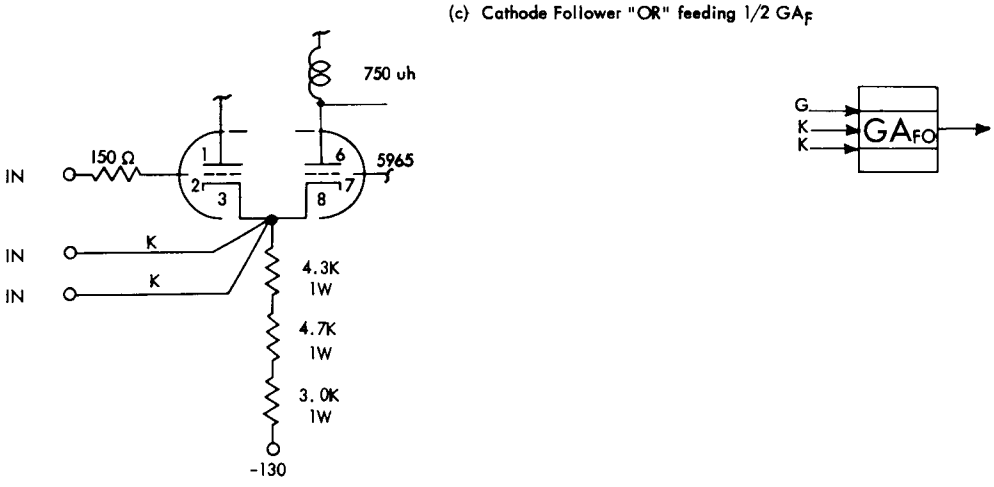


FIGURE A22. GROUNDED GRID AMPLIFIER (FULL PLATE) GA_F

2.10.00 GROUNDED-GRID AMPLIFIER (GA_F)

The grounded-grid amplifier GA_F, shown in Figure A22a, is used as a level setter and pulse shaper. As pulses pass through the machine, their shape and voltage levels deteriorate. The GA_F is used to reshape the pulse and feed it to cathode followers. The special down level of -38 volts permits normal cathode follower down level loss without affecting minimum down level requirements. The GA_F does not invert the signal.

2.10.01 Circuit Description

The grid of the right tube is held at approximately -3 volts by the voltage divider network between -60 volts and ground. With -30 volts on the left grid, the right tube is conducting approximately 10.5 ma, the cathode is -2.5 volts, and the right plate is at +45 volts, resulting in -38 volts at the divider output. The left tube is cut off.

As the input signal rises, the left tube starts to conduct with approximately -10 volts on its grid. More current flows through the cathode resistors and the voltage at the cathode rises. Because the grid bias is fixed at -3 volts, the rising cathode voltage causes the right tube to begin cut-off action and its plate voltage rises toward +140 volts. The tube characteristics are such that when the input voltage reaches +3 volts, the cathode is at +3.5 volts and the right tube is cut off. The divider output is now +10 volts. Any further rise of the input causes the left tube to conduct harder and the cathode voltage rises as in a cathode follower. Because the right tube is cut off, the rising cathode voltage has no effect on the right tube or the output voltage.

As the input drops, the previous action is reversed. The right tube starts to conduct when the input is at +3 volts and is in full conduction when the input falls to -10 volts. The divider output returns to -38 volts. There is about a 4-to-1 speed-up in rise time and about a 10-to-1 speed-up in fall time. The reason for the difference in speed-up of the rise and fall time is the shape of the portion of the input signal that is being used. The leading edge of the input signal is usually sloped much more in the used portion than the trailing edge. Figure A22b shows a typical input to a GA_F and the resultant shaped and level-set output. Minimum input voltage requirements are +5 to -20 volts. The tapped plate output levels are +138 volts to +94 volts nominal.

There is a special case in the arithmetic circuits in CPU where a GA_F is used to reset a voltage level before impulsing a trigger. Noise on the incoming pulse was found to pass through the GA_F and erroneously to set the trigger. A 68-uuf capacitor has been added from GA_F plate to ground. The addition of this special capacitor is shown outside the GA_F logic block.

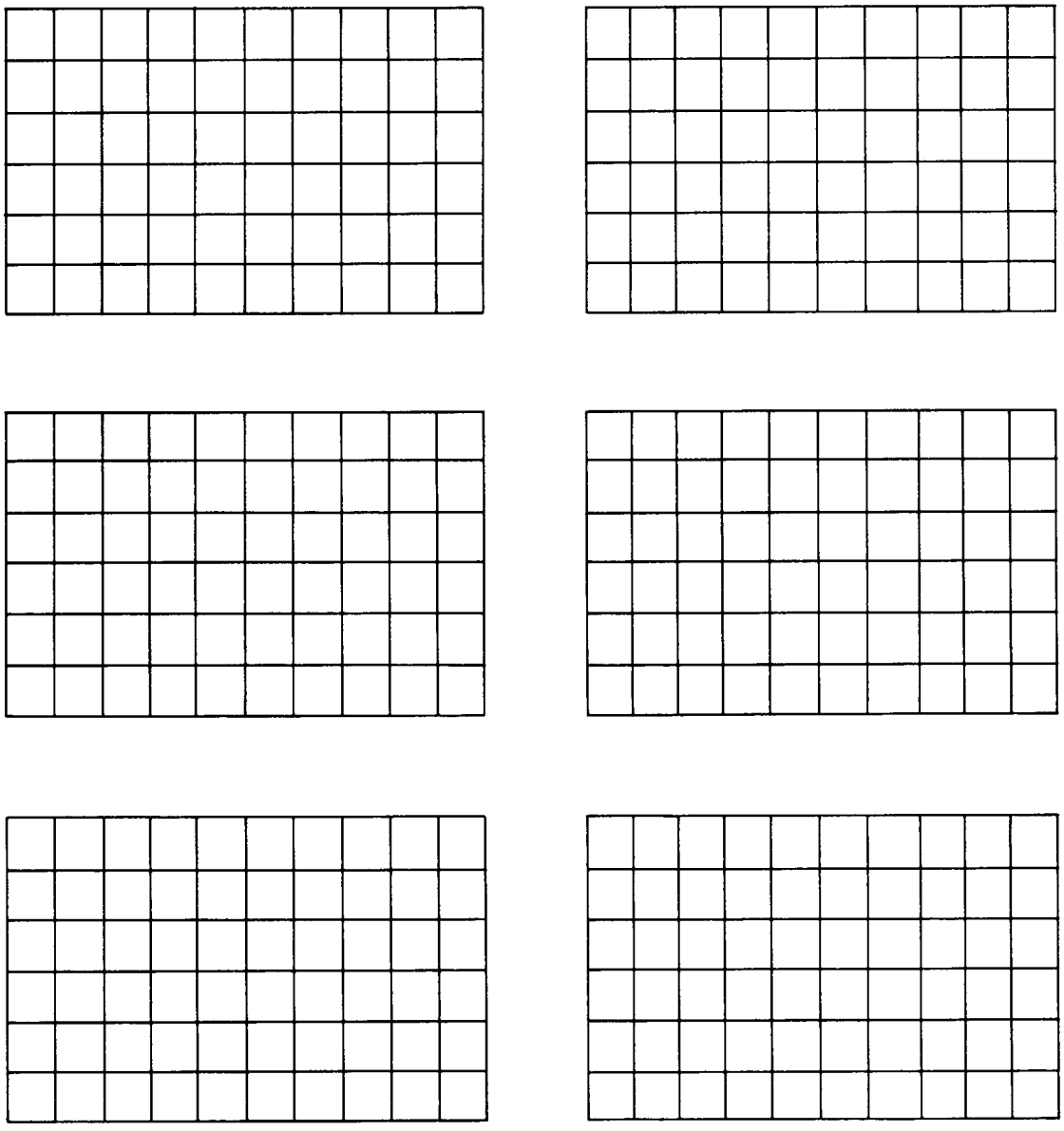
2.10.02 Variation--1/2 GA_F

Sometimes the output of a cathode follower OR circuit needs to be shaped and level set. One-half tube can be saved by feeding the OR output directly to the cathode of the right tube and deleting the left tube. The rising input to any cathode follower in the OR configuration operates the right tube in the same manner as the GA_F. The

$1/2\,GA_F$ block uses one-half of a 5965 and the input is at cathode level. All K_O blocks have infinity signs denoting that they are sharing the cathode circuit of the $1/2\,GA_F$ (Figure A22c).

2.10.03 Variation (GA_{FO})

The GA_{FO} is a GA_F with multiple inputs (Figure 22d). One input is the normal grid input and one or more inputs are tied to the cathode. Therefore, any of the inputs can control the output. The inputs are labeled G for grid and K for cathode to denote their levels.



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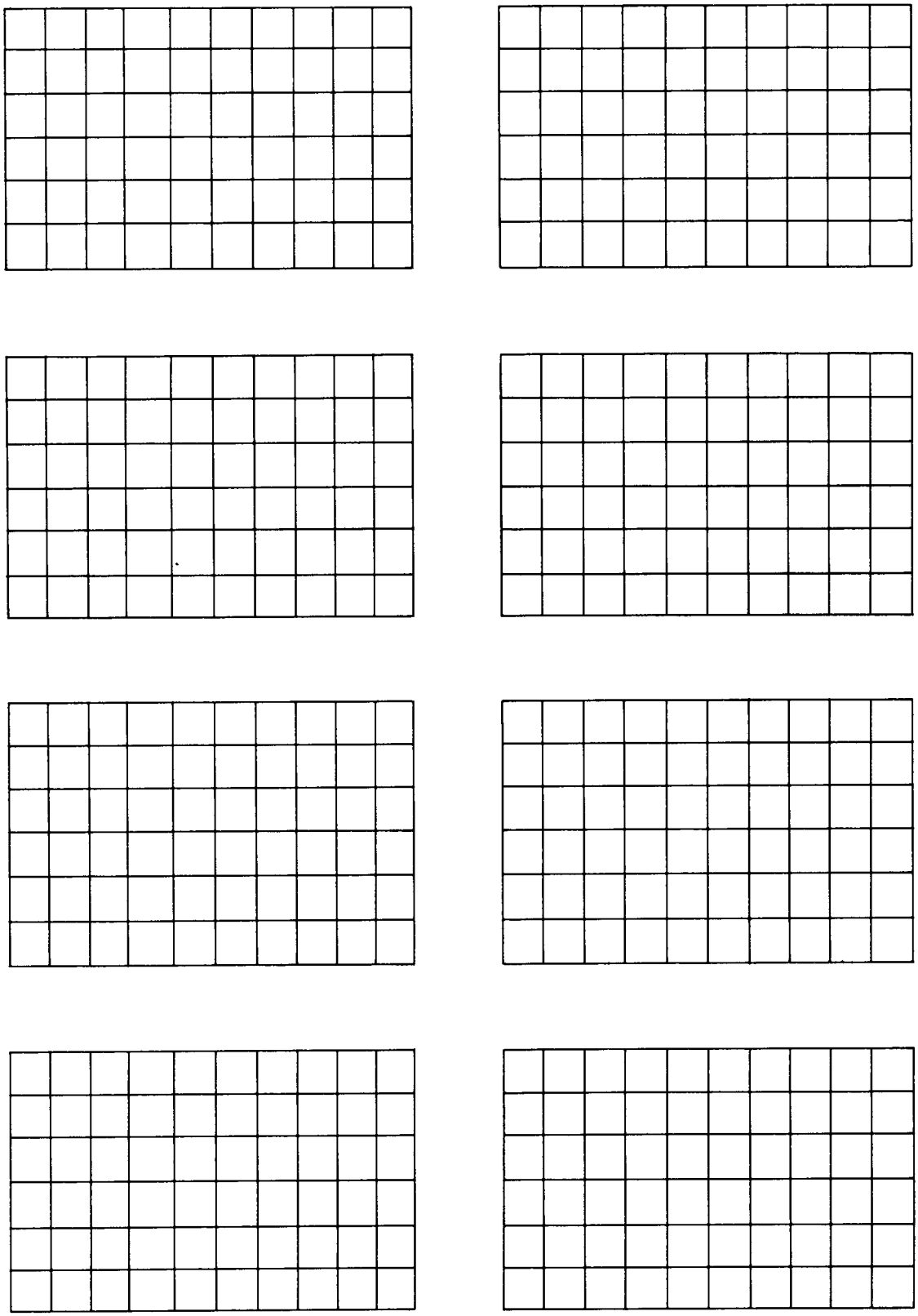
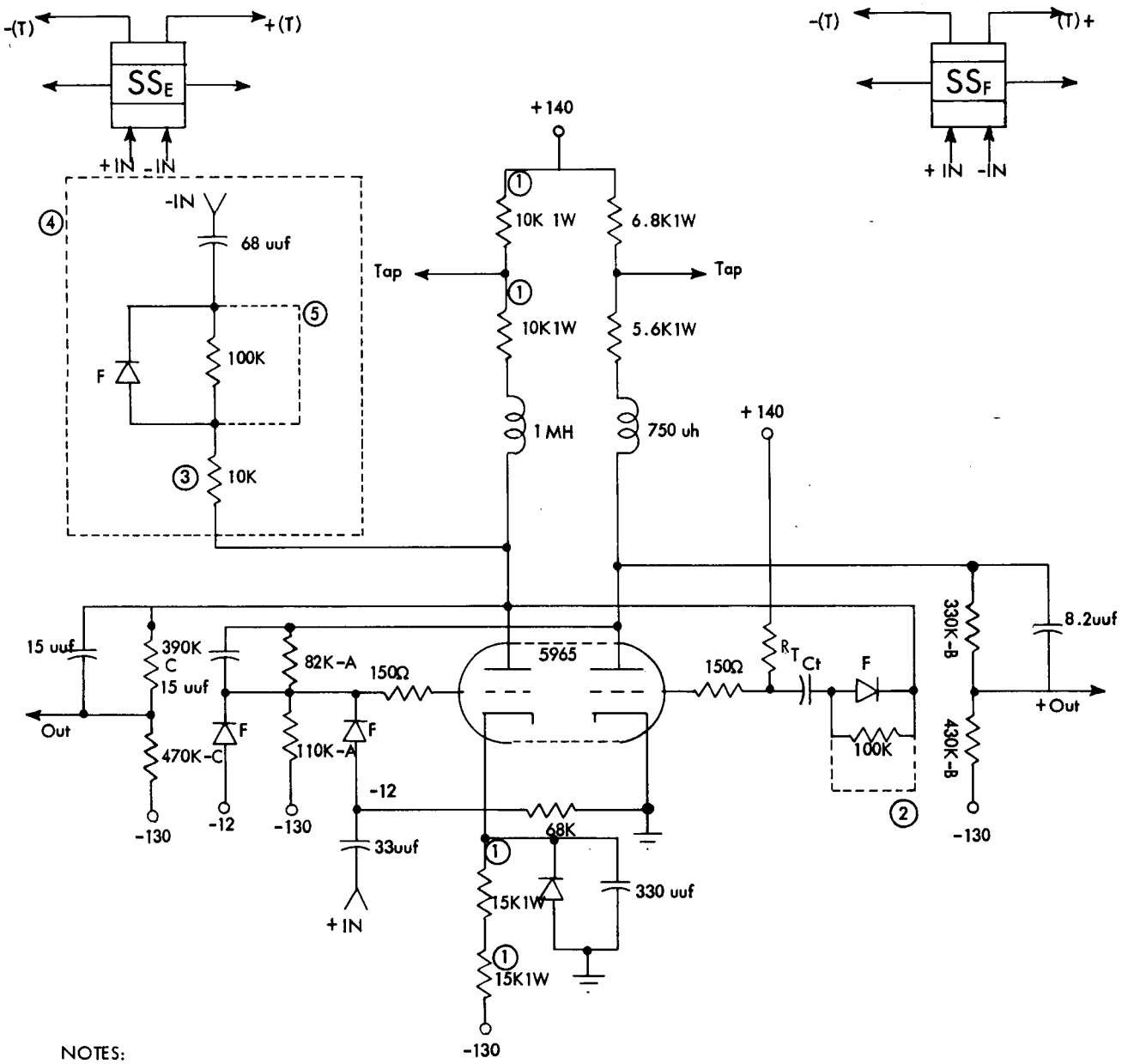




NOTES:

1. The left plate and cathode resistors are to be 1% precision type for accurate timing.
2. For SS_E, replace F diode and 100K with short circuit.
3. For timing equal to or less than 10 usec, replace the 10K in the negative shift input with a short circuit.
4. Negative shift input for SS_E only.
5. For SS_F, replace F diode and 100K with short circuit.
   R_T will also be a precision resistor in critical timing applications.

FIGURE A23. SINGLE SHOTS SS_E AND SS_F

2.11.00 SINGLE SHOT (SS_E)

A basic monostable multivibrator is the single shot, SS_E. It currently replaces the standard single shot SS, and, therefore, is covered in this section. This circuit is used to generate gates or pulses of specified duration and to provide delays. A single shot resembles a trigger circuit in that it may be flipped into a certain state. But it then returns to its previous state after a predetermined time without being impulsed from an external source. After being impulsed, the circuit turns on and stays on until the predetermined time has elapsed. The circuit then returns to its off or quiescent state.

2.11.01 Circuit Description (Figure A23)

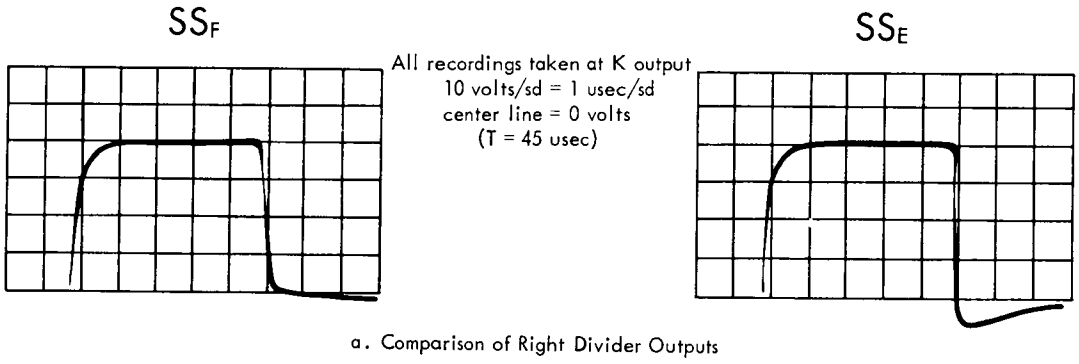
In its quiescent state, the right tube conducts about eight milliamperes with the right grid at about zero volts and the right plate down to about +35 volts. Because of the same type of cross-coupling as is in the trigger, the left grid is held down and clamped at -12 volts. The left tube is cut off and its plate is up near +140 volts and its cathode is at ground level because of the ground clamp diode. The cathode can rise above ground level but it cannot fall below this point.

Assume a 40v negative shift being applied to the input capacitor. The shift couples through the 68 uuf capacitor, through the negative facing diode and is impressed on the left plate. It is coupled on through the timing capacitor C to the right grid, dropping the grid to about -40 volts and solidly cutting the right tube off. Because the voltage across a capacitor cannot change instantaneously, the plate side of the timing capacitor is now at about +100 volts with the grid side at about -40 volts. The regenerative action of the circuit now starts. As the right tube begins to cut off, the right plate rises. This rise is coupled back to the left grid, bringing the left tube into conduction. As the left tube starts to conduct, the left plate voltage drops to +53 volts. This voltage drop aids the original negative shift, reducing the grid another 47 volts (100-53). When the left side is in full conduction (about 4.5 ma), the circuit has the following voltage status:

Left plate	+53 volts
grid	+10 volts
cathode	+10 volts
Right plate	+118 volts
grid	-87 volts

With the right grid driven down to -87 volts, the timing capacitor C_T still has a potential of 140 volts across it.

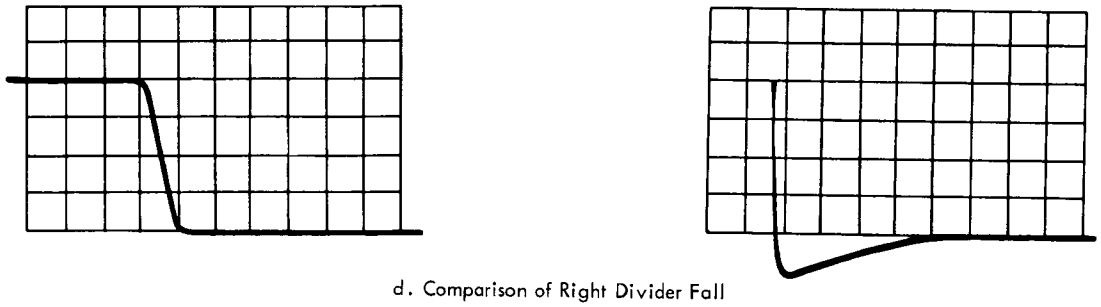
As the left tube reaches its steady state of conduction, the voltage shift affecting the right grid stops and the timing-out action of the single shot starts. The right side of C_T is held at +53 volts by the left plate voltage. C_T starts to discharge and the right grid rises toward +140 volts through R_T. The right grid voltage rises exponentially until it reaches -6.5 volts, the cut-off point of a 5965. Because the grid has to rise 80.5 volts to reach cut-off, the rise represents only 35 percent of the possible potential change (to +140 volts is maximum). Referring to the universal time constant curve (Figure E4), note that 35 percent of the total possible change is accomplished in 45 percent of the time constant. The time of this single shot is equal to $0.45\ C_T\ R_T$.



a. Comparison of Right Divider Outputs

b. Comparison of Left Divider Outputs

c. Comparison of Left Divider Rise



d. Comparison of Right Divider Fall

FIGURE A24. OUTPUT WAVE FORMS SS_F AND SS_E

As the right grid reaches -6.5 volts, the right tube starts to conduct and the regenerative action takes place to cut off the left tube. The right tube, going into conduction, lowers its plate voltage and this shift is fed back to the left tube to cut it off. Cutting off the left tube allows its plate to rise slightly and this rise is coupled through C_T to the right grid, bringing the grid up to zero volts where it is held by grid current flowing through R_T. The regenerative action is complete and the single shot has "timed out."

2.11.02 Recovery Time

At the completion of the regenerative action, C_T has zero volts on the grid side and +59.5 volts on the plate side. Before the single shot can be used again, the circuit must be restored to its quiescent state with a charge of 140 volts across C_T. The charging or recovery time is now determined by the R/C network of C_T and the two 10K resistors in the left plate circuit. The voltage on the left plate is held back for the time necessary to charge C_T. This recovery time is about 5 percent of the timing-out time.

2.11.03 Timing Accuracy

The left tube circuit contains precision cathode resistors that provide degeneration or self-biasing characteristics. Effect on the circuit by variations in tube characteristics is held to a minimum. The capacitor in the left cathode circuit momentarily keeps the left cathode positive as the left grid is being pushed down at the end of the timing cycle. The cathode tends to follow the grid down; it would take longer to cut off the left side.

With a variation of 10 percent while biasing the +140v and -130v supplies, the timing does not vary more than +4 percent to -6 percent.

2.11.04 Inputs

The circuit description mentions the negative shift input. The single shot can also be impulsed by a positive input (Figure A23). The input is tied directly to the left grid with a diode to block negative shifts. The positive shift forces the left tube into conduction and the regenerative action takes place as before. The inputs to the single shot show their polarity by their position on the logic block. The positive input is placed on the left side and the negative input is placed on the right.

Both inputs require a 25v minimum shift at 60 volts/usec and an input pulse width of at least two usec. A noise pulse of 14v sharp rise triggers the single shot through the positive input while a noise pulse of 11v sharp fall triggers the single shot through the negative input. The 10K resistor in the input circuit is removed for timings of 10 usec or less.

2.11.05 Outputs

The various nominal output levels and rise/fall times are as follows:

Output	Voltage Level	Rise/Fall
Right divider	+10, -33	0.2/0.35 usec
Tapped right plate	+130, +86	same
Left divider	+14, -34	*/0.2 usec
Tapped left plate	+137, +92	same

* A function of C_T and left plate load.

The delay in the rise of the left plate is caused by the exponential charging of C_T during recovery time. See typical output wave forms in Figure A24.

2.11.06 Miscellaneous

The Systems page shows near the SS_E logic block the value of C_T, the value of R_T, and the timing or duration of the single shot. R_T can be varied from 130K to 1.0 megohms. C_T can be varied from 100 uuf upward. It is unwise to use a single shot for timings below 3.5 usec. All resistors in the left plate and cathode circuits are precision resistors for timing accuracy. R_T is also a precision resistor in critical timing applications.

2.11.07 Variation (SS_F)

The SS_F is one design variation of the single shot. The SS_F is used when a fast left divider output pulse is required. During restoration the SS_E has a left plate voltage that is slowly rising because C_T is charging.

The only circuit change in the SS_F is the location of the diode and 100K resistor. They are moved from the input circuit to the plate side of C_T (Figure A20). The addition of these components between C_T and the left plate releases the plate from C_T during recovery time. As the left side of the tube cuts off after timing out, the left plate is free to rise rapidly. Because the 100K resistor and C_T represent a divider circuit to the plate, the voltage at the plate does not rise to +140 volts but to a value slightly lower. The transition is not as far as the SS_E but it is faster.

By adding the 100K resistor in the charge path of C_T, the recovery time of the SS_F is longer than the SS_E. Recovery time for this circuit is about 40 percent of the single shot duration.

2.11.08 Outputs (SS_F)

The output levels are the same as the SS_E. However, the rise/fall times are changed as follows:

Output	Rise/Fall
Right divider and plate	0.2/0.6 usec
Left divider and plate	0.7/0.2 usec

In all other respects, the SS_E and the SS_F are the same.

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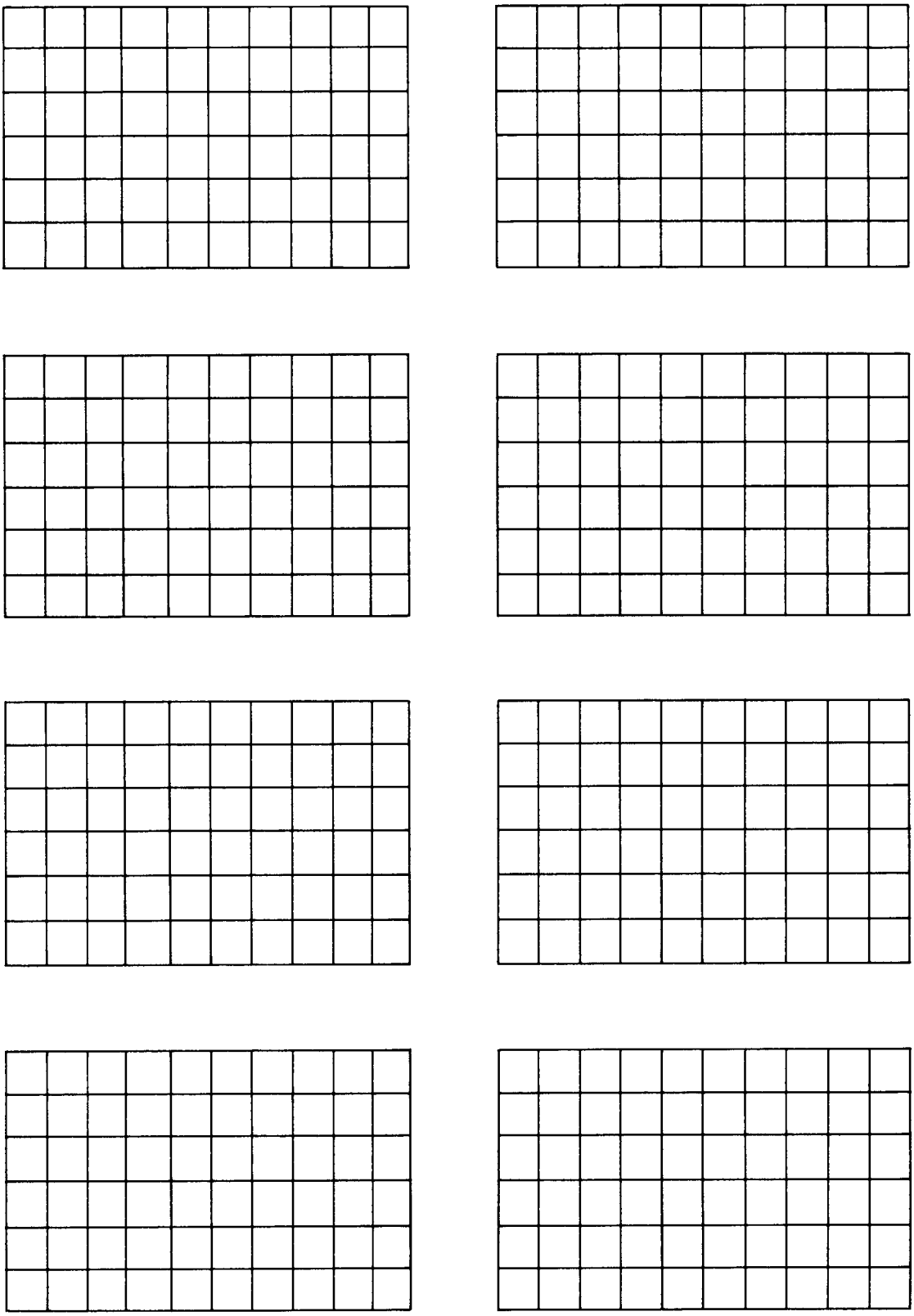

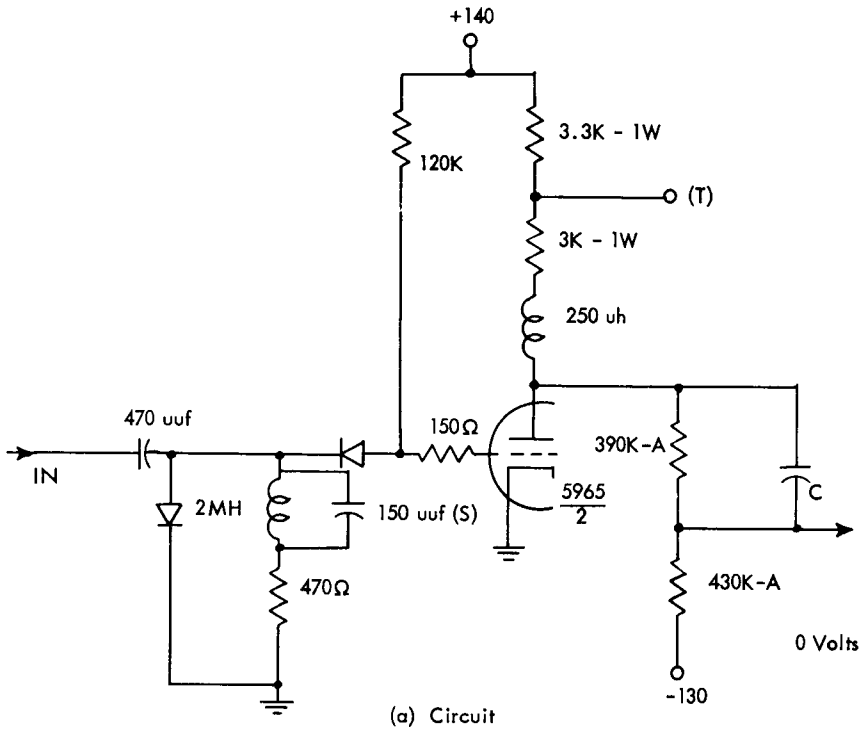

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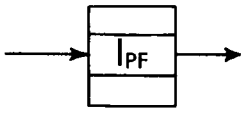
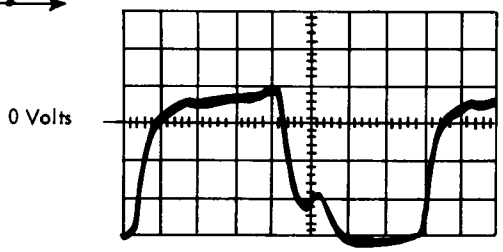
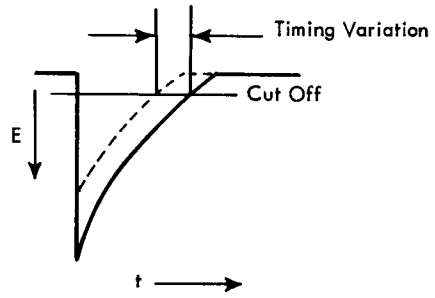


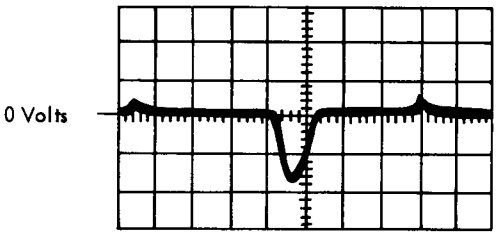
Logic Block



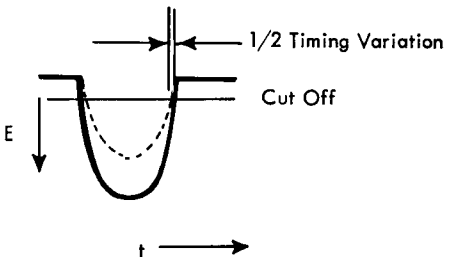
Input



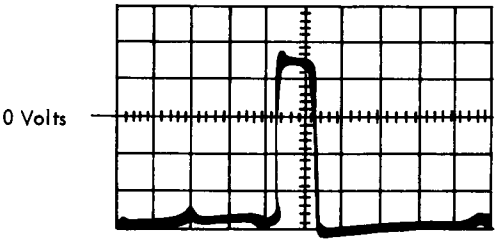
(b) RC Timing and Variations



Grid



(c) LC Timing and Variations



Divider Out

(d) Waveforms
2 usec/sd 10 v/sd

FIGURE A25. PULSE FORMING INVERTER (t_{PF})

2.12.00 PULSE FORMING INVERTER (I_{PF})

The pulse-forming inverter I_{PF} (Figure A25a) generates pulses at various points in the system. The input to the I_{PF} is a negative transition with an amplitude of 25 to 50 volts, and a fall time greater than 60 volts/usec to the driving cathode follower. (A standard cathode follower always drives an I_{PF}.) No change is allowed in the input wave form until four usec after the negative transition, to allow the circuit to time out normally. The divider output of the I_{PF} is a nominal +10v to -31v pulse with a rise time of 0.15 usec and a fall time of 0.40 usec (0.15/0.4). The nominal pulse width is two usec at 50 percent amplitude.

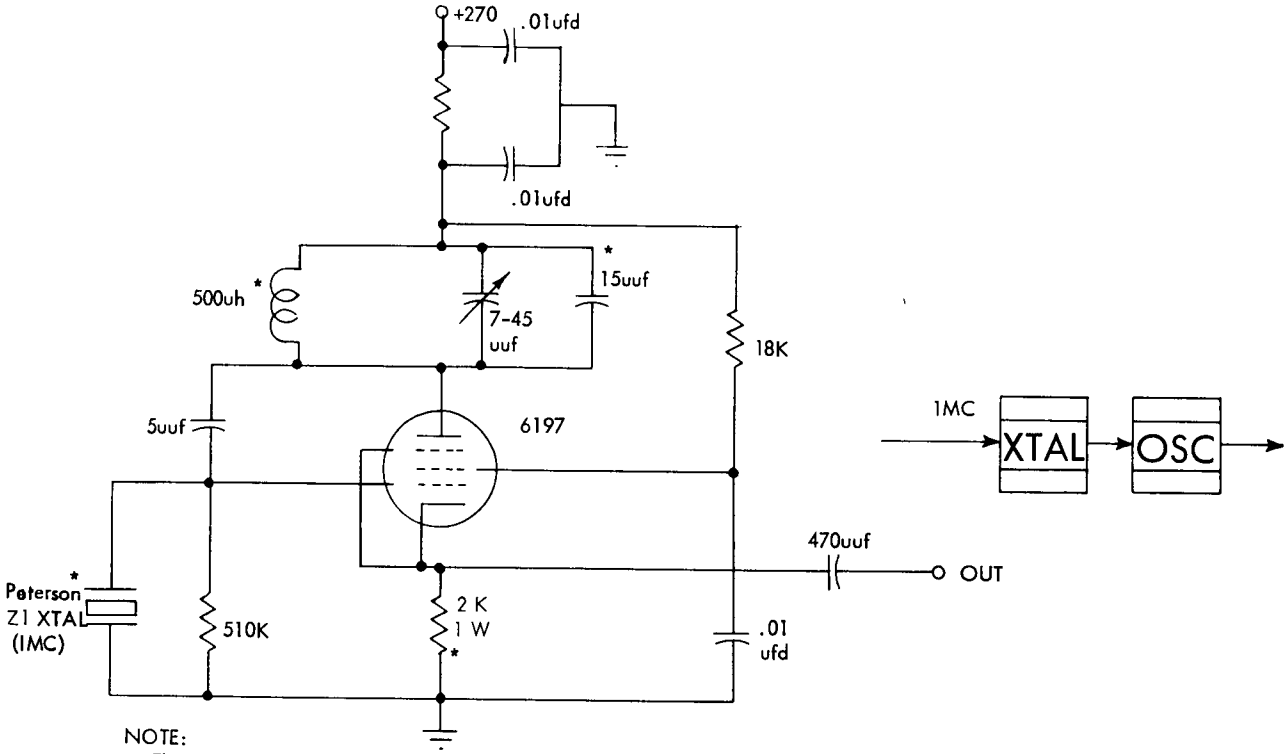
2.12.01 Circuit Description

In its quiescent state, the tube conducts about 12.5 ma with the grid drawing about 0.02 ma. Positive shifts at the input are clamped by the diode to ground and blocked by the diode to the 150-ohm grid resistor. The divider output is about -30 volts. The negative shift supplies the current to charge the tank circuit and to lower the grid voltage. The current flowing into the tank charges C and magnetic energy is stored in L. (See "LC Tank Circuits," section 1.01.04, Book E.) Near the bottom of the falling input pulse, the slope of the pulse decreases. This decreased slope causes a change in charging current to the tank. Inductor L tries to resist the current change by giving up its magnetic energy (collapsing flux lines), tending to keep the current flowing. The collapsing field starts the tank circuit oscillating even before the input shift is complete. (See input wave form for reflection effect from tank.) When the grid goes negative, the tube is rapidly cut off and the divider output swings up to about +12 volts with some overshoot caused by the coil in the plate circuit. The output pulse width is determined largely by the natural period of the LC tank circuit in the grid with the input capacity and the circuit resistance tending to increase this width ($t = 2\pi\sqrt{LC}$). The input tank tends to ring but the positive half cycle is dissipated by the ground clamp diode. The 120K resistor from the grid to +140 volts speeds up the swing back of the grid to ground level after the negative transition. The 470-ohm resistor keeps DC current out of the tank circuit and routes it through the diodes to +140 volts.

The wave forms show the input pulse, the voltage at the grid and the divider output. Note that the upward transition of the tank circuit is reflected back to the input. For this reason, the driving cathode follower does not feed any other circuit. The input must stay down until the tank has completed its timing cycle.

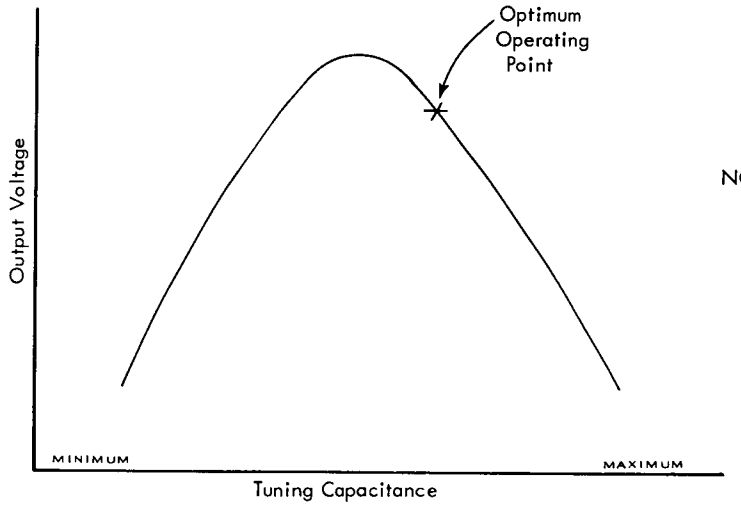
2.12.02 I_{PF} Timing

There are definite reasons why an LC tank circuit is used instead of RC timing as found in the single shot. The I_{PF} is used to generate a relatively accurate timed pulse. The circuit should not be affected by variations in the input shift. Figure A25b shows the timing variation that can be encountered if an RC input circuit is used. The input shift varying 10 volts has a material affect on the time that the grid is held below cut-off. Figure A25c shows that a tank circuit, whose time or frequency is largely a function of L and C, does not produce as large a timing variation as did the RC circuit. The grid voltage also moves through the cut-off point at a faster rate, producing a faster falling voltage at the plate.



NOTE:
This same circuit is used with a 476KC cyrstal, a 1MH choke, a 68 uuf capacitor and a 1.8K-1W load resistor. Refer to section 2.08.02, Book B. The circuit is also used with a 2MC crystal, a 7-35 uuf timing capacitor, a 100 uh choke and no decoupling to the +270 volt supply.

FIGURE A26. OSCILLATOR (CLOCK) -OSC



NOTE:
Some oscillators may have two peaks, one smaller than the other. The smaller will be on the maximum capacity side of the largest peak. Tune to the higher peaks maximum capacity side.

FIGURE A27. GENERAL OSCILLATOR TUNING CHARACTERISTIC CURVE

2.13.00 OSCILLATOR (CLOCK OSC)

The oscillator (Figure A26) used in the clock drive is a crystal-controlled modified electron-coupled oscillator. Feedback in this type of circuit is usually accomplished by the interelectrode plate-to-grid capacitance. However, to insure circuit stability, a small plate-to-grid capacitor has been added. A quartz crystal with properties enabling it to vibrate at a specific frequency (one megacycle is shown) is used in the grid circuit to control tube conduction. An adjustable tank ciruit feeds the swinging plate voltage back to the grid, to re-energize the crystal.

2.13.01 Circuit Description

When power initially comes up, the tube starts conducting because there is no negative bias to prevent conduction The initial surge of current is enough to lower the plate voltage and, through the feedback capacitor, to shock the crystal. The negative transition of the crystal (acting as a tank circuit) cuts off the tube and the plate current falls. The falling plate current produces a positive voltage transition in the plate tank circuit. Thus, the phase of the sine wave voltage produced by the crystal and that of the tuned tank circuit are naturally 180^{o} apart.

If the alternating voltage at the plate were exactly 180^{o} out of phase with the grid voltage, the feedback would be degenerative and the oscillations would not continue. The tank circuit is, therefore, detuned slightly to produce a regenerative feedback action. The variable capacitor is adjusted until maximum output at the cathode is obtained. The response curve (Figure A27) of the circuit shows the optimum operating point. The tuning capacitor should be adjusted so that a slight amount of capacitance is added beyond the peak. This procedure insures maximum stability for the circuit (dependable starting with power on, operation while biasing, and minimum effect of stray capacitance of oscilloscope probes).

The grid wave form is a nominal 440v peak-to-peak sine wave. The plate wave form is a slightly distorted sine wave with an amplitude of about 500 volts, peak-to-peak. The cathode wave form is a positive peak, about 80 volts in amplitude. The negative portions are clipped as the tube is cut off. The cathode voltage drops slightly even after the tube is cut off. This drop is caused by the interelectrode capacitive coupling between grid and cathode. The output of the oscillator consists of positive-going pulses of 0-80 volts occurring once each microsecond. The magnitude of the feedback voltage in combination with the cathode bias is such that the tube is overdriven. The result is that the output is not a pure sine wave, but is distorted on the positive excursion and clipped by the cut-off action of the tube (negative excursion). The output is taken from the 2K cathode resistor which serves both as bias and as part of the load for the circuit.

This oscillator uses a pentode tube (a common practice with high frequency oscillators) with the suppressor grid tied to the cathode. The suppressor performs the screening action in a pentode as well as the suppression of secondary emission. The screen grid is tied to +270 volts through an 18K dropping resistor and is also coupled to ground through a 0.01-ufd capacitor. (This helps maintain a steady voltage level on the screen.) In this circuit, the screen grid accelerates the electrons through the tube. Without the screen's accelerating action relatively few electrons would penetrate the space charge and reach the plate. The 510K resistor from grid to ground serves as a DC path for the grid. The decoupling in the plate circuit keeps noise out of the power supply.

2.14.00 THYRATRON CIRCUITS

All thyratron circuits to date use the 2D21, a heated cathode, Xenon-filled, tetrode gas tube. The thyratron has several characteristics that differentiate it from a vacuum tube. In a vacuum tube, the grid exercises full control over tube conduction. In the thyratron, however, the grid controls only the start of conduction. Once the gas is ionized and the tube is in full conduction, the grid has no further control. Conduction is stopped by either opening the plate circuit or lowering the effective plate voltage to a point where ionization is no longer sustained. For this reason, the circuits in this section either use a high impedance RC plate circuit or the plate circuit is opened by circuit breakers to stop conduction.

Another deviation from vacuum tubes is the delay in starting and stopping conduction. These delays are known as ionization and de-ionization times, respectively. Ionization time is the time necessary to gain sufficient energy for the electrons traveling from cathode to plate to cause ionization (dependent upon type of gas present in tube). Once ionization takes place, the tube is immediately in full conduction. Ionization time can be about 1-2 usec. This delay can be materially decreased by having pre-ionization current flowing before the control grid is impulsed. Pre-ionization current flows in all circuits that have the screen grid returned to a positive power supply. A tube in this case is cut off (no plate current) although screen current is flowing. Circuits that are not affected by long ionization time have the screen grid tied to the cathode to minimize power usage.

De-ionization time is the time necessary (after plate voltage has been sufficiently lowered or removed) for the gas ions to regain their electrons and become neutral atoms again. Because the ions are relatively heavy and slow-moving, this neutralization time can be several hundred microseconds. Thus de-ionization time limits the frequency of operation for thyratrons.

Ion bombardment of the cathode can cause minute quantites of the cathode material to flake off (cathode migration) and travel to the grid mesh. This foreign matter on the grid acts as an electron emitter with the resulting current seriously affecting the bias level of the grid. The current in this case may be only several microamperes, but, with a very high impedance (1 MEG), the bias variation could be several volts.

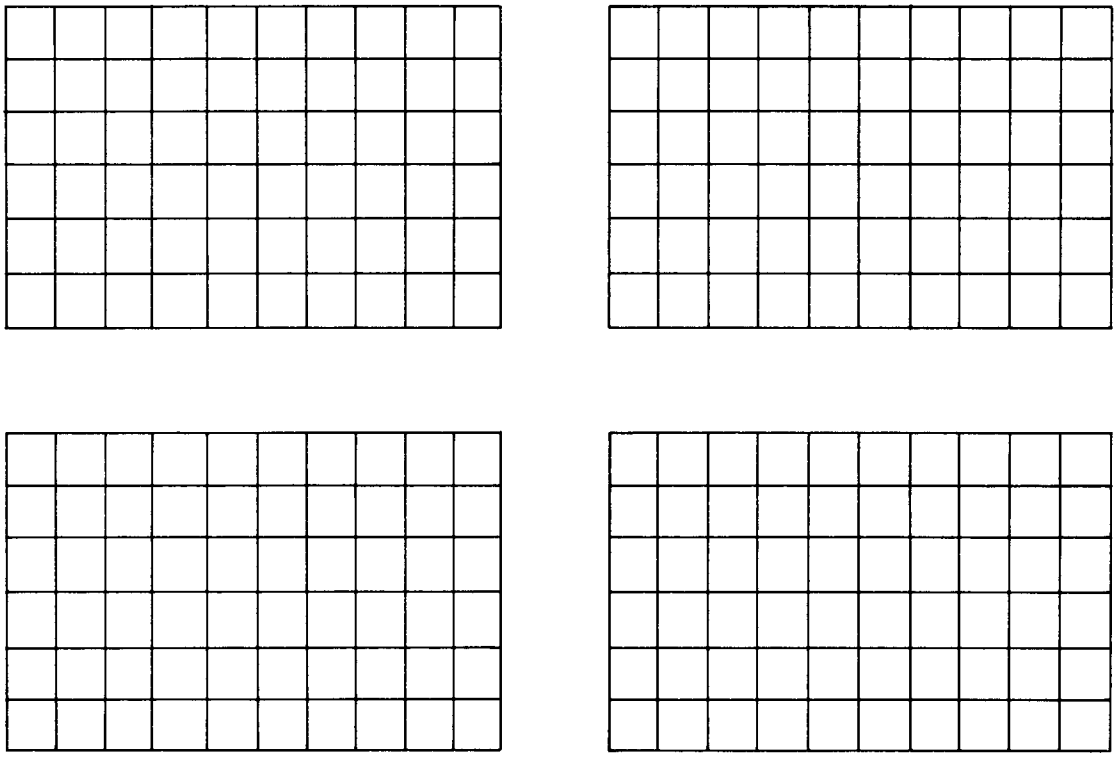
The thyratron changes characteristics not only through the normal factors of cathode interface (increased resistance between cathode sleeve and oxide layer because of tube inactivity), interelement leakage, and cathode migration and deterioration, but also through variation in gas pressure and/or mixture. Excessive negative voltages applied to tube elements during ionization can cause enough ion acceleration to imbed the gas atoms in the metal of the tube element. This lessens the number of gas atoms available for ionization and hence increases the tube drop (cathode-to-plate impedance). The amount of current available from the tube is decreased. This effect can take place in a matter of hours; it is difficult to predict by marginal checks.

It is impossible to state at what control grid bias level ionization takes place. This point is determined largely by the amount of screen grid current, and there fore, by the screen bias level. The average control characteristics of the 2D21 (Appendix, Figure E19) give this firing point.

Most of the above mentioned characteristics of thyratrons do not enter into servicing techniques but should help to familiarize the reader with the gas tube and its operation.

2.14.01 Printer/Punch Magnet Thyratron (TH)

The printer/punch magnet thyratron TH (Figure A28) is used to fire the print magnets in the 717 printer and punch magnets in the 722 punch. In the quiescent state, the input divider holds the grid at -22 volts and the thyratron is cut off. The input pulse to the circuit is the output of the buffer amplifier BAp. A BAp is used to insure a pulse of sufficient duration to fire a thyratron (section 2.04.06, Book B). The input pulse is a 48v positive pulse and is approximately 20 microseconds in duration. A 48v pulse applied to the thyratron causes the tube to conduct. The thyratron is extinguished by breaking the plate return to +72 volts by the use of circuit breakers. When the thyratron fires, the plate voltage falls approximately to ground.



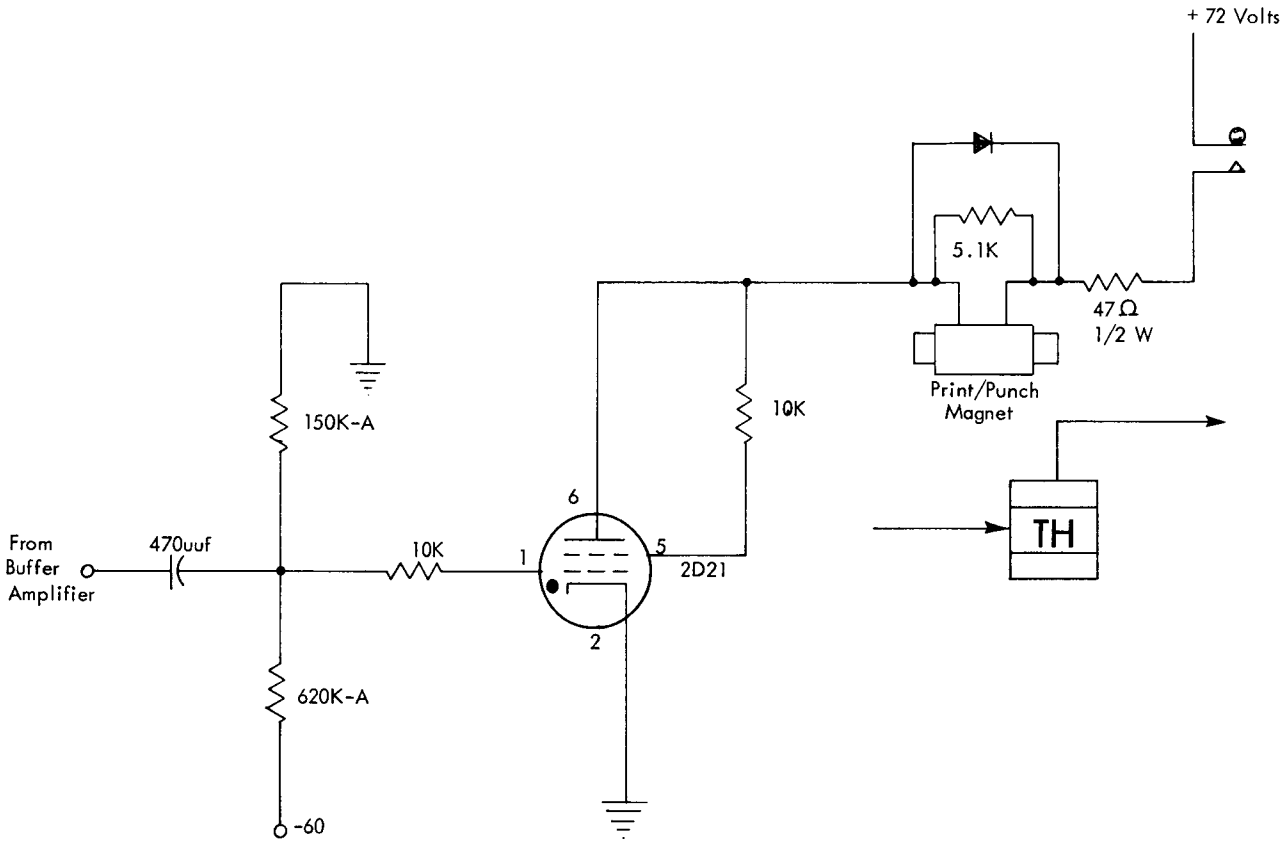


FIGURE A28. PRINT/PUNCH MAG. THYRATRON TH

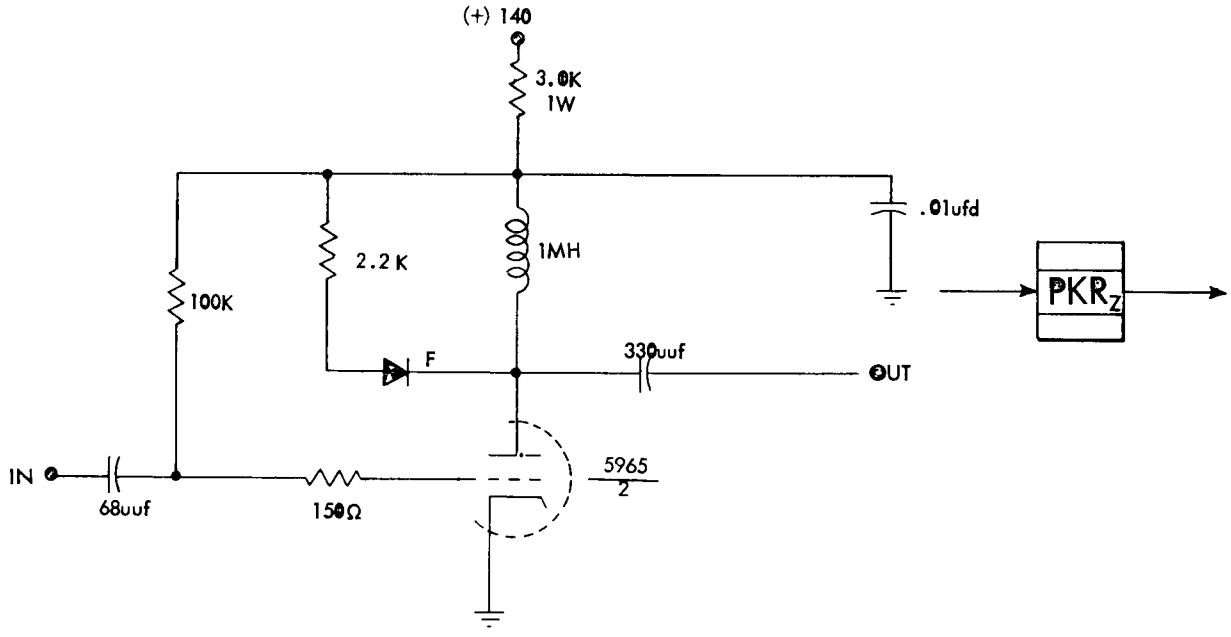


FIGURE A29. WAVE-FORM GENERATOR PEAKER - PKR_Z

2.15.00 PEAKER (PKR)

In the 700 series many circuits have the designation "PKR" meaning peaker circuit. A peaker is a special type of inverter used to produce a narrow pulse of fixed width and large amplitude.

2.15.01 Principles of Peaker Circuit Operation

RLC Circuit

The essential part of a peaker circuit is a parallel RLC network connected to the plate of the tube. The inductance L in the plate circuit is in the form of a coil. The resistance R is the resistance of the coil plus any other resistance placed in parallel with the coil. The capacitance C is any effective capacitance across the terminals of the coil. The capacitance in the RLC circuit includes the shunt capacity of the coil, any capacitor wired across the terminals of the coil, plate-to-ground capacity in the tube, wiring capacity of the output, and input capacity of the following stage. See section 1.04.00, Book E, for LC tank circuit operation.

Peaker Operation

Peakers produce positive output pulses in the following manner. Assume that the tube is initially conducting (Figure A29). The current should be as large as possible within the dissipation rating of the tube. The current is limited by the plate load resistor so that the allowed plate dissipation is not exceeded. A negative input pulse cuts off the tube. The coil then generates a voltage that tends to keep the current flowing; this voltage is of such polarity that the end of the coil connected to the plate becomes more positive than the other end. The capacitor, connected between the coil and the plate load resistor, allows current flow through the coil into the shunt capacitances. If this capacitor were not present, the output of the circuit would be like that of an ordinary shunt-peaked inverter circuit. After the field in the coil collapses and its current goes to zero, the voltage built up across the capacitance then causes current to flow in the opposite direction. This process usually produces oscillations in the plate voltage; that is, the circuit tends to ring. Energy continues to be transferred between the capacitance and the inductance until it is all dissipated in resistance in the circuit. Because only a single positive pulse is required from this circuit, the portion of the ringing output that tends to go more negative than the original plate level is clamped by diodes.

Pulse Width and Amplitude

The pulse width is determined by the resonant frequency of the circuit; it is calculated in microseconds as two pi times the square root of the product LC, where L and C are the inductance in henrys and capacitance in uuf of the plate resonant circuit as described above. Therefore, increasing either the L or the C widens the pulse width.

The amplitude of the original pulse is dependent mostly upon the amount of an inductance in the plate circuit and the rate of change in current through the tube when it is cut off. The pulse amplitude in volts may be approximated by the expression LI_O/T, where L is the plate circuit inductance in millihenrys, I_O is the original tube current in milliamperes (assuming complete cut-off and linear fall of

current), and T is the time in microseconds from the beginning of the current fall to cut-off. This formula shows that increasing the initial current, the inductance, or the speed of cut-off increases the amplitude of the output voltage pulse. The expression LI_O/T is theoretically correct only when there is no shunt capacitance across the coil. The greater the capacitance across the coil, the more the amplitude of the pulse is reduced.

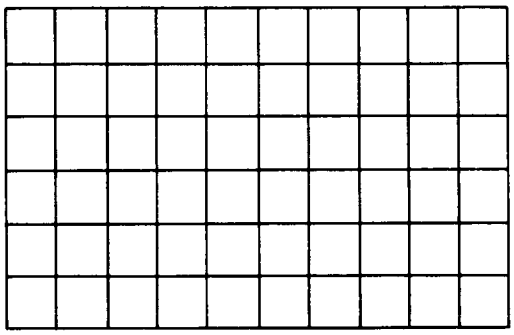
A more exact computation may be made when the LC product is large in comparison with the cut-off time. The pulse amplitude in volts equals I_O times the square root of L/C, where I_O is in milliamps, L is in microhenrys, and C is in micro-microfarads.

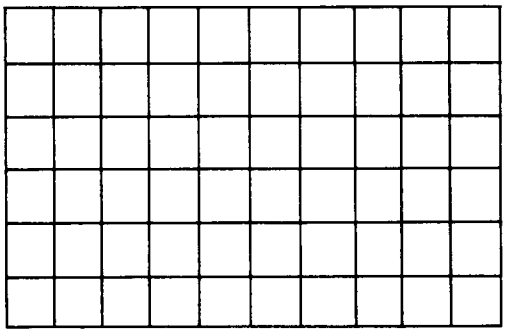
Other Considerations

The input has some special restrictions. First, it must have a fast fall to produce a fast change in plate current. Second, the input pulse must be longer than the output pulse, or else the rise of the input pulse interferes with the action of the ringing circuit. Third, the input pulse must go far enough negative to keep the tube cut off even when its effective plate voltage is raised by the peaking action. The plate voltage usually rises higher than the plate supply voltage. The load capacitance and shunt capacitance across the coil may be sufficient to obtain the desired pulse width, but, if it is not, a capacitor may be wired in parallel with the coil to widen the pulse.

2.15.02 Wave Form Generator Peaker (PKR_Z)

The wave-form generator peaker PKR_Z (Figure A29) is used in the memory and the wave form generator to generate peaked pulses. For general peaker circuit operation, see section 2.15.01, Book A. The input pulse to the PKR_Z is a negative shift of at least 60 volts per microsecond. The peaked pulse at the plate of the PKR_Z is approximately 100 volts in amplitude and 0.4 microseconds in duration. There is a slight negative overshoot at the plate when the PKR_Z comes back into conduction. The output pulse of the PKR_Z is a 90v pulse, 0.4 microseconds in duration. This pulse is passed through cathode followers and divider networks until the final amplitude is approximately 40 volts. The pulse is used for the memory and accumulator samples. The 2.2K resistor in series with the diode in the plate circuit limits the current through the diode during the time the diode is conducting. The .01-ufd capacitor in the plate tends to maintain a steady potential at the top of the one-millihenry coil.





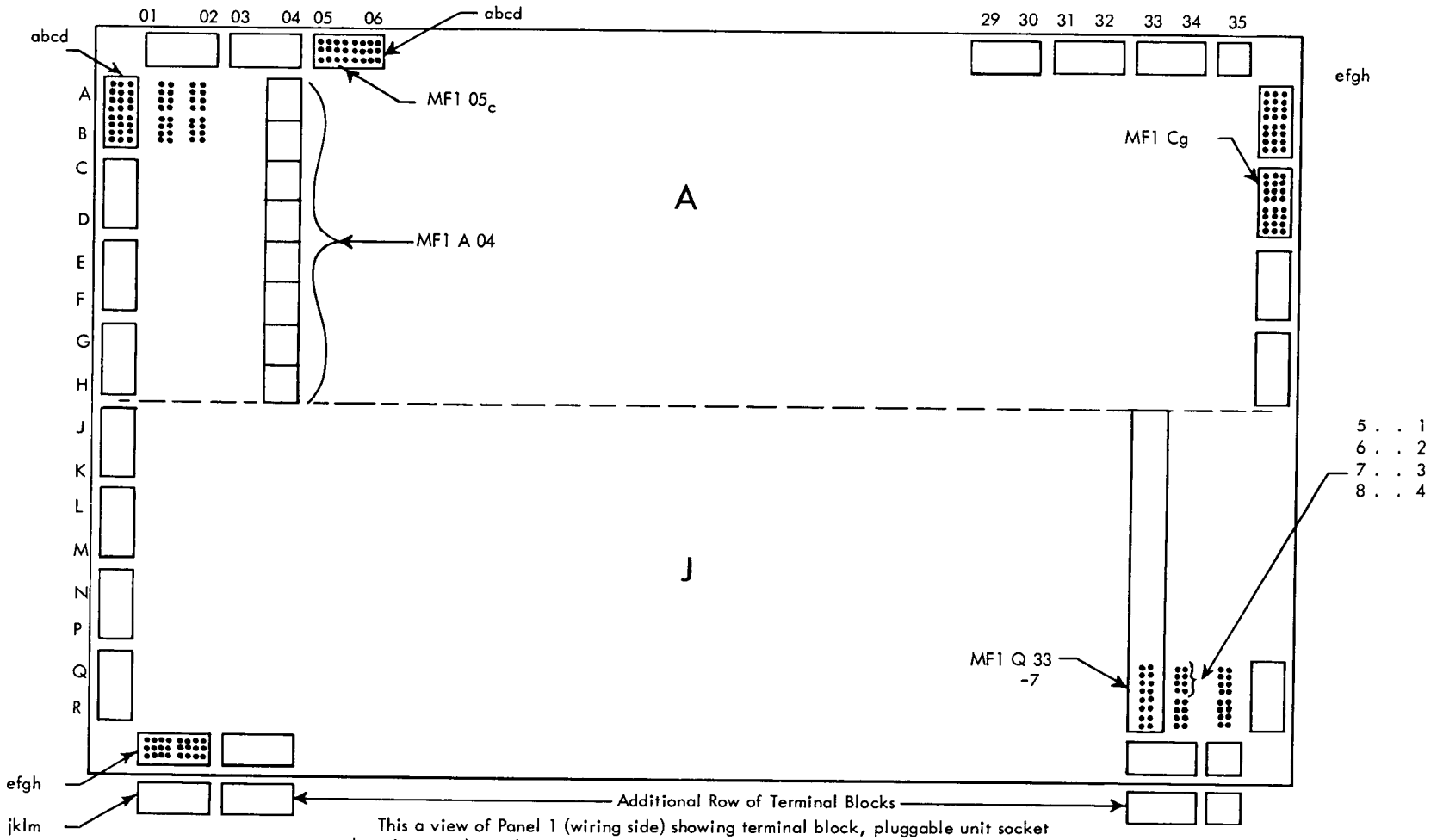
Component Circuits

Book B. 701-704-709 Components

CONTENTS

CONTENTS (continued)

CONTENTS (continued)



This a view of Panel 1 (wiring side) showing terminal block, pluggable unit socket locations, and coordinate system.

Note: Alphabetic characters O and I are not used; the letters jklm are used for any extra row of blocks.

FIGURE B1. MAIN FRAME, PANEL 1

1.00.00 GENERAL INFORMATION

1.01.00 CIRCUIT LOCATION

A coordinate reference system is used on all pluggable unit panels. This system is illustrated in Figure B1. With this reference system, it is possible to locate pluggable unit sockets, pluggable-unit pin connections, and edge connector connections.

The following location codes are used as an illustration in Figure B1.

For a pluggable unit:

MF	1	A	04
Frame	Panel	Section	Column

For a pluggable unit panel pin:

MF	1	Q	33	-7
Frame	Panel	Row	Column	Pin Number

For an edge connector:

MF	1	C	g	MF	1	05	c
Frame	Panel	Row	Pin	Frame	Panel	Column	Pin

For a tube location within a pluggable unit:

The top tube in the unit is tube 01, the one immediately below is tube 02, then 03, and so on.

For location of a tube in the machine:

MF 2 J 06	-3
Location of the pluggable unit	Location of the tube in the pluggable unit

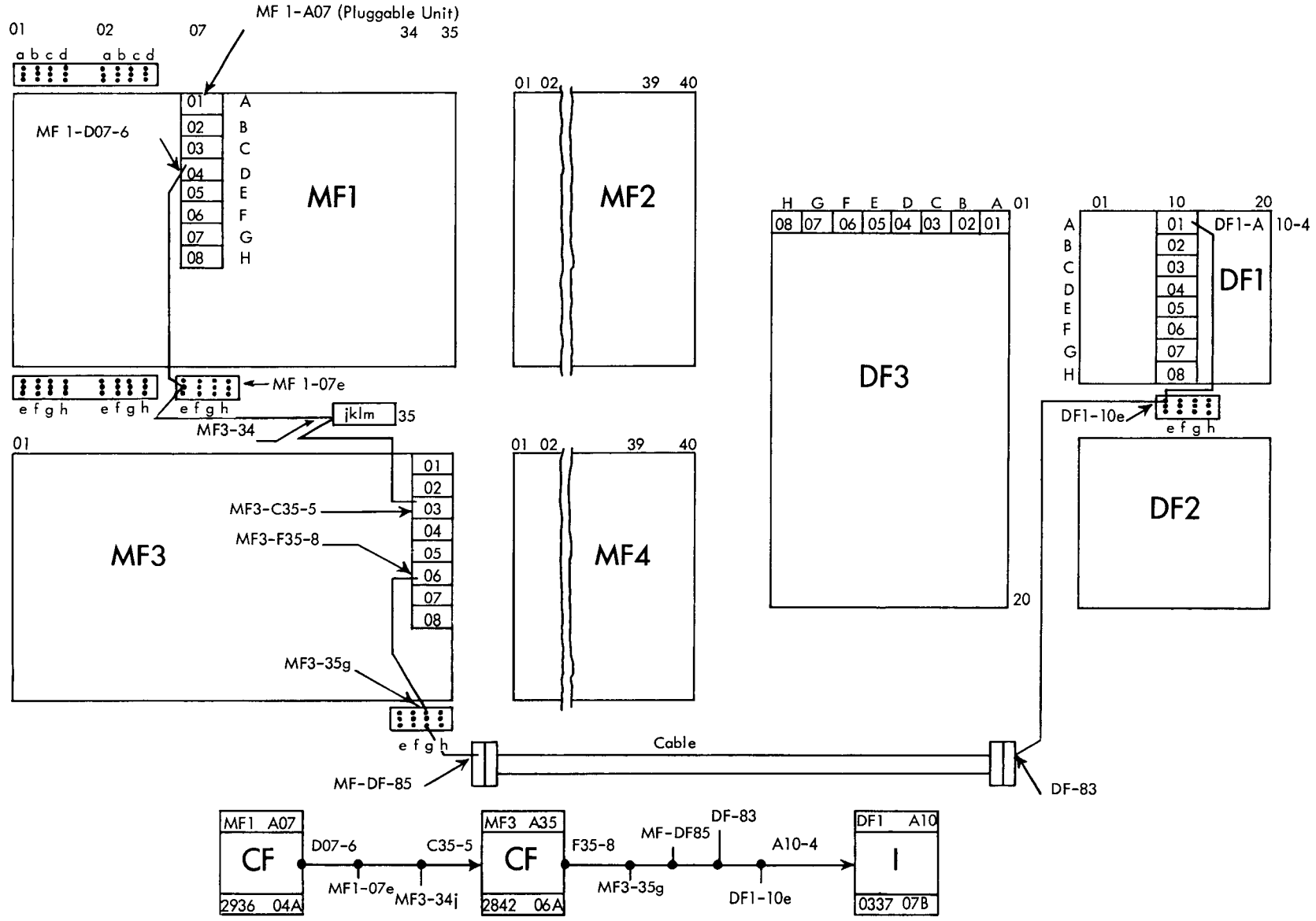


FIGURE B2. PANEL WIRING, SYSTEMS REPRESENTATION

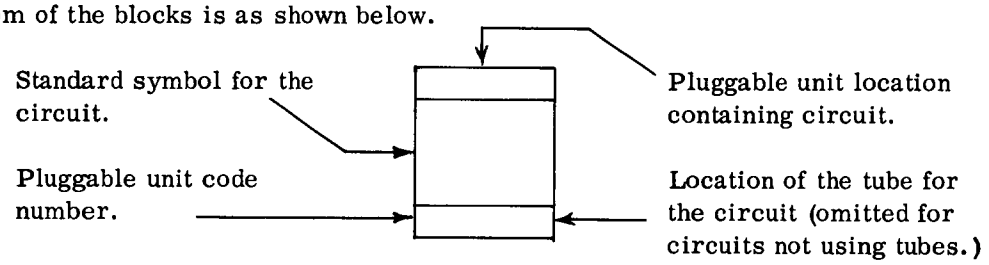
1.02.00 HALF-TUBE DESIGNATIONS

Half-tube sections are located by adding the suffix A or B after the tube location number, such as, 06A or 02B. The A section of a tube is the section that has an element connected to the lowest pin number, exclusive of heated connections. The B section is the remaining section. Using this rule, the A and B sections for some common tubes are as follows:

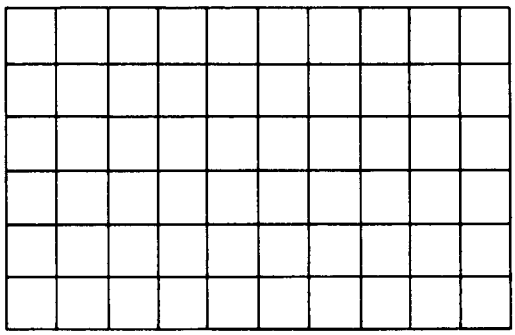
Tube	Section A	Section B
5965	1, 2, 3	6, 7, 8
5687	1, 2, 3	6, 7, 9
5844	1, 6, 7	2, 5, 7

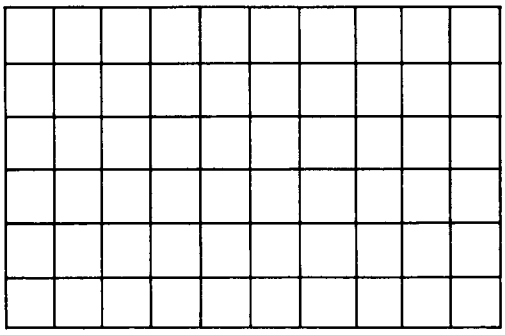
1.03.00 SYSTEM BLOCK DIAGRAMS

The system diagrams serve as an aid in explaining the operation of the machine, as well as a service aid in locating circuits. The diagrams are made up of standard blocks, as illustrated in Figure B2. The identification in the strips at the top and bottom of the blocks is as shown below.



Lines between the blocks shown in Figure B2 represent the signal wires connecting individual circuits. Wires connected to panel socket pins or terminal block pins are given the numbers of those pins. Frame and panel indications are dropped from the pin number if they are clear from the origin of the wire. A wire joining two blocks on two different pluggable units has two socket pin numbers, one at each end. If the two units are on different panels, there are two numbered edge connectors also. If a wire goes from one frame to another, a cable connection is indicated and labeled by the initials of the frame in which the previous block is located and, in the case of cables coming from the main frame, it is labeled by the initials of the frame to which the line is going, as well as the cable terminal number. Wires that go off the edge of a drawing are labeled with the page number of the drawing to which they go.





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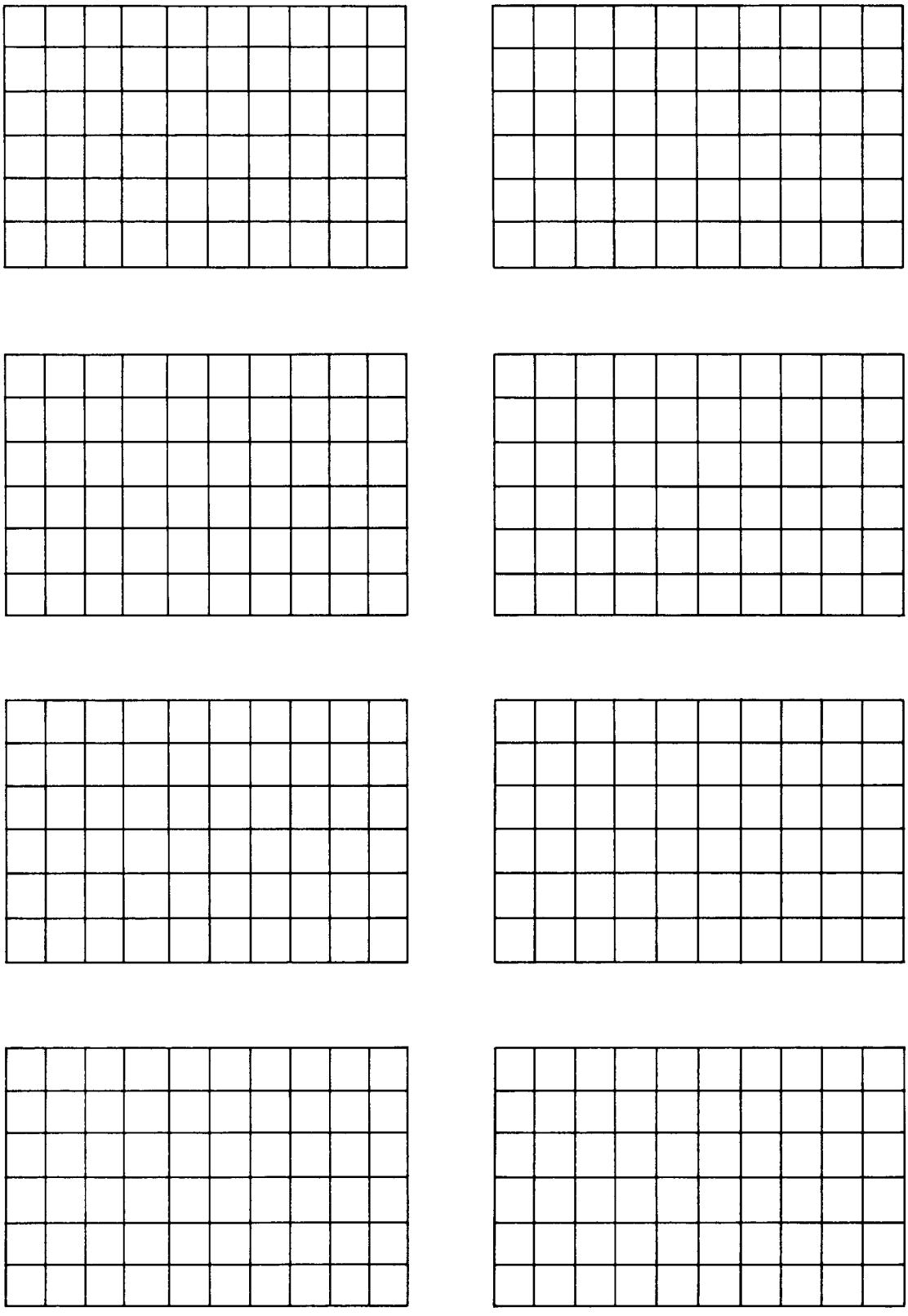
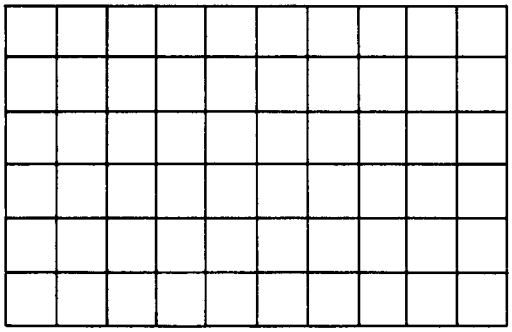


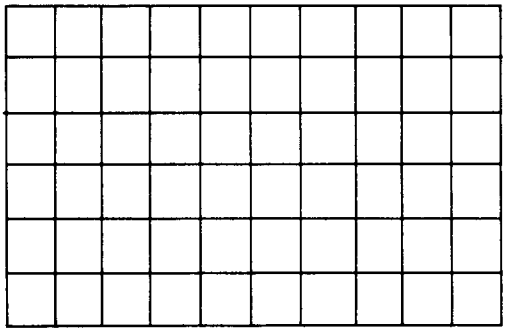
2.00.00 COMPONENT CIRCUIT DESCRIPTIONS

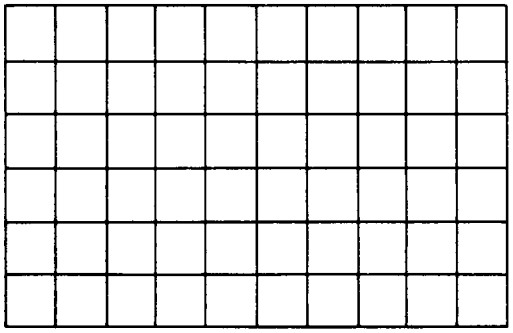
This section describes each component circuit that is represented by a logic block. The circuit descriptions are arranged in the same order as the circuit schematics that are found in the systems for each machine. Thus, 2.01.01 (inverter) is the same circuit that is found on 4.01.01. Numbers unassigned as of this writing are so noted.

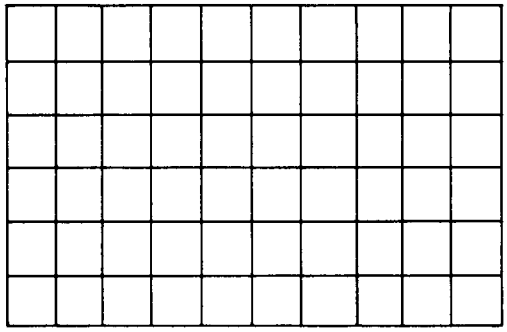
Each circuit description is designated by a three-part decimal number. The first part of the number is a 2, which represents this section. The second part of this number represents the functional classification of the circuit. These functional classification numbers are as follows: 1--inverters, 2--triggers, 3--single shot multivibrators, 4--amplifiers, 5--cathode followers, 6--diode circuits, 7--delay circuits, 8--pulse generators, 9--pulse-shaping circuits, and 10--special circuits. These classifications are rather loose, and some circuits may fall into either of two categories. The third part of the number is the number of the circuit within its classification. The circuits are usually arranged alphabetically within one category.

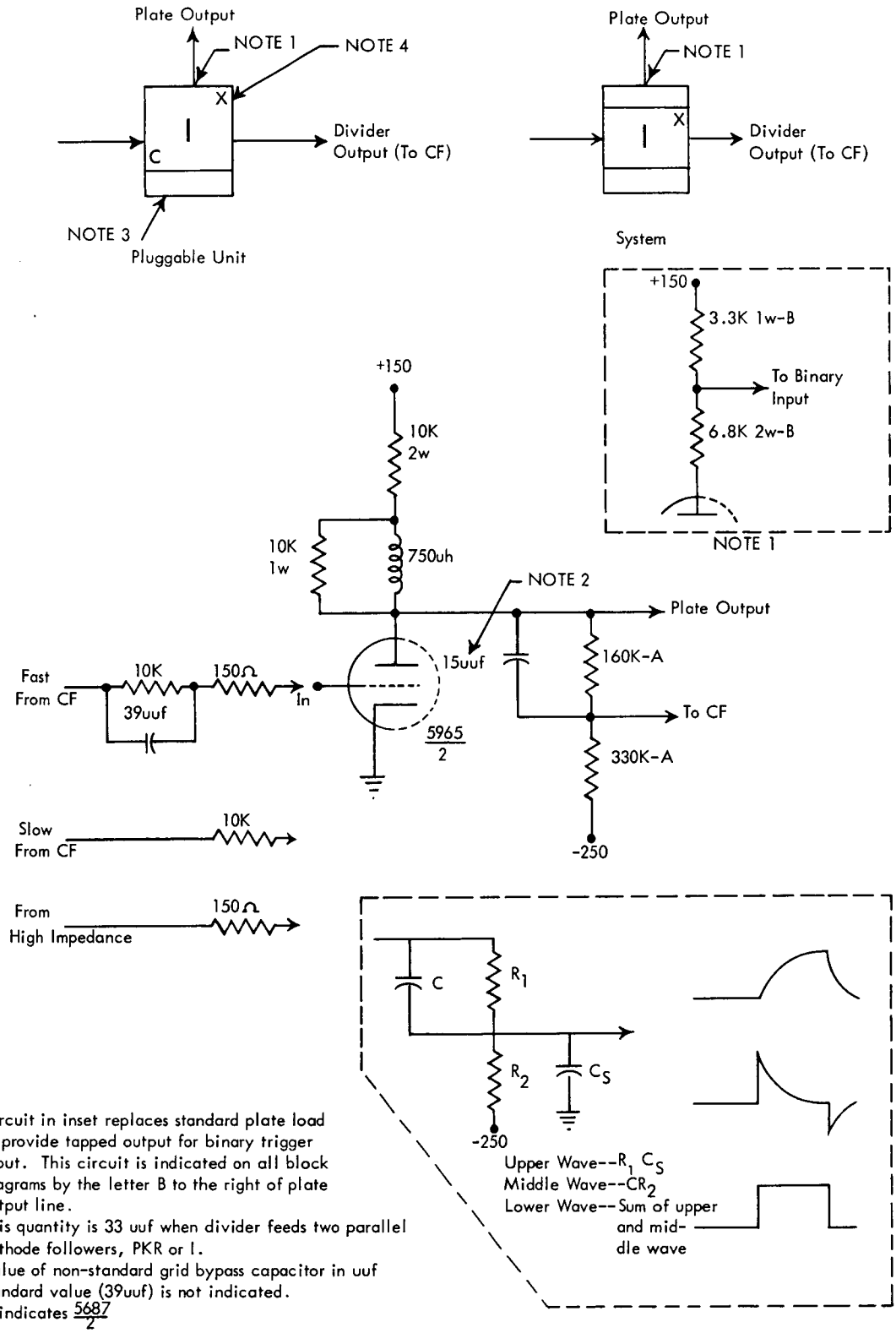
Many of the component circuits are not complete in themselves; that is, components in the circuits that feed them or are fed by them are just as important to the circuit operation as the components shown in the corresponding block.











NOTES:

1. Circuit in inset replaces standard plate load to provide tapped output for binary trigger input. This circuit is indicated on all block diagrams by the letter B to the right of plate output line.
2. This quantity is 33 uuf when divider feeds two parallel cathode followers, PKR or I.
3. Value of non-standard grid bypass capacitor in uuf standard value (39uuf) is not indicated.
4. X indicates $\frac{5687}{2}$

FIGURE B3. INVERTER (I)

2.01.00 INVERTERS

The operation of the standard inverter is discussed in section 2.05.00, Book A.

2.01.01 High-Speed Inverter (I)

The resistor in the plate circuit in parallel with the coil serves as a bobbin for the coil and also serves to prevent ringing in the plate circuit after the initial peaking action has occurred. This circuit produces a pulse with a nominal rise time of less than 0.2 microsecond and a fall time of about 0.3 microsecond. The coil causes slight overshoot in the rise of the plate voltage, but it has practically no effect upon the fall time of the circuit.

Inputs

The inverter may have one of three standard inputs. If the inverter is fed from a high-impedance source, its input is only the 150-ohm parasitic suppression resistor. If the circuit is fed from a low-impedance source, such as a cathode follower or an OR circuit, a 10K grid-current-limiting resistor is used instead of the 150-ohm resistor. If an AND circuit with a low load resistance feeds the inverter, the grid-current-limiting resistor may be used. If high-speed operation is required, the 10K resistor is shunted with a 39-uuf capacitor, but since this leaves no unbypassed parasitic resistor next to the grid, a 150-ohm resistor is inserted between the RC combination and the grid. The addition of the capacitor makes only about a 0.05-microsecond difference in rise time. There are no identification markings on the block diagrams to indicate which of these inputs is used. The inverter has an approximate input capacity of 35 uuf. Required inputs for the inverter are from +5 to +15 volts and -15 to -30 volts.

Outputs and Voltage Levels

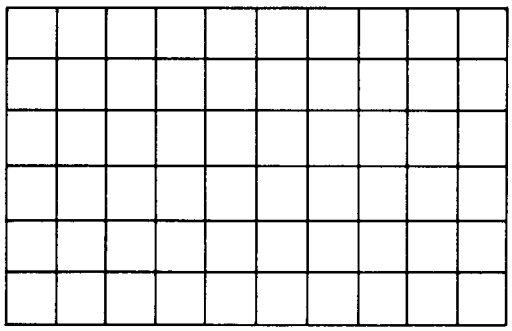
Outputs from the inverter may be from the plate, from a tapped plate load resistor, or from a divider connected to the plate. The voltage swing from a full plate output is about +60 to +150 volts. If the inverter is to feed a binary input of a trigger, its plate resistor is composed of a 6.8K resistor next to the plate and a 3.3K resistor next to +150 volts, and a B is placed next to the plate output line on the block diagram. The coil and shunting resistor are not used for the binary output. The voltage appearing at the junction of these two resistors feeds the binary input. This voltage swing is from +120 to +150 volts. The voltage divider connected to the plate is present only when a standard signal output is required. The plate swing when the divider is present is about +55 to +142 volts, and the divider output is nominally -41 to +14 volts. Since the output is high-impedance, it must feed a cathode follower directly, and the output of this cathode follower fixes the standard signal level. The divider output is compensated according to the number of cathode followers that it feeds.

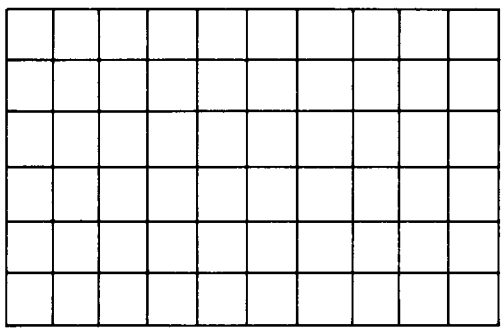
Delay of an Inverter

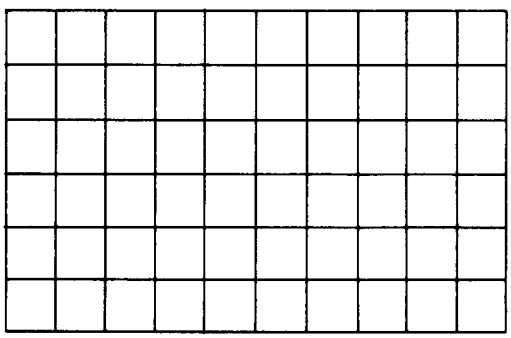
Another characteristic of an inverter is the delay it produces. Delay is defined as the time elapsed between the beginning of a voltage shift at the grid and the beginning of the resultant shift at the plate. Since a positive input pulse starts from a level of about -15 to -30 volts, and it must rise to the cut-off point for the tube (about -6 volts in this circuit) before any conduction occurs, the time required to rise in this point appears as delay in the output. Conversely, any time required for an input pulse to fall from the nominal +10 level (where grid current flows) to ground (where grid current ceases) also appears as a delay in the output. Therefore, the slower the voltage transition at the grid, the more the delay that is produced by the circuit. This delay is about one half of the rise or fall times of the input pulse. Delay of an inverter should not be confused with its own rise and fall time characteristics. The interval between the beginning of the input transition and the time the output transition reaches its final value is equal to the delay plus the time of the output transition itself.

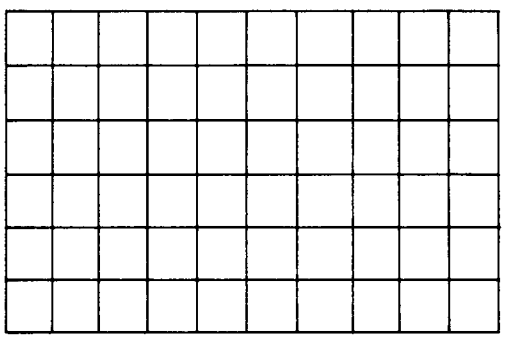
Compensated Output

The output circuit is designed to produce fast rise and fall time. See lower insert, Figure B3. The normal output of the inverter must feed the next circuit where stray capacitance (C_S) acts to distort the wave shape. When C_S must be charged or discharged through R1, the rise or fall time is seriously slowed. But if compensating capacitor, C, is added, forming a differentiating circuit with R2, a typically differentiated wave form is added. The sum of the two is a good square wave to the grid of the next tube.









2.01.02 Inverter-Dash Generator (I_A)

This component was assigned to 701 electrostatic memory and is not used now.

2.01.03 Inverter-Sync Generator (I_B)

This inverter (Figure B4) is used in the inverted sync generator to amplify the inverted clamp input pulse.

2.01.04 Clock Inverter (I_C)

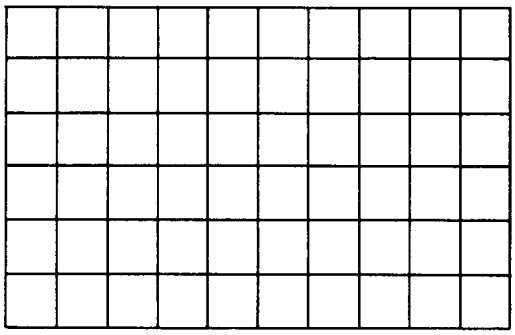
I_C is the symbol for the inverter (Figure B5) that feeds the binary trigger, driving the clock (Systems diagram 8.04.00). This circuit receives clock drive pulses that are delayed by a delay line to position the clock pulses in relation to the sync and clamp pulses. The rise of the pulse is not so sharp as that of the clock drive pulse from the clock drive circuit, but it still has about a 0.2-microsecond rise time. The plate wave form is a 50-volt swing for feeding the binary trigger. The low value of plate resistance allows the plate voltage to return to +150 volts before the next input pulse arrives.

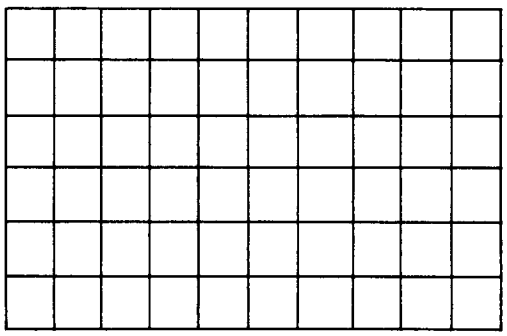
2.01.05 Clamp Inverter I_{CL}

The master-inverted-sync and master-inverted clamp pulses are distributed from the sync and clamp generators by coaxial transmission lines to the arithmetic column units. Here these pulses must be inverted before they feed the microsecond delay units in the form of sync or clamp pulses. Each arithmetic column unit contains one sync inverter and one clamp inverter to feed the sync and clamp pulses to the three delay units in each column unit.

The input of each of these inverters is isolated from the transmission lines by a RC-coupled cathode follower. For economy reasons, each cathode follower feeds the inputs of either two sync inverters or two clamp inverters. One inverter is located in the unit containing the cathode follower; the other is located in an adjacent unit. There is only one of these RC-coupled cathode followers in each column unit.

For example, the cathode follower in column S and each even-numbered column receives master-inverted-clamp pulses from pin 07-3 and feeds isolated-inverted-clamp pulses to the clamp inverter in that column and also to the clamp inverter in





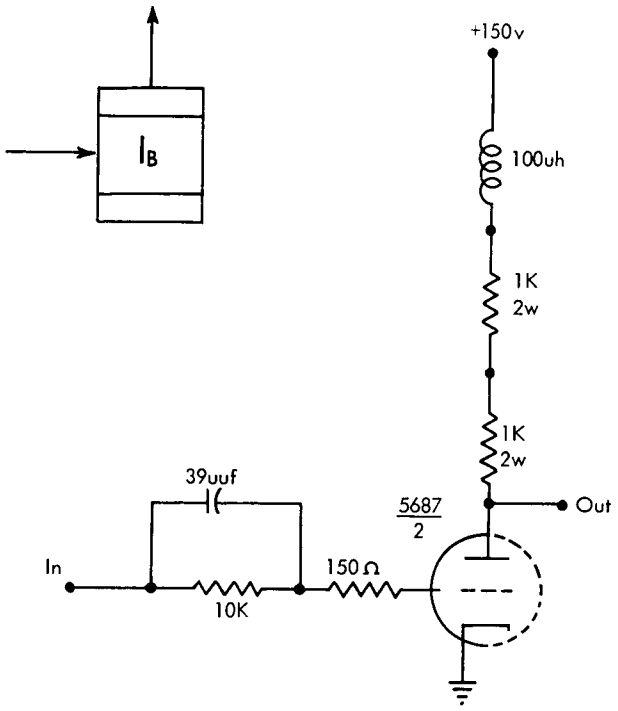


FIGURE B4. INVERTER (I_B)

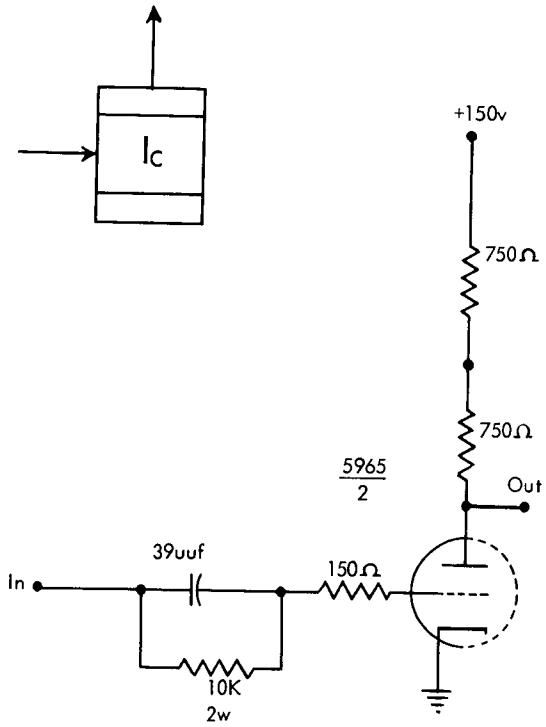
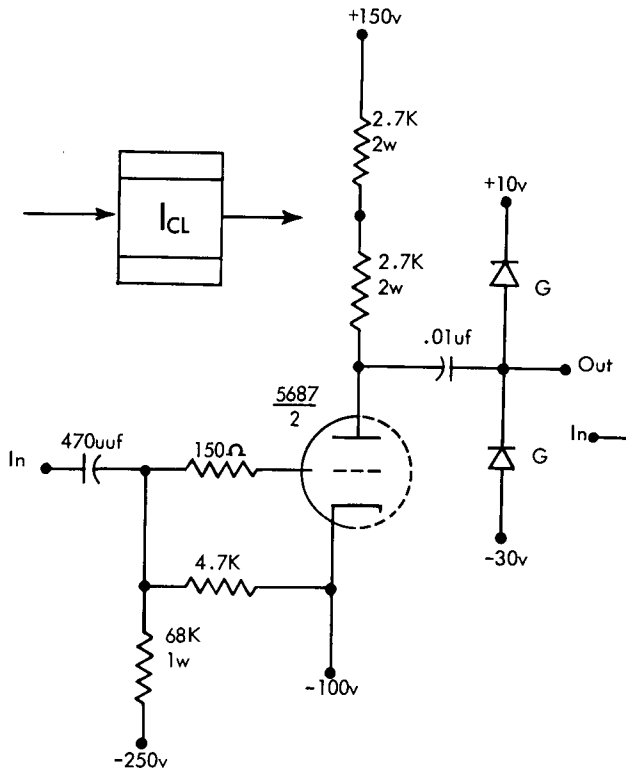


FIGURE B5. INVERTER (I_C)



Note: The filament center tap is biased at -50v.

FIGURE B6. CLAMP INVERTER (I_{CL})

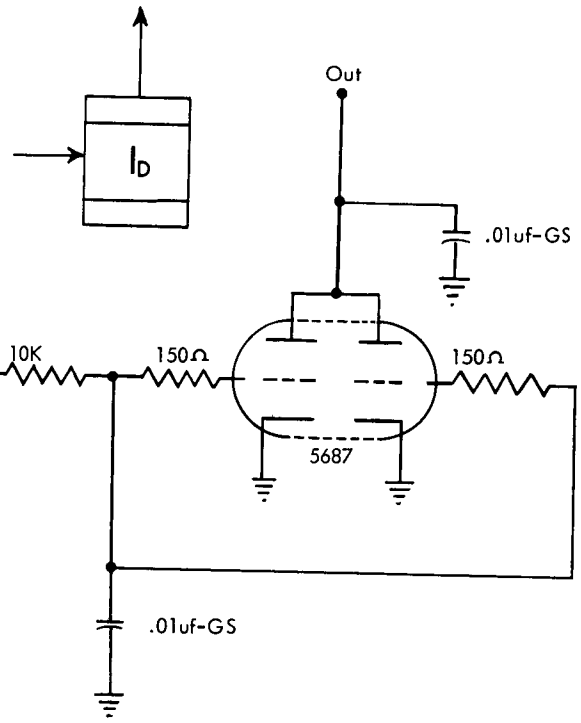


FIGURE B7. INVERTER (DRUM) (I_D)

the next higher, odd-numbered column through pin 07-4. Conversely, the cathode follower in each odd-numbered column receives master-inverted sync pulses from pin 07-2 and feeds isolated-inverted-sync pulses to the sync inverter in that column and also to the sync inverter in the next lower, even-numbered column through pin 07-8. (Column 1 feeds column S.) Therefore the two-column units act together in supplying sync and clamp pulses to their delay units; one may not operate without the isolated-inverted-sync or clamp pulses that the other provides.

Circuit Description

Clamp inverters, I_{CL}, (Figure B6) are located in each column unit to provide clamp pulses of nominal +10v to -30v levels to the delay units. The input and output of this inverter are RC-coupled so that the proper levels may be obtained. The input is biased by a divider to about -110 volts with respect to ground. The tube is normally conducting lightly, but during a pulse input, the tube is brought into heavy conduction. Because the clamp pulse must be short, the plate resistance is made small. The plate voltage swing is from about +90 volts to -20 volts, and the output is caught by the diodes from +10 to -30 volts.

2.01.06 Inverter (Drum) (I_D)

I_D is a special inverter circuit (Figure B7) used to pick read relays, write relays, and timing and index relays in the drum system. These inverters feed a variety of relay coil combinations. The capacitor on the grid provides integrating action so that noise pulses do not tend to pick the relay coils.

Typical output levels for this circuit are:

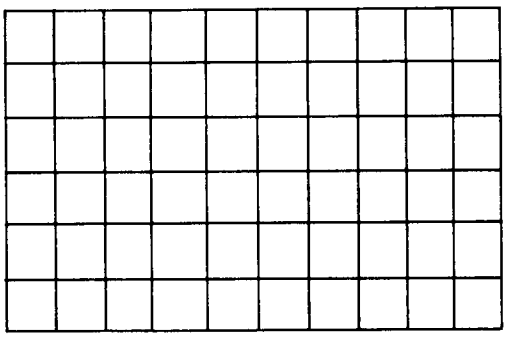
+60 to +80 and +150	for timing and index relays.
+55 to +75 and +150	for read relays.
+42 to +72 and +150	for write relays.

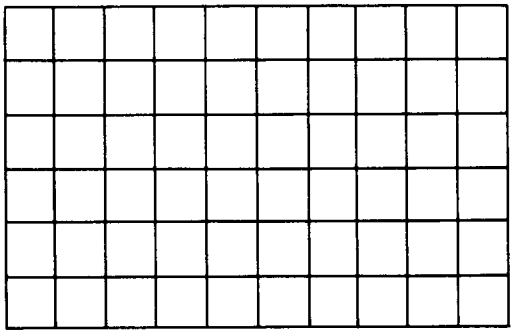
2.01.07 Inverter (I_E)

This component was assigned to 701 electrostatic memory and is not used now.

2.01.08 Inverter (I_F)

This component was assigned to 701 electrostatic memory and is not used now.





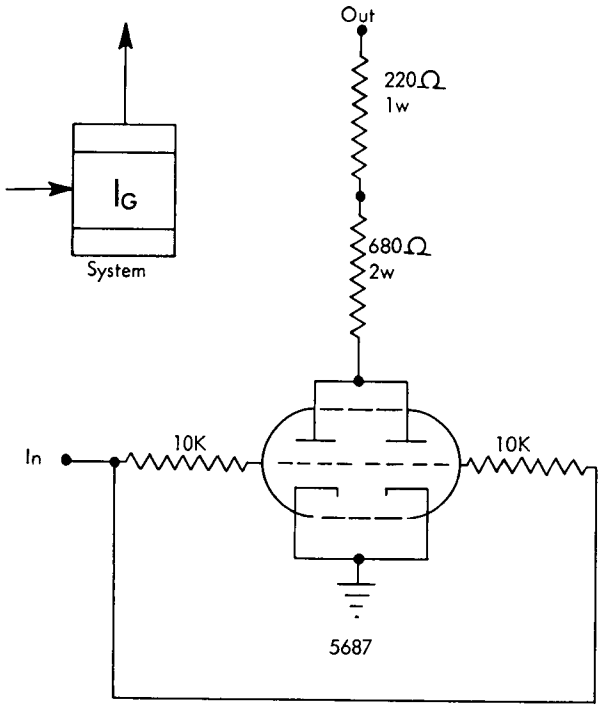


FIGURE B8. INVERTER (I_G)

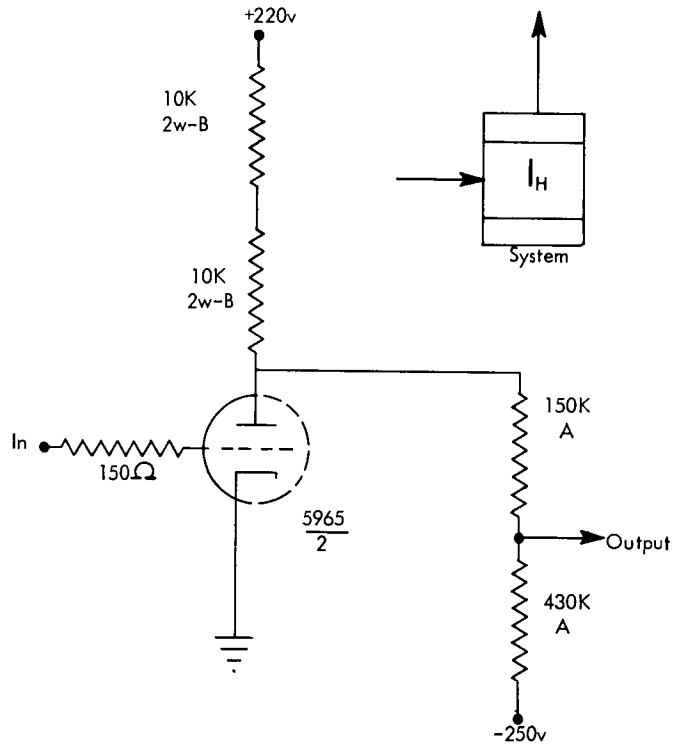


FIGURE B9. INVERTER (I_H)

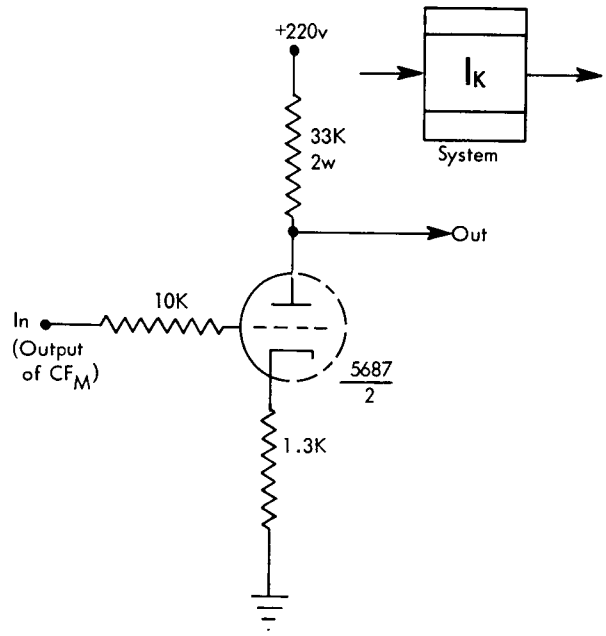


FIGURE B10. INVERTER (I_K)

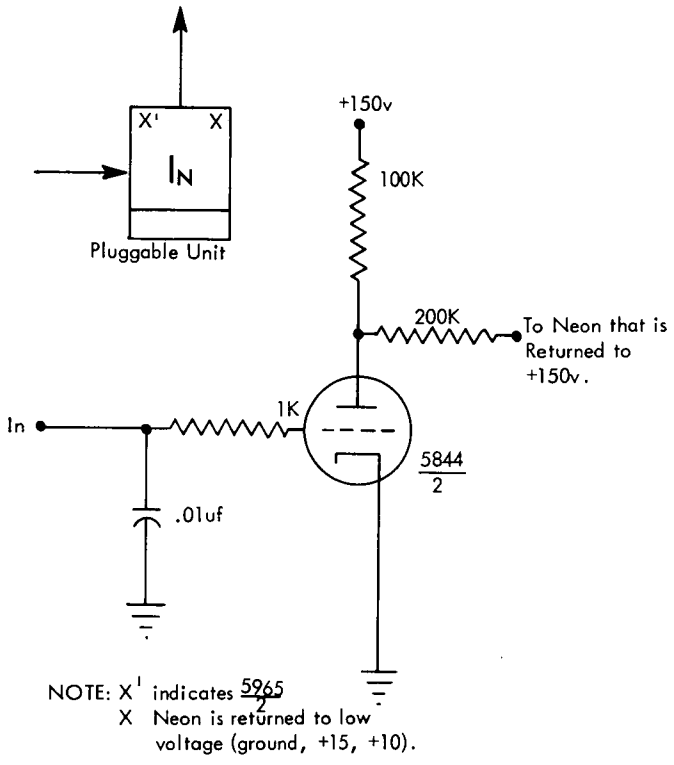


FIGURE B11. NEON INVERTER (I_N)

2.01.09 Inverter (I_G)

I_G is the symbol for an inverter circuit (Figure B8) which powers some of the 48-volt indicator lamps. It is fed a signal of about -30 to +60 volts and its output is about +102 to +150 volts. The plate resistance for the I_G is chosen to give the proper voltage drop across the bulbs. In some instances, this resistance value may be slightly different than shown for adjusting the brightness of the indicator lamps to like values. Each lamp requires about 48 milliamperes; therefore, a full tube is used.

2.01.10 Inverter (I_H)

The special circuits I_H and PCF_A are used to supply driving voltage of opposite polarities to the circuits feeding opposite ends of the moving clutch coil. The I_H (Figure B9) is designed so that a 40v signal produces a swing of about 140 volts at the plate. The input divider is provided for two purposes: (1) for dividing the two sets of input voltages so that the tube is cut off for the more negative voltages of each set, and conducts for the more positive voltages of each set, and (2) to provide grid current limiting for the upper level voltages. With the tube removed, the divider tends to produce voltages of about -94 volts for +10v input, +60 volts for +150v input and -250 volts for a floating input. The equivalent plate circuit is 24K returned to about +83 volts. The large resistance in the plate circuit is used to provide a large plate swing.

2.01.11 Inverter (I_J)

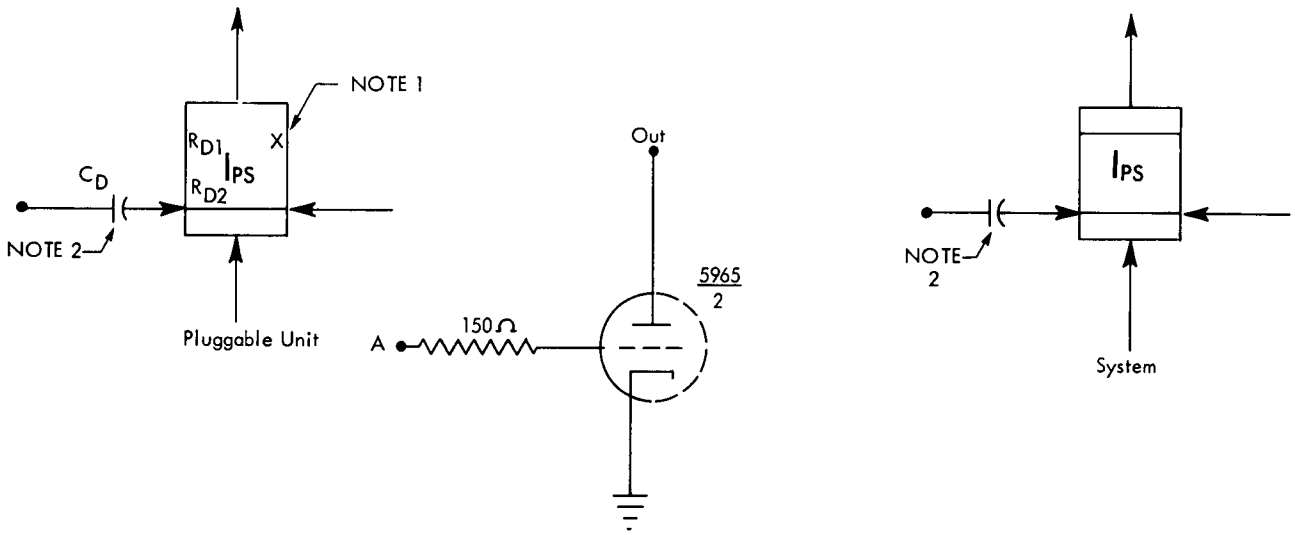
This component was assigned to the 701 field tester only, and is not used now.

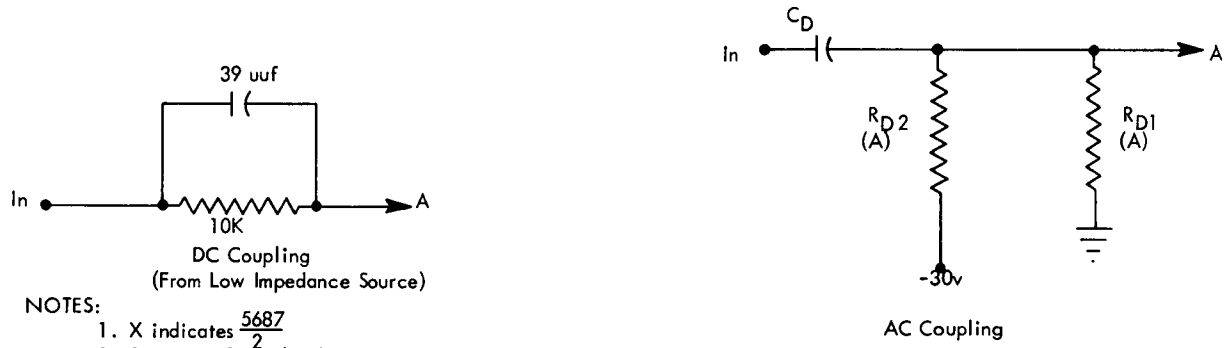
2.01.12 Inverter (I_K)

This component (Figure B10) is used in the tape read circuits to feed an SS_O (section 2.03.04, Book B). The function of the I_K is to supply a satisfactory negative shift to the SS_O. The inverter has some cathode degeneration, tending to keep the operation class A.

2.01.13 Neon Inverter (I_N)

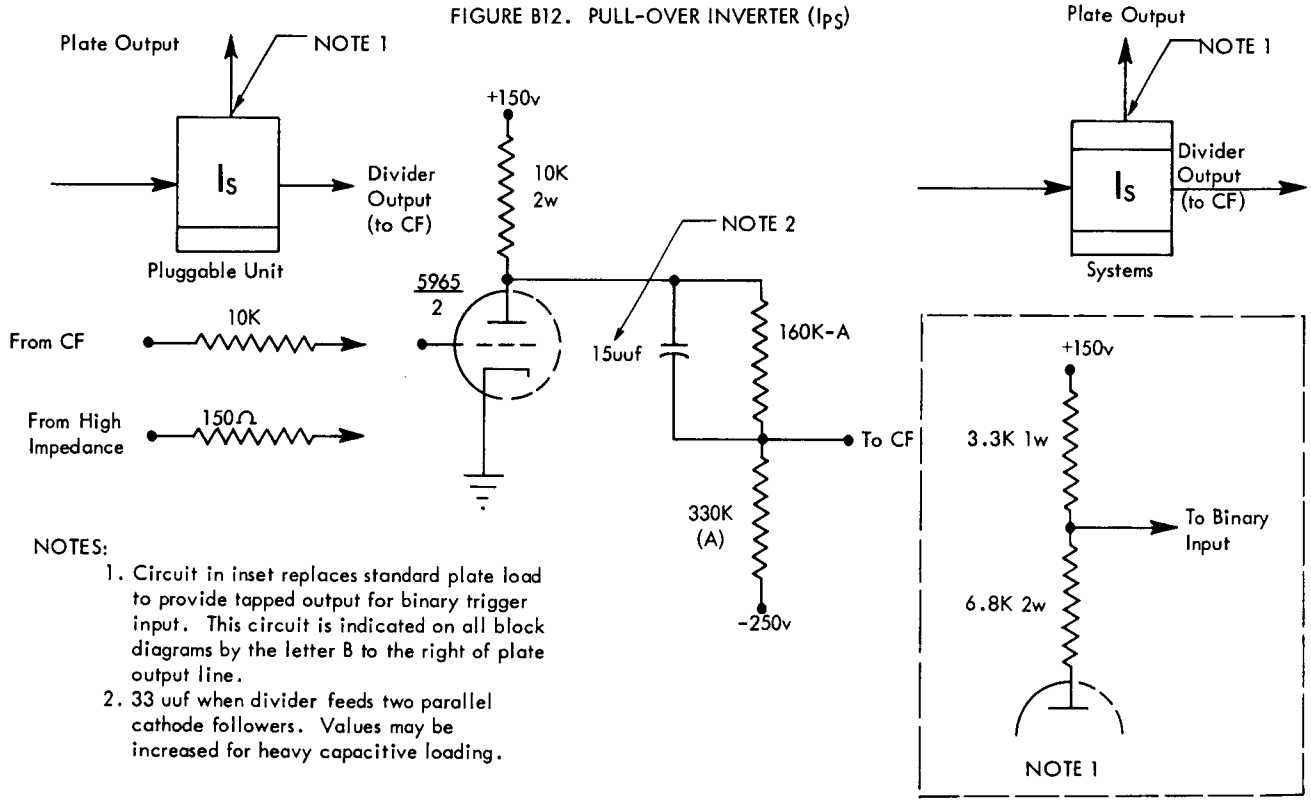
I_N is the symbol for the neon inverter circuit (Figure B11) used in the main frame to drive the operator's panel neon indicator lights. It receives an input signal through an integrating resistor located in the column units. This signal averages around the +10v or about -25v levels, although it is not a smooth wave form. The output signal varies from +150 volts to about +80 volts, depending upon whether the neon is fired.





NOTES:
1. X indicates $\frac{5687}{2}$
2. Capacitor Symbol indicates AC input. No capacitor symbol indicates DC input.

FIGURE B12. PULL-OVER INVERTER (I_{PS})



NOTES:
1. Circuit in inset replaces standard plate load to provide tapped output for binary trigger input. This circuit is indicated on all block diagrams by the letter B to the right of plate output line.
2. 33 uuf when divider feeds two parallel cathode followers. Values may be increased for heavy capacitive loading.

FIGURE B13. SLOW INVERTER (I_S)

2.01.14 Neon Inverter (I_{NA})

This component was assigned to 701 electrostatic memory and is not used now.

2.01.15 Pull-Over Inverter (I_{PS})

The inverter circuit used for plate pull-over of trigger or single-shot circuits is called a pull-over inverter, I_{PS} (Figure B12). Its plate load is the load resistor of the plate to which it is connected, and its conduction pulls down the voltage on that plate. Its positive input pulse should rise higher than +5 volts with the tube removed and must fall lower than -15 volts for reliable operation. With the tube in place, the input cannot rise appreciably above ground because of grid-circuit clipping. When a pull-over inverter is feeding a single shot and the pulse width of the input is greater than 75 percent of the single-shot pulse width, the inverter input must be RC-coupled; otherwise it may be direct-coupled. If the input is fed from a low-impedance source and is direct-coupled, it must have grid-current-limiting circuit shown at the bottom of Figure B12 added to point A. The values of resistors used in the RC-coupled input are shown in the pluggable unit blocks. Although the input shown on the block in Figure B12 is located on the side of the block at the bottom, it may alternatively be located at the bottom in the middle, or at the right side near the bottom. An X placed in the upper right portion of the block indicates that a 5687 tube is used instead of the standard 5965.

2.01.16 Inverter (I_R)

This component (Figure B14) is used to supply current to the moving clutch coil in the tape unit and to drive relays in the operator's panel circuits. It is also used in the drum-read-sample generator, where it functions as a pull-over inverter for an SS_D.

2.01.17 Slow Inverter (I_S)

In applications where the speed of the high-speed inverter is not needed, a slow-speed inverter, I_S (Figure B13), is used. This inverter is basically the same as the high-speed inverter (section, 2.01.01). The principal difference is that neither the coil nor the damping resistor is used in the slow inverter. The omission of the coil causes the rise time of a slow inverter output pulse to be about 0.5 microseconds, but the fall time is not changed from that of the high-speed inverter, namely 0.3 microseconds. Because the high-speed input of the high-speed inverter is not needed, only a 150-ohm parasitic suppression resistor or a 10K grid-current-limiting resistor is used in the input circuit. No tapped plate output is taken from this inverter, but the divider output is identical to that of the high-speed inverter. Input levels required for correct operation and output voltages are identical to those of the high-speed inverter. Delays are also produced in this circuit as in the high-speed inverter.

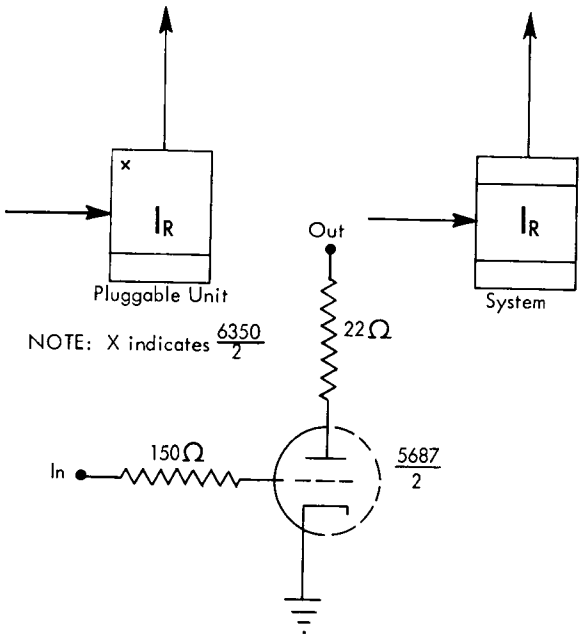
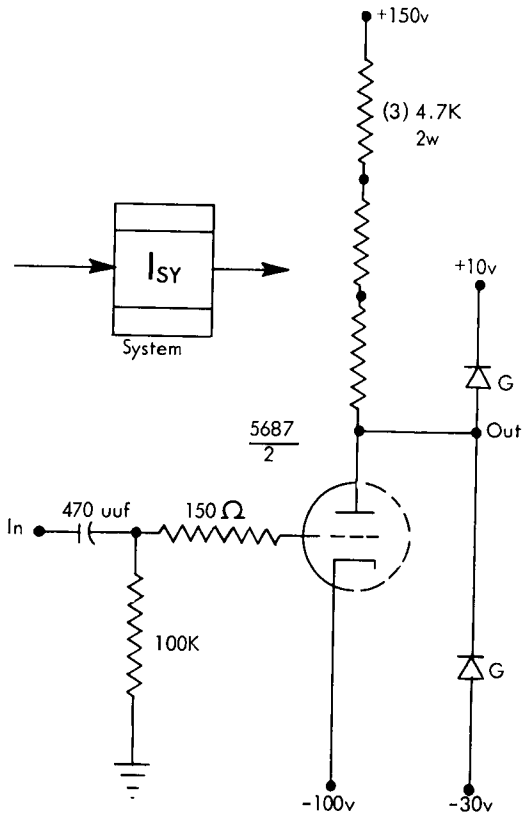


FIGURE B14. INVERTER (I_R)



NOTE 1: Filament center tap is biased at -50v.

FIGURE B15. SYNC INVERTER (I_{SY})

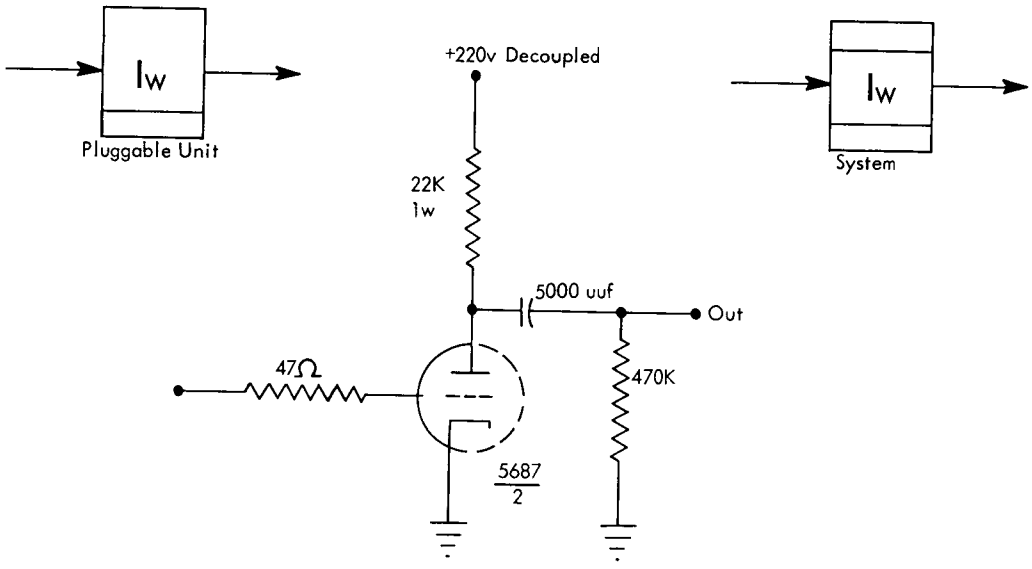


FIGURE B16. WRITE INVERTER (DRUM) (I_W)

2.01.18 Sync Inverter (I_{SY})

Sync inverters, I_{SY}, (Figure B15) are located in each column unit to provide sync pulses of nominal +10v to -30v levels to the delay units. The input to the sync inverter is RC-coupled for setting the level of the input pulse. The tube is normally conducting very heavily but during the pulse, the tube becomes cut-off. When the tube is again made to conduct, the heavy conduction through the tube enables the output voltage to fall very rapidly; the fast fall is the important characteristic of the sync pulse. The diodes on the output keep the signal output within nominal limits.

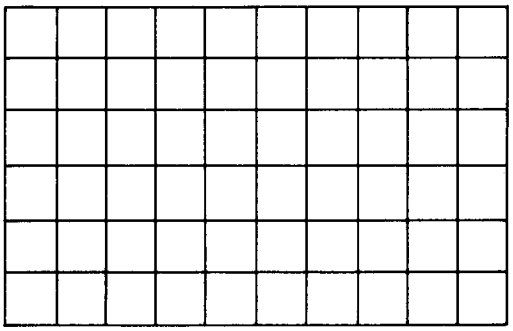
2.01.19 Pull-Over Inverter (I_T)

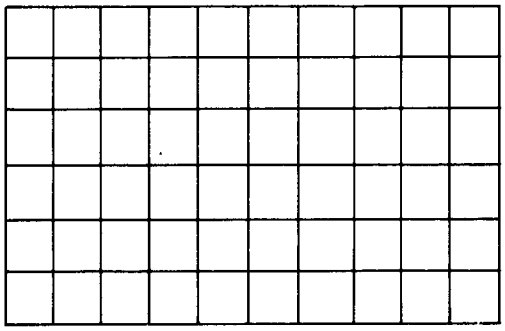
This component was assigned to 701 electrostatic memory and is not used now.

2.01.20 Write Inverter (I_W)

The 701 drum system uses the circuit I_W (Figure B16) for writing information. This system of writing is used instead of a cathode follower (as is used for writing the timing track) so that damage to the write coil does not result from loss of bias in the circuit.

The sequence of operation is as follows: Normally, the tube is cut off, and the capacitor is charged to +150 volts. The circuit is conditioned to write by connecting the output to the write coil. When a pulse of about 1.5 usec duration arrives on the grid, the tube conducts, discharging the capacitor through the tube and through the write coil. The impedance of the coil is much less than 470K, so that practically all of the discharge current flows through the coil. The discharge current is initially about 350 milliamperes, and because the discharge path has a time constant of about three microseconds, the current is between 200 and 250 milliamperes at the time that the tube is again cut off. Then, the capacitor begins to charge again through the coil and through the plate load resistor of the tube but because this resistor is much larger than the dynamic resistance of the tube during discharge time, the initial value of charging current is not sufficient to cause writing. This circuit requires about 425 microseconds to fully recover, that is, about 425 microseconds until the capacitor is again charged to +150 volts. A smaller value of parasitic suppression resistor in the grid circuit is used so that grid current during the pulse is not limited as much as if 150 ohms were used.





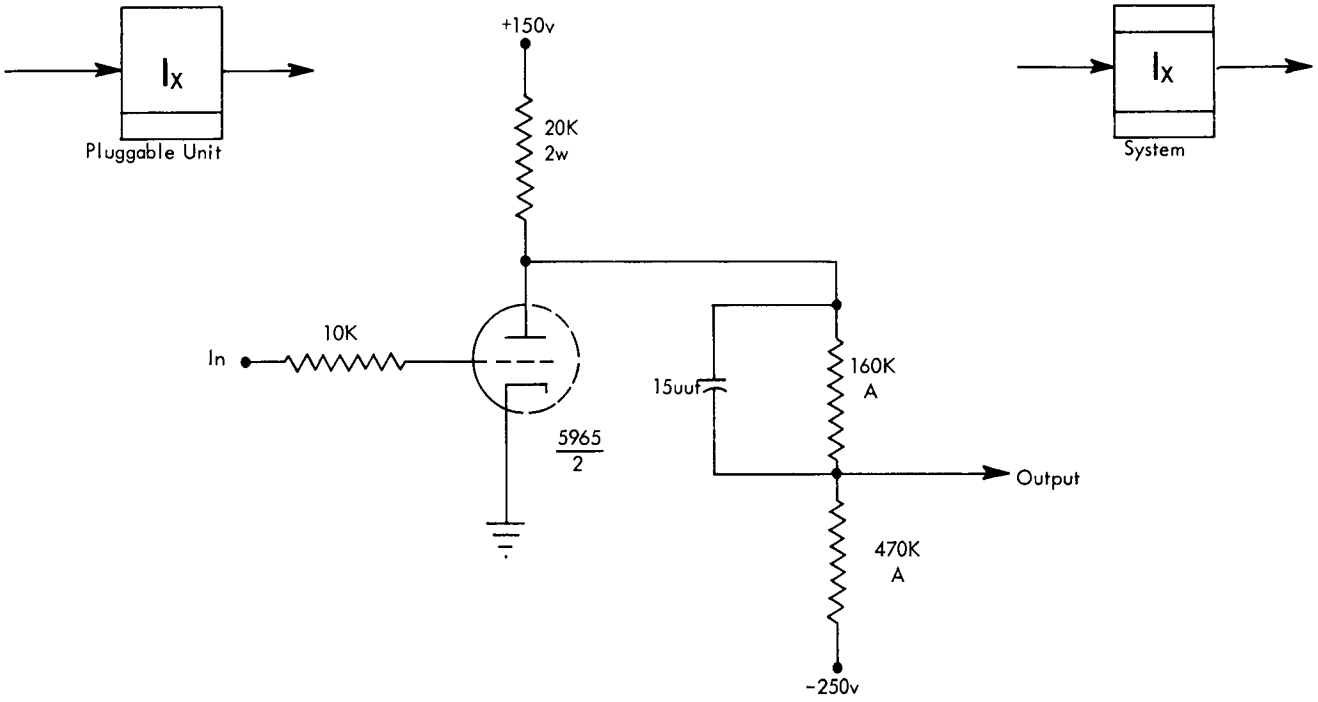


FIGURE B17. INVERTER (I_X)

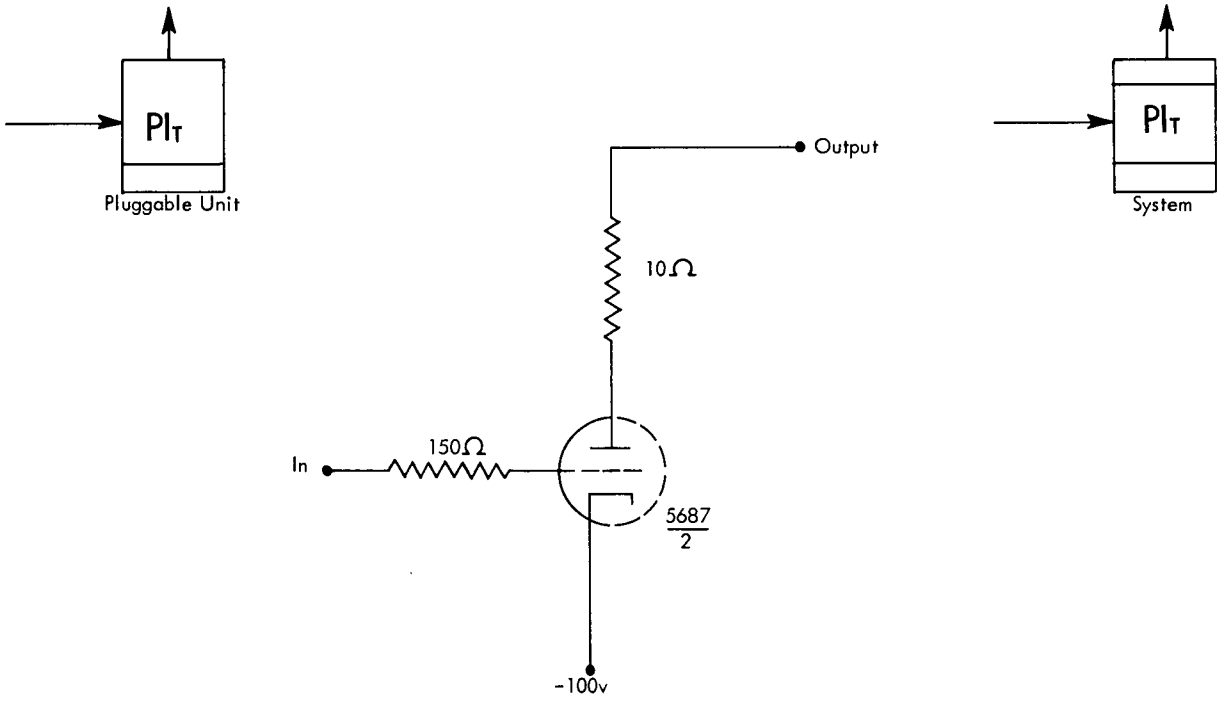


FIGURE B18. INVERTER (PI_T)

2.01.21 Inverter (I_X)

I_X is the symbol for a special inverter circuit (Figure B17) used in the 701 drum-system writing circuits. It resembles a standard inverter, I, except that its plate resistor and divider resistor values have been changed to produce a large output swing. In this way, the output of the following cathode follower is clipped by both catcher diodes. This swing on the grid of the cathode follower when the cathode follower tube is removed should be about +36 volts to -35 volts. This means the plate swing can be about +136 volts to +38 volts.

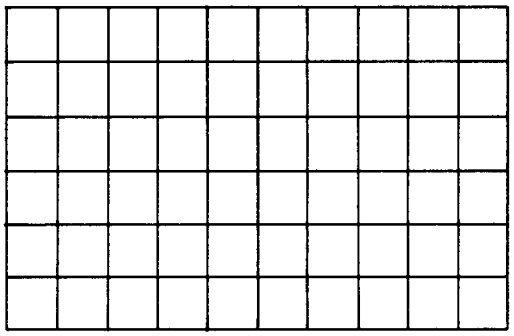
2.01.22 Unassigned

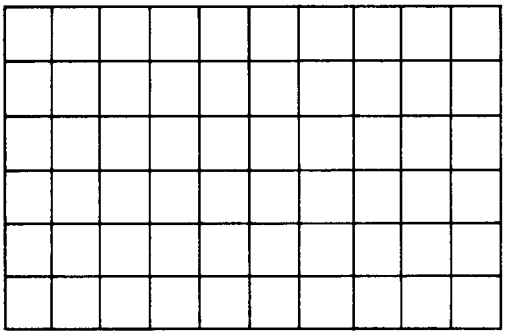
2.01.23 Phase Inverter (PI)

This component was assigned to 701 electrostatic memory and is not used now.

2.01.24 Inverter (PI_T)

The inverter PI_T (Figure B18) is a part of the circuits used to supply current to the moving clutch coil in the tape unit. Three PI_T's are provided in parallel with the two I_R's in the feed, for "stop current" to help switch this accelerating current for a short interval of time. The inverters are fed a positive shift of about 140 volts from a -140v level from a differentiating circuit. This pulse returns to -100 volts through a circuit with a time constant of about two milliseconds. When this pulse reaches about -100 volts, the three PI_T's conduct and lower the impedance of the circuit through which the accelerating current must flow. That is, the action of bringing the three PI_T's to zero bias condition from a cut-off condition causes the plate voltage of the tube to be lowered. Because the opposite end of the coil is connected to a cathode follower, that voltage will not change appreciably; therefore, the overall voltage across the coil is increased, and more current flows through the coil.





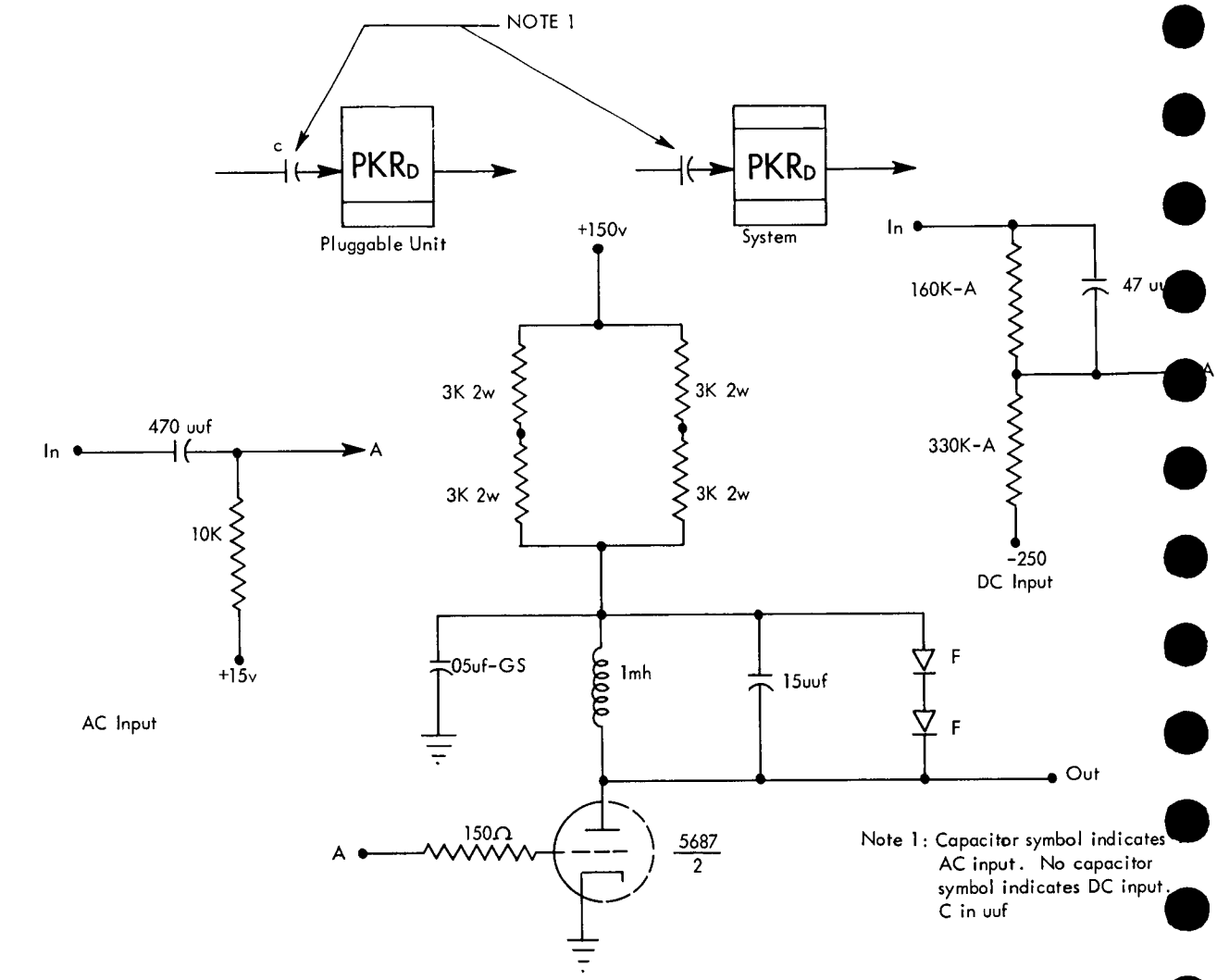


FIGURE B19. PEAKER (PKR_D)

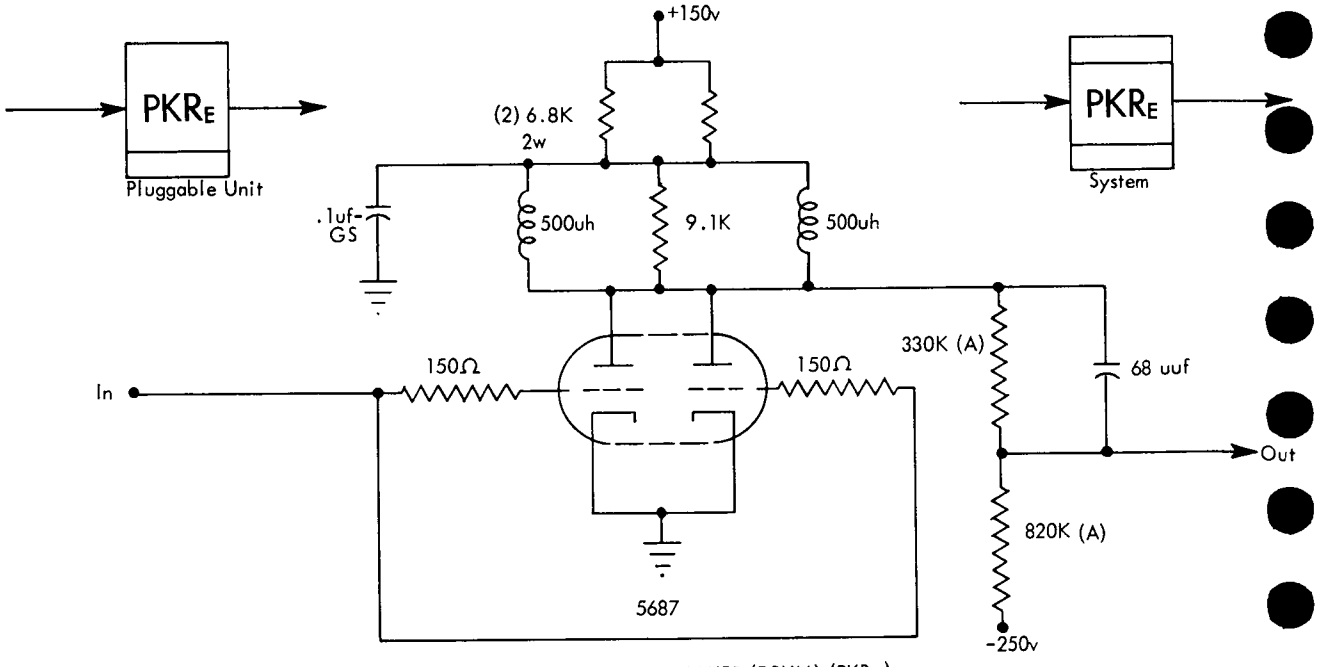


FIGURE B20. READ SAMPLE PEAKER (DRUM) (PKR_E)

Principles of Peaker Circuit Operation

The 700 series systems use many circuits designated peaker, PKR. A comprehensive coverage of peaker operation is given in section 2.15.00, Book A.

2.01.25 Sample Read-In Peaker (PKR_A)

This component was assigned to 701 electrostatic memory and is not used now.

2.01.26 Left or Right Sample Peaker (PKR_B)

This component was assigned to 701 electrostatic memory and is not used now.

2.01.27 Dot Generator Peaker (PKR_C)

This component was assigned to 701 electrostatic memory and is not used now.

2.01.28 Bit Sweep Start Peaker (PKR_D)

This component shown in Figure B19, is used to deliver sharp one-usec pulses to a heavily capacitive load. The capacitor shunting the peaking coil produces the correct output pulse width.

2.01.29 Read-Sample Peaker (Drum) (PKR_E)

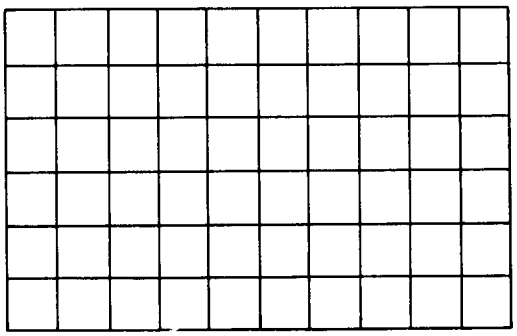
PKR_E (Figure B20) generates the read sample pulse (slightly less than one microsecond wide at its base). No additional capacitor is added in the plate circuit, because the distributed capacitance of the coils, wiring, and so on, is sufficient to obtain the desired pulse width. Two tubes are used to give the pulse a greater amplitude.

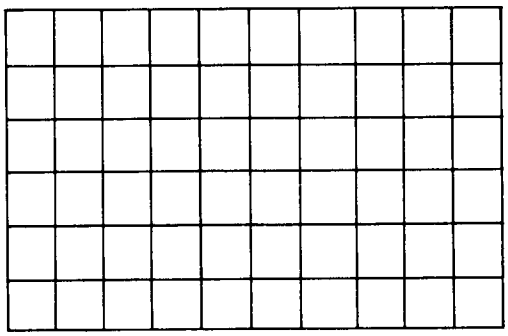
2.01.30 Inverter (I_{SYA})

This component was assigned to the 701 field tester only (section 2.01.11, Book B).

2.01.31 Inverter (I_{CLA})

This component was assigned to the 701 field tester only (section 2.01.11, Book B).





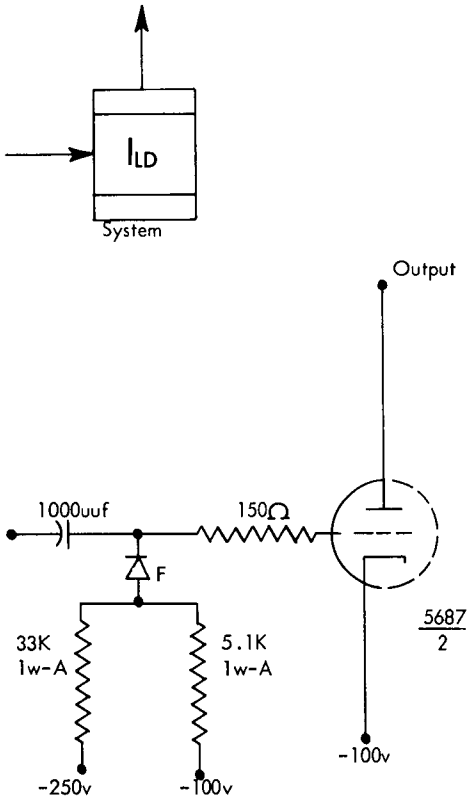


FIGURE B21. LINE DISCHARGE INVERTER I_{LD}

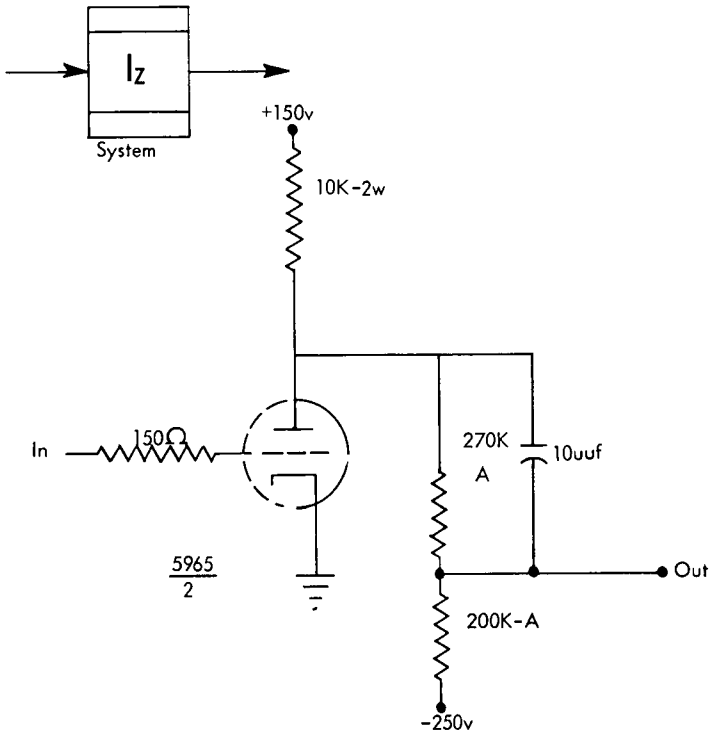


FIGURE B22. INVERTER (I_Z)

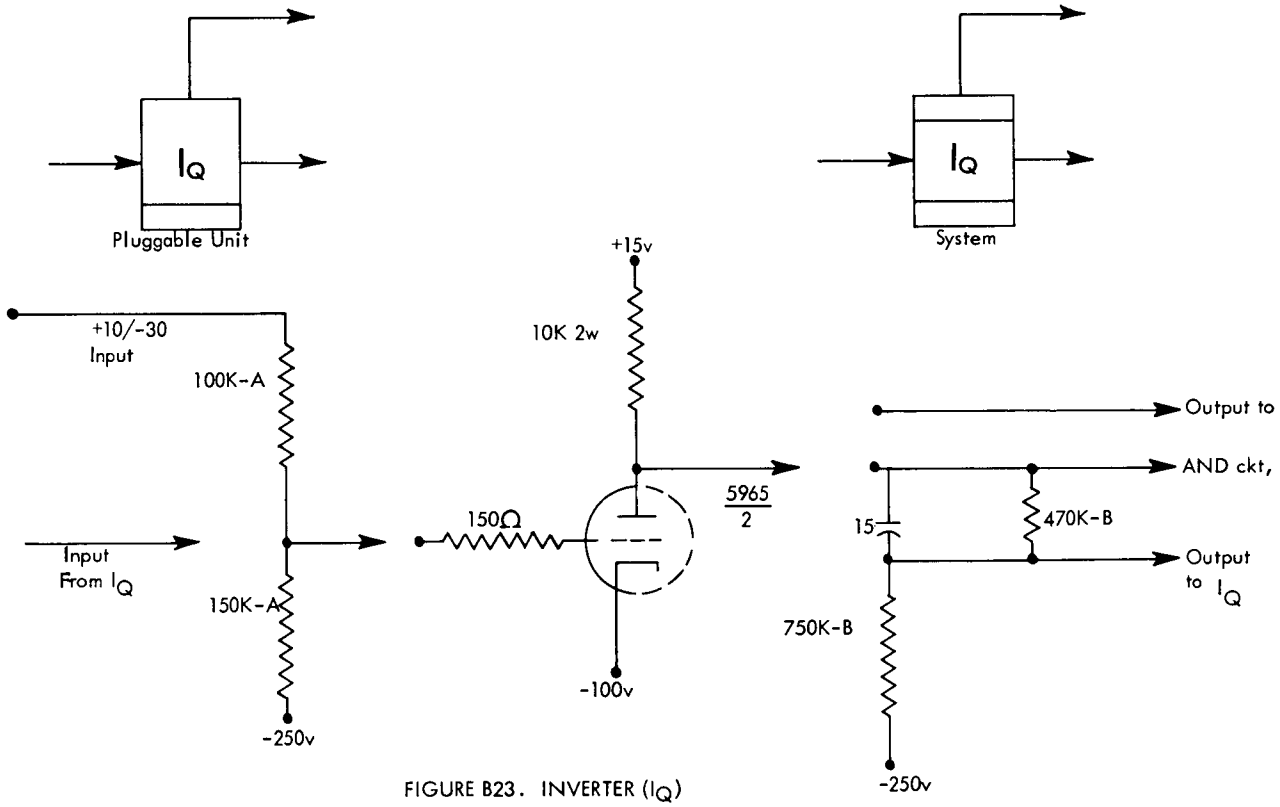


FIGURE B23. INVERTER (I_Q)

2.01.32 Line Discharge Inverter (I_{LD})

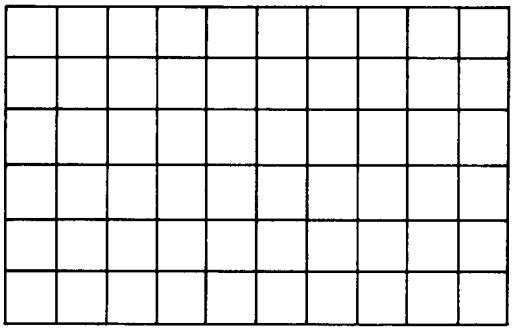
The I_{LD} (Figure B21) operates in conjunction with a cathode follower. The output of the cathode follower follows the input, if the input goes positive. When the input goes negative, line capacity sometimes is so great that the input falls far more rapidly than the output. To pull these lines down, the line discharge inverter is used. The plate load for the inverter is the line being operated on. Its cathode is returned to -100v. The voltage divider network in the grid holds the tube below cut-off normally. When a positive signal is applied to the grid, the tube conducts, offering a fast discharge path to the line capacity. This must coincide, however, with a negative shift to the grids of the cathode followers holding the line up. This inverter arrangement greatly improves the fall time of heavily loaded lines. It is used to help drop some of the hold lines to the microsecond-delay units.

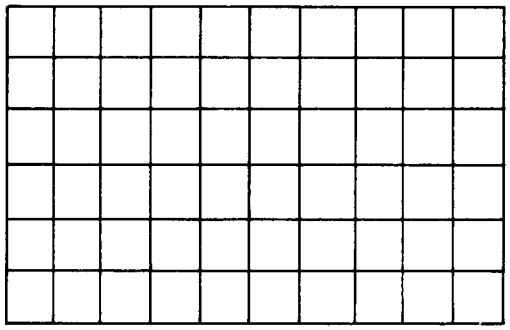
2.01.33 Inverter (I_Z)

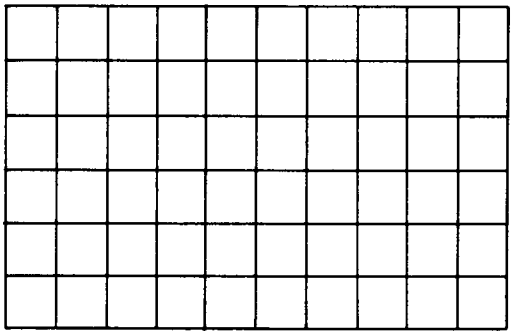
Operation of the I_Z (Figure B22) is like that of the slow inverter I_S. The output is a -100v/-130v signal for use in the CRT output recorder.

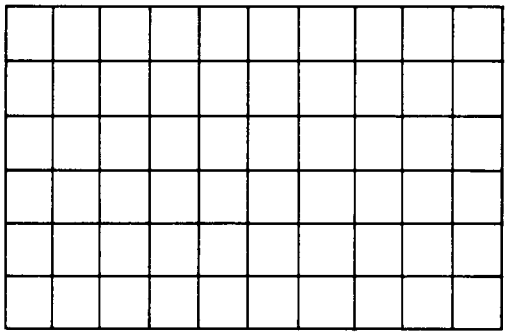
2.01.34 Inverter (I_Q)

The inverter I_Q (Figure B23) is always used in pairs. The first stage receives a normal level input and drives an AND circuit and the second I_Q. The second tube delivers an output to an AND circuit in phase with the input. The I_Q is basically a level restorer with the plate operating at standard signal level and the cathode connected to a -100v supply. Otherwise, operation of the I_Q is like that of the I_S.









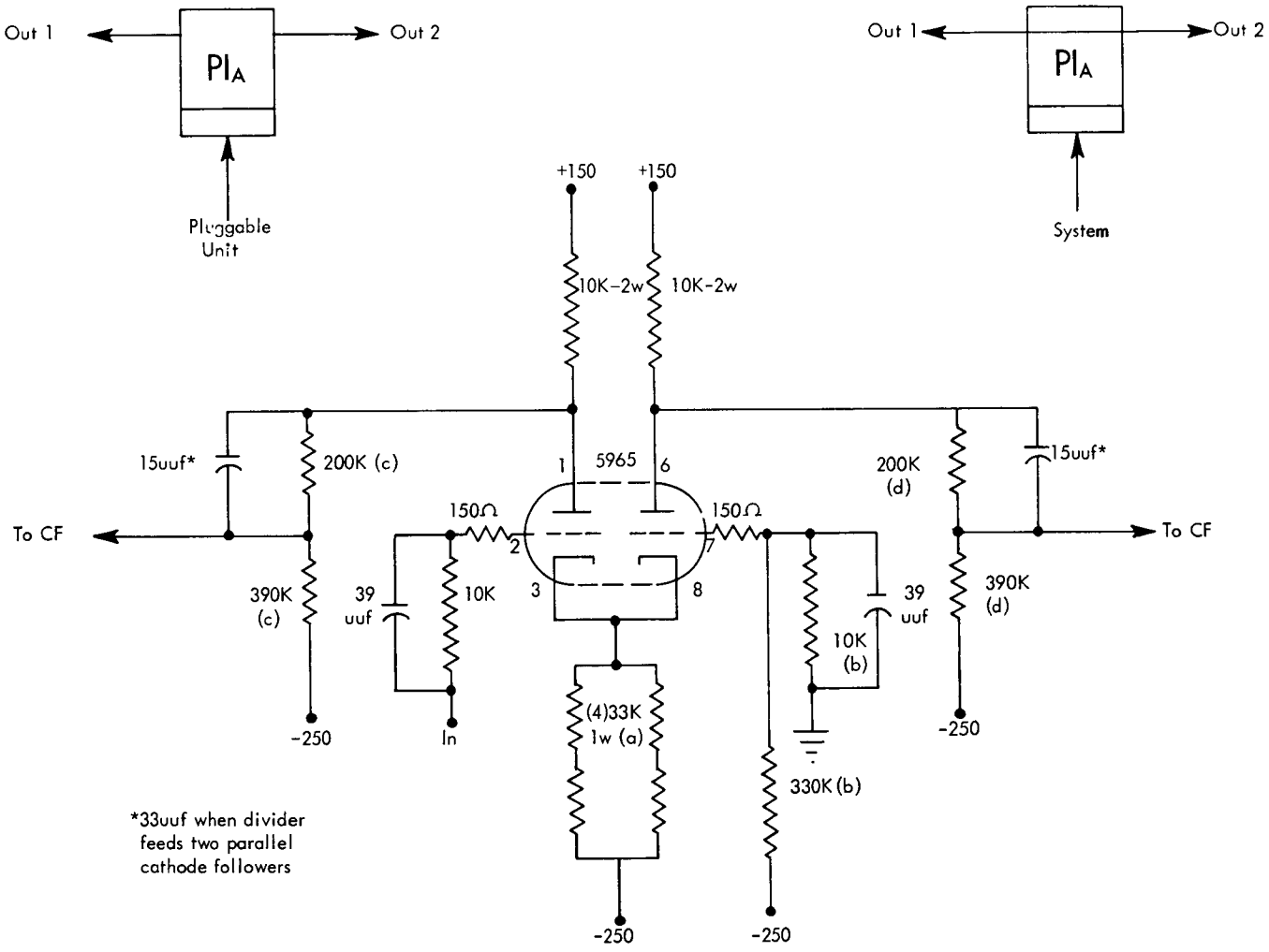


FIGURE B24. PHASE INVERTER AMPLIFIER (PI_A)

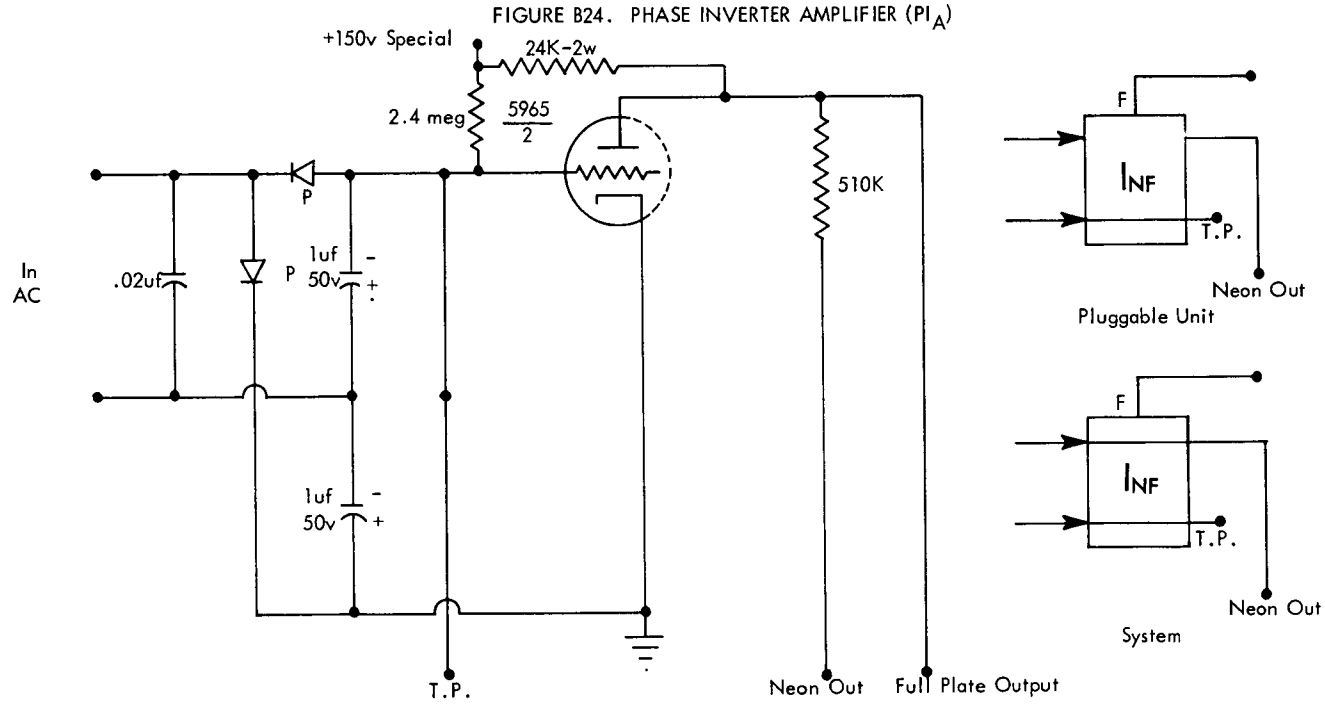


FIGURE B25. INVERTER, NEON, FILAMENT DETECTION (I_{NF})

2.01.35 Phase Inverter Amplifier (PI_A)

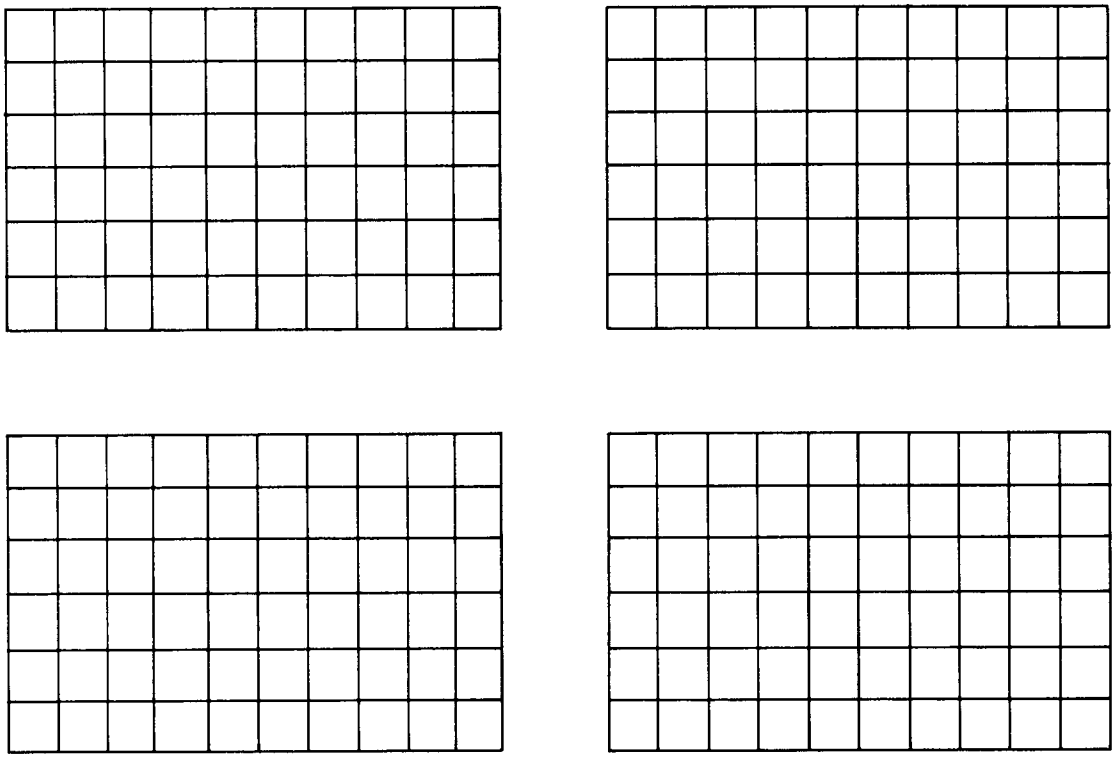
The PI_A (Figure B24) is similar in operation to the A_S (Figure B47) with the exception that a plate load resistor appears in the left half. An additional output is taken from the left plate providing an output inverted from the input. Thus, the PI_A serves as both an inverter and an amplifier while causing no additional delay.

2.01.36 Inverter (Open Filament Detection) (I_{NF})

This component (Figure B25) is used in the open-filament-detection circuit. It takes an AC input from an unbalanced condition in the bridge circuit created by a burned out filament in a tube-half. This signal is then amplified to light the display neons.

2.01.37 Inverter (I_{NE})

The inverter I_{NE} is a modified version of the inverter I_N (section 2.01.13, Book B) using a 5965 in place of a 5844. I_{NE} is an I_N (X') without the .01-uf capacitor shunting the input.



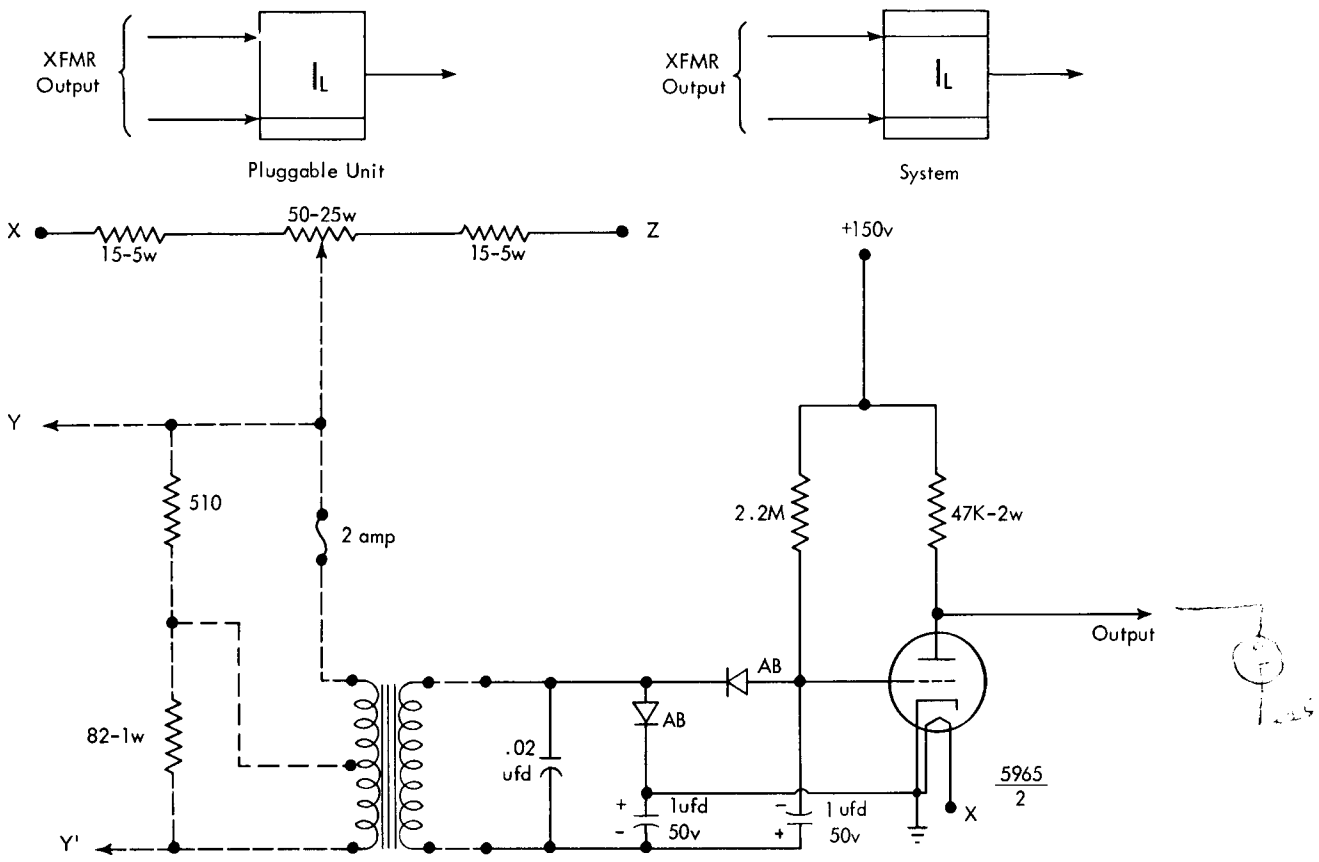


FIGURE B26. FILAMENT DETECTION NEON INVERTER

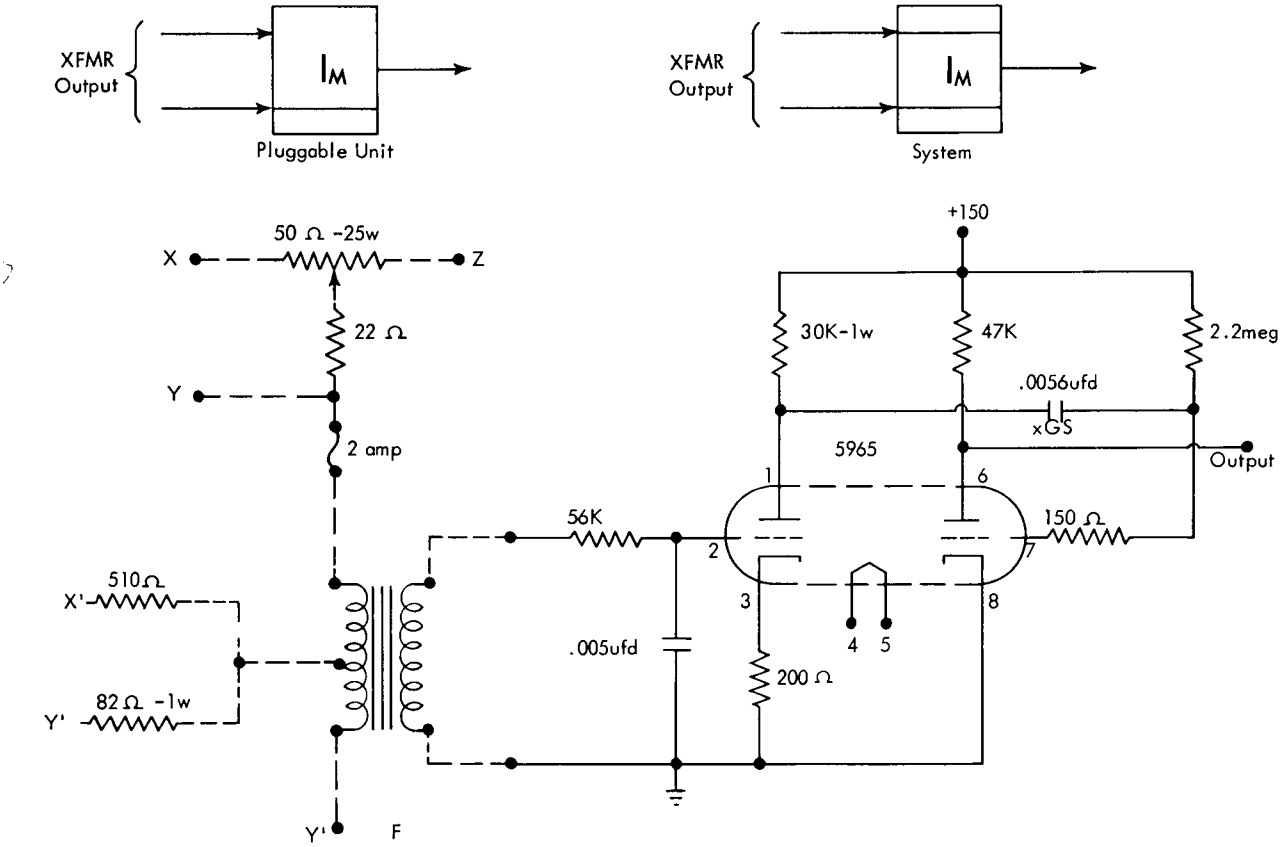


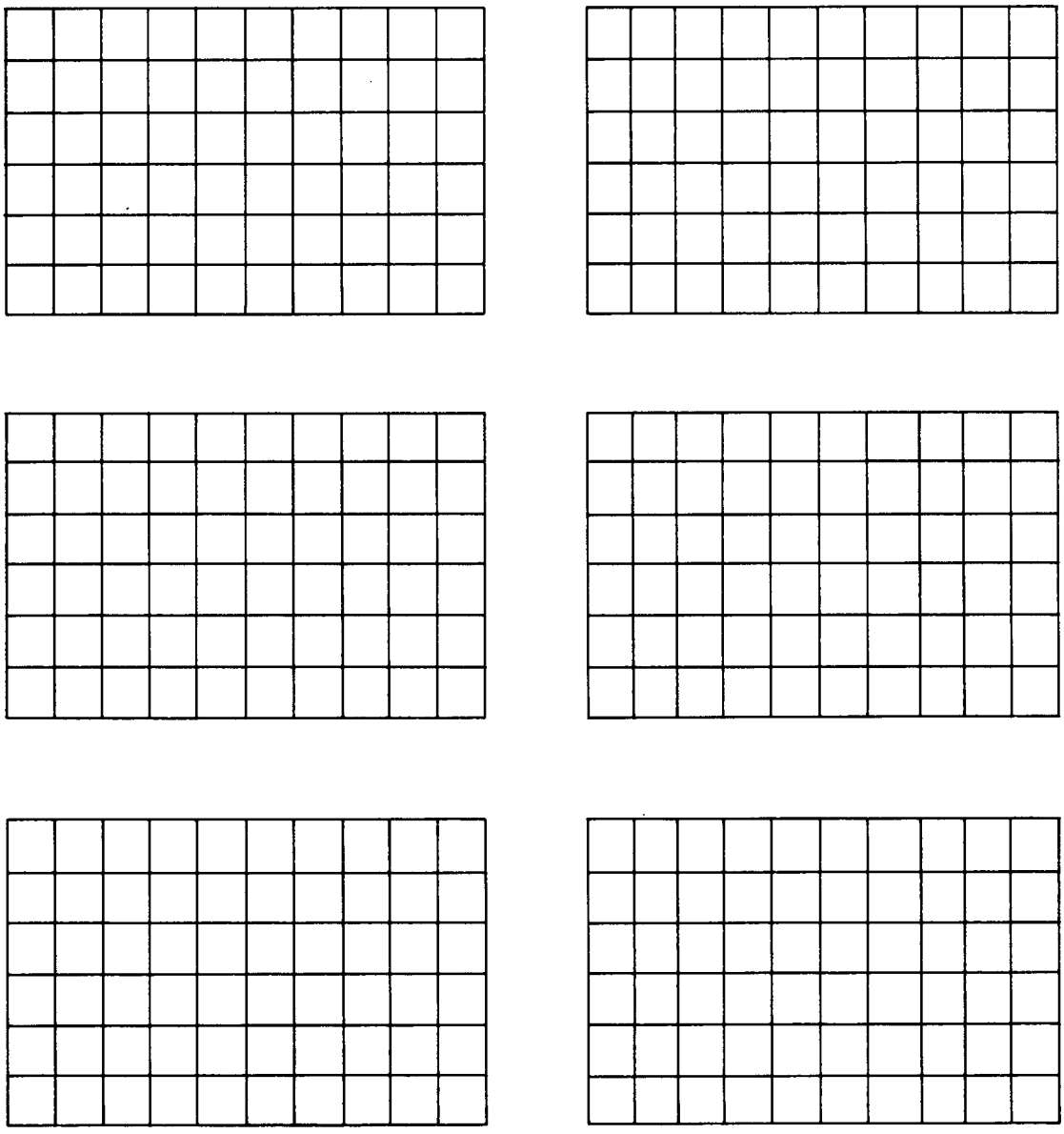
FIGURE B27. FILAMENT DETECTION NEON INVERTER

2.01.38 Filament Detection Neon Inverter (I_L)

The function of this component (Figure B26) is identical to that of the I_{NF} (section 2.01.36, Book B).

2.01.39 Filament Detection Neon Inverter (I_M)

The function of this component (Figure B27) is identical to that of the I_{NF} (section 2.01.36, Book B).



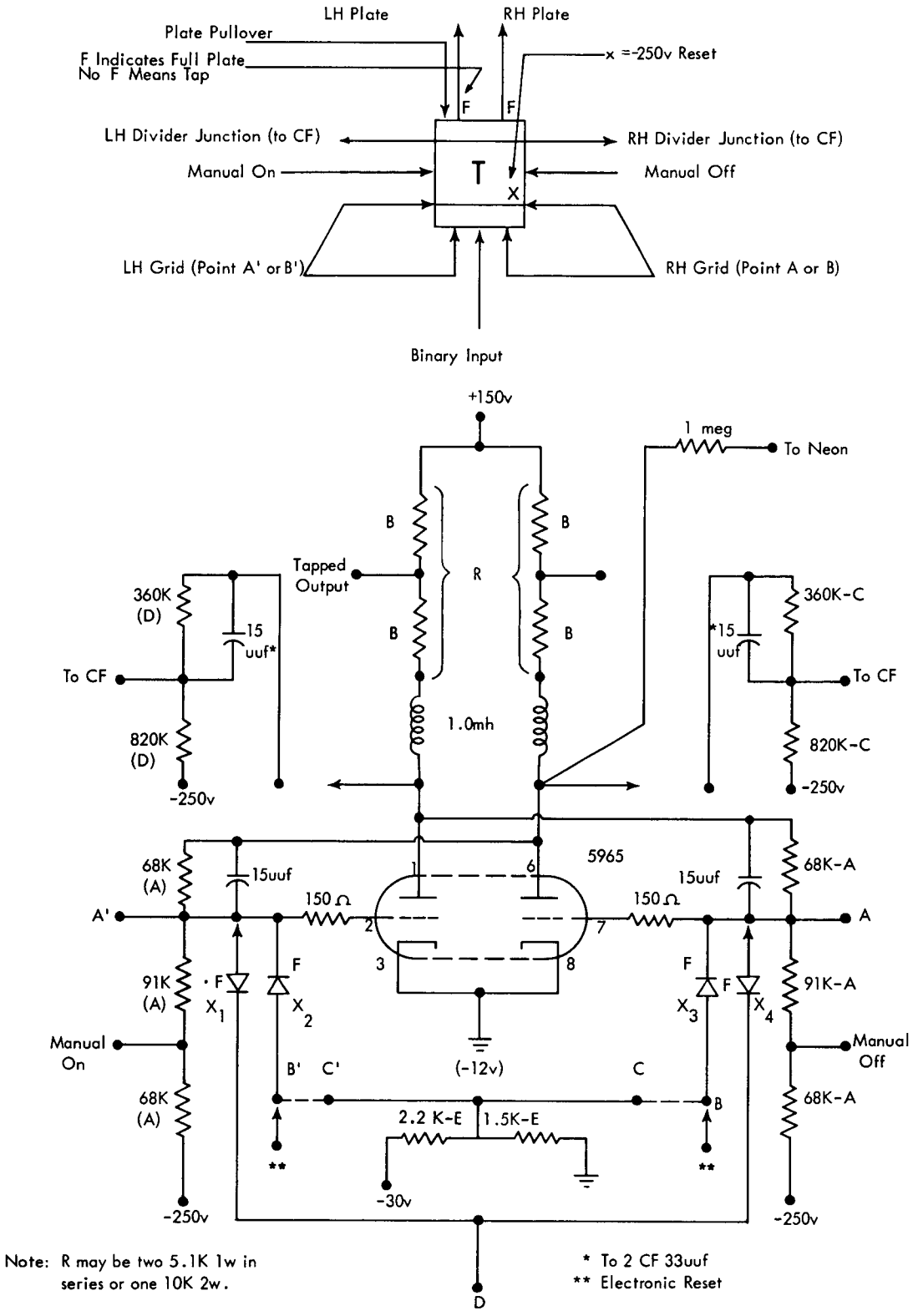


FIGURE B28. HIGH-SPEED TRIGGER (T)

2.02.00 TRIGGERS

2.02.01 High-Speed Trigger (T)

The operation of the standard high-speed trigger is discussed in section 2.06.00, Book A.

Normally, the tube-half with the lower pin numbers is the left side, as shown in Figure B28. In some triggers of the machine, the left side of the circuit is wired to the high-numbered pins. This difference in wiring does not affect the logic of the circuit, but it is important in trouble-shooting a trigger. To indicate that a trigger is wired in such a reversed manner, an R is placed above each corresponding pluggable unit or systems block.

Inputs to a High-Speed Trigger

In Figure B29 are shown six inputs to a trigger circuit. These are explained in section 2.06.06, Book A.

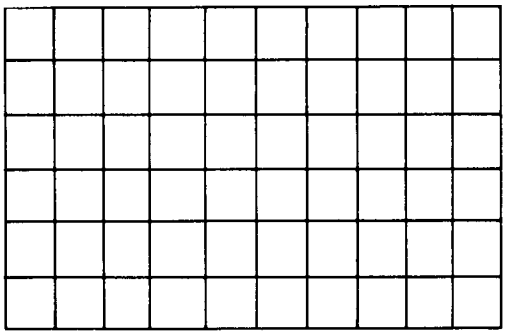
Input Requirements for the Trigger

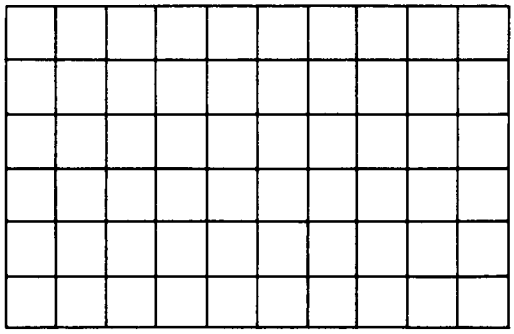
The following are minimum requirements for flipping a trigger with various inputs:

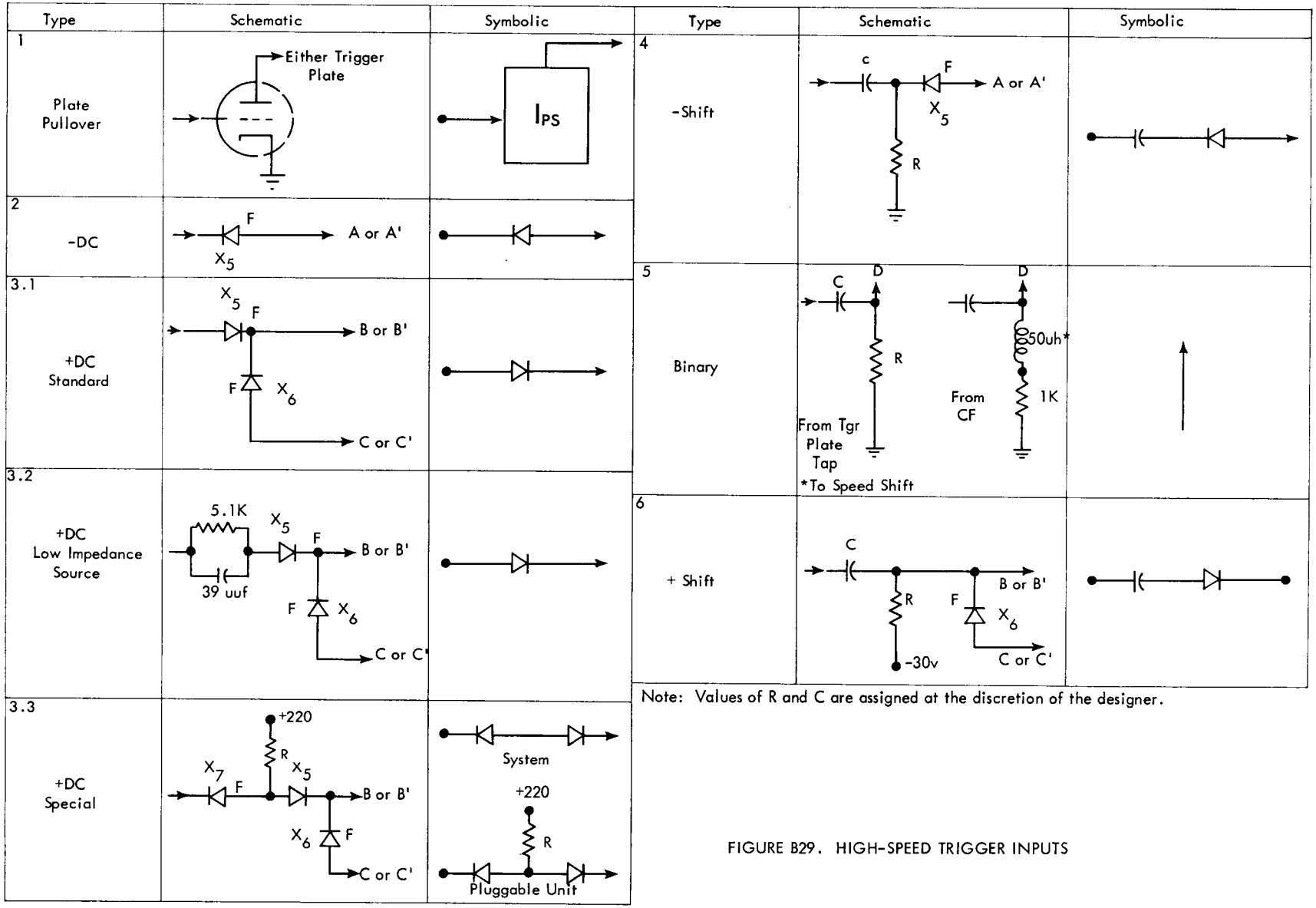
Plate pull-over: standard inverter input.
+DC: lower level, -20 to -30 volts; upper level, +5 to +15 volts.
-DC: lower level, -15 to -30 volts; upper level, +5 to +15 volts.
-Shift: 20v step, 35 volts/usec minimum slope.
Binary input: 0-2 megacycles, 20v step, 30 volts/usec minimum slope.

Power Reset

The triggers may be wired to be reset whenever a power reset is given the machine. A power reset opens a special -250v reset line in each voltage section. If a grid divider resistor is wired to this line instead of to the normal -250v line, the breaking of the reset line upon a power reset produces a positive shift at the corresponding grid to flip the trigger (if the grid was initially cut-off). Connection of the reset line to the right grid divider return allows the trigger to be reset off upon power reset. The -250v reset line is the same as a normal -250v line except for the relay points that open the line and an isolation resistor placed in series with the contacts. The voltage rise across this resistor may cause the voltage on the -250v reset line to be as high as -245 volts.







Note: Values of R and C are assigned at the discretion of the designer.

FIGURE B29. HIGH-SPEED TRIGGER INPUTS

Voltage Levels in the Trigger

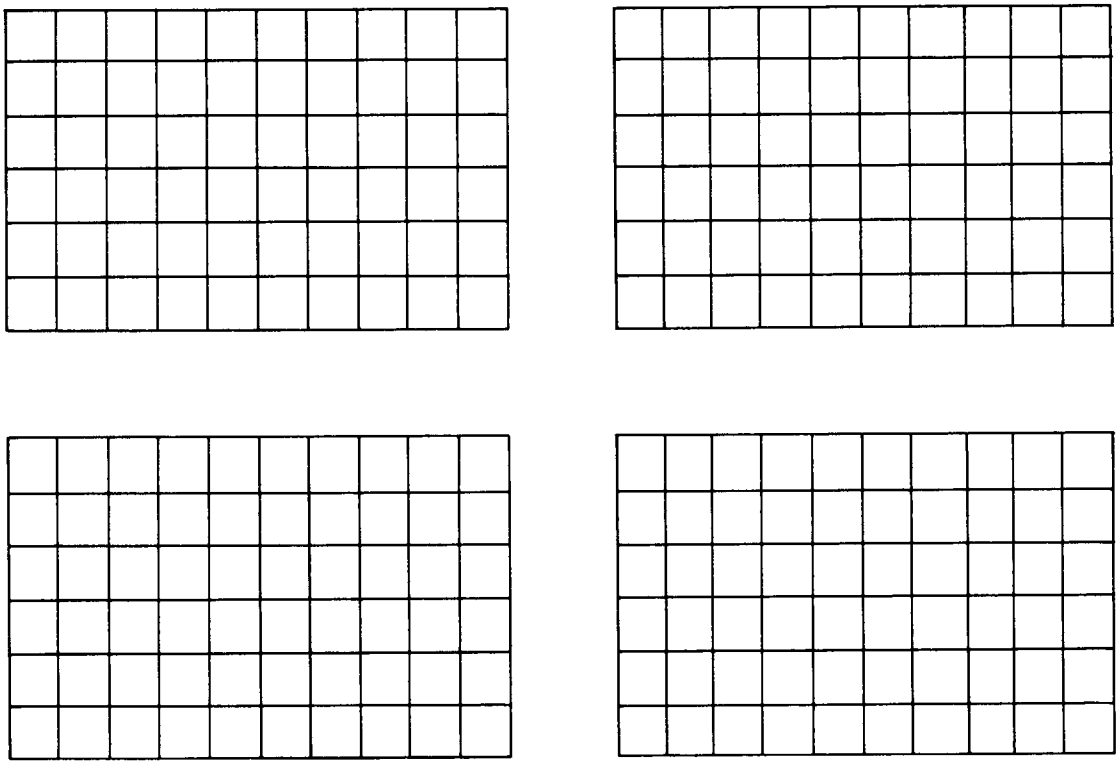
The following are nominal voltage levels in a high-speed trigger:

Full plate: +52 and +127 (divider connected).
Tapped plate: +101 to +139 (divider connected).
Divider output: -40 to +12.
Grid: Tends to go down to -38 but is clamped by diode at -12.
Tends to go up to +12 but is grid-clamped at about ground.
Tweak points: -143 to -152.

When the voltage divider is not connected to the plate output, the upper plate level is +150 and the lower level is only a few volts higher than that given. A trigger may produce a one-tenth microsecond delay; it gives nominal rise and fall times of 0.3 microsecond.

Special Features

To indicate the state of a trigger, a neon is usually connected through a one-megohm resistor to the right plate. The neon is mounted on the panel and is returned to +15 volts. It will be lit when the trigger is on. Some triggers have neons taken off the left plate, but they are returned to +150 volts and still light when the trigger is on. The neon connection is not shown on block diagrams, but color coding on the bulb indicates the tube to which it corresponds. A trigger circuit always uses the half-tubes in the same envelope.



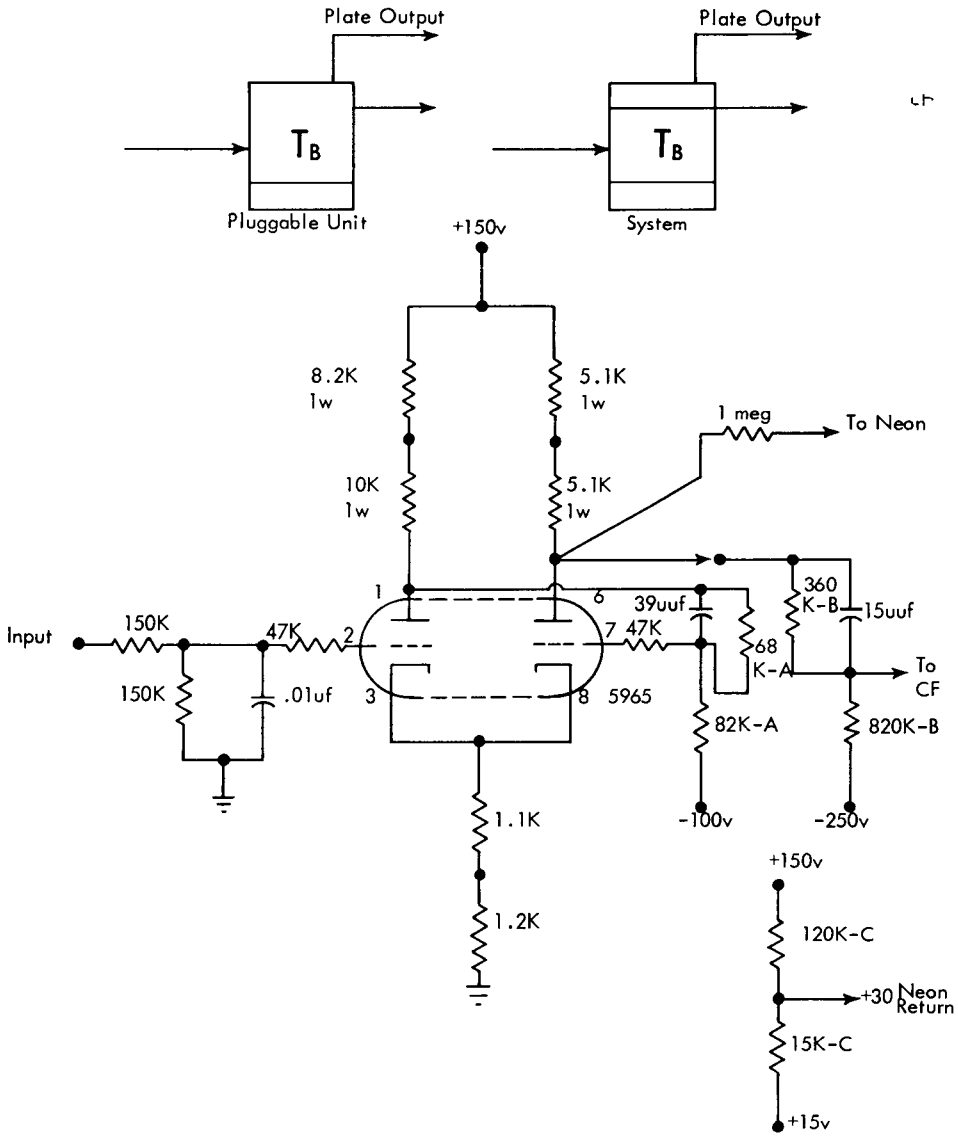


FIGURE B30. SCHMITT TRIGGER (T_B)

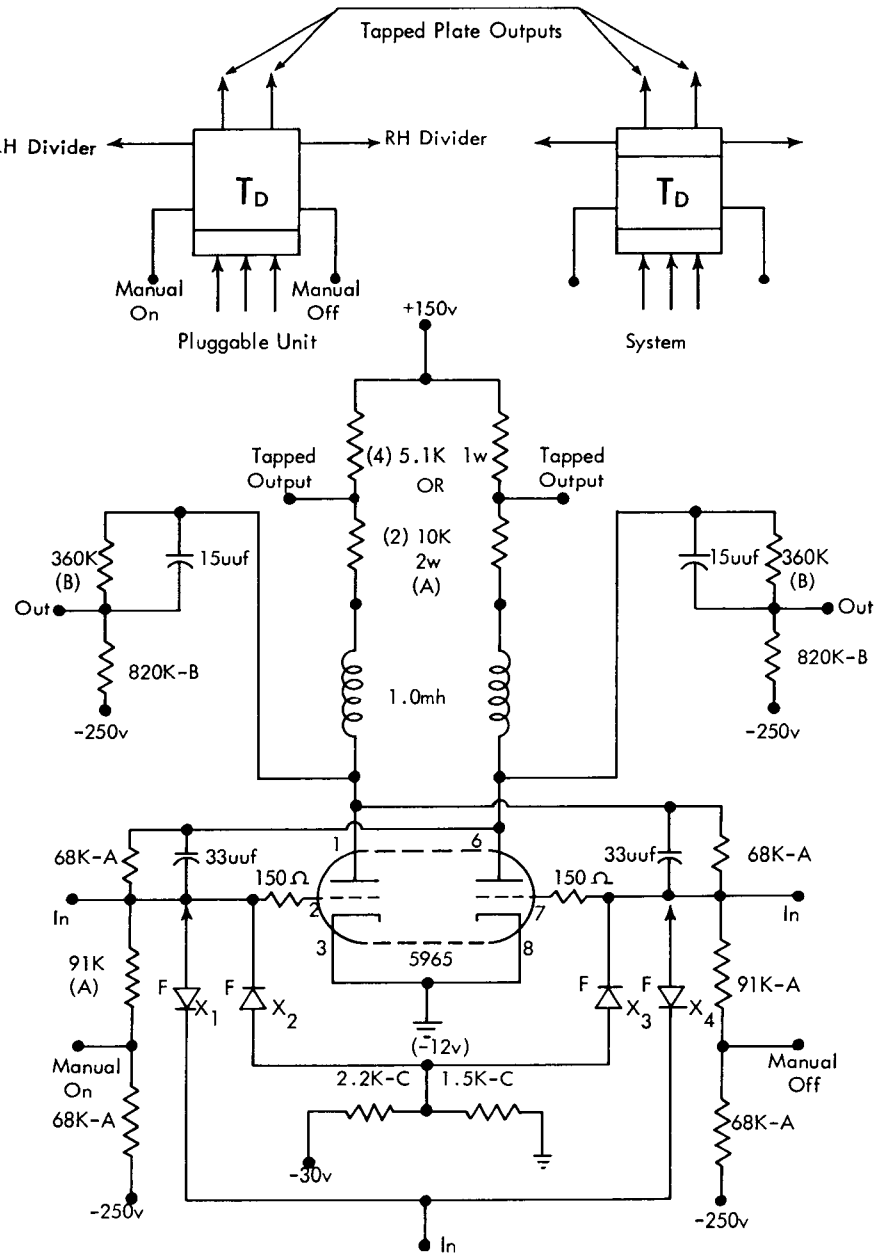


FIGURE B31. TRIGGER (DRUM) (T_D)

2.02.02 Trigger (T_A)

This component was assigned to 701 electrostatic memory and is not used now.

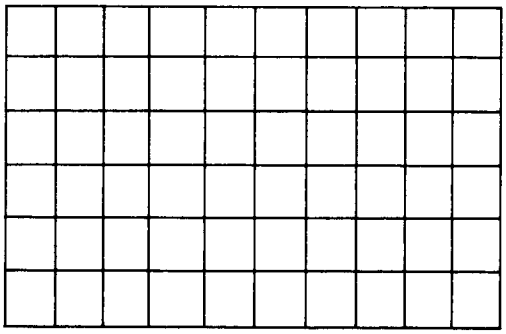
2.02.03 Schmitt Trigger (T_B)

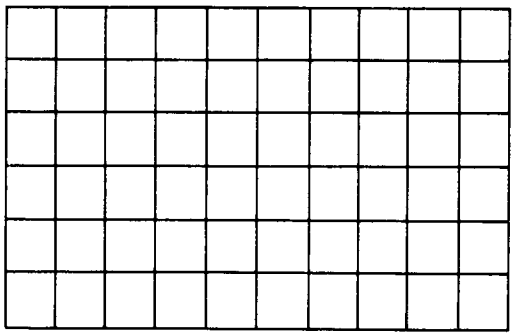
T_B is the symbol for the Schmitt trigger (Figure B30) used as a key trigger to produce gates for as long as the input key is depressed. When the key is not depressed, the input is held to ground by the resistor connected to the left grid and also by a resistor connected to the key. Under these conditions, the left tube is cut off, and the right tube is operating at about zero bias, drawing a slight amount of grid current. The cathode and right grid are at about +18 volts, the left grid at zero volts, the left plate at about +120 volts, the plate-to-right-grid divider output about +20 volts, the right plate at about +70 volts, and the output at about -26 volts.

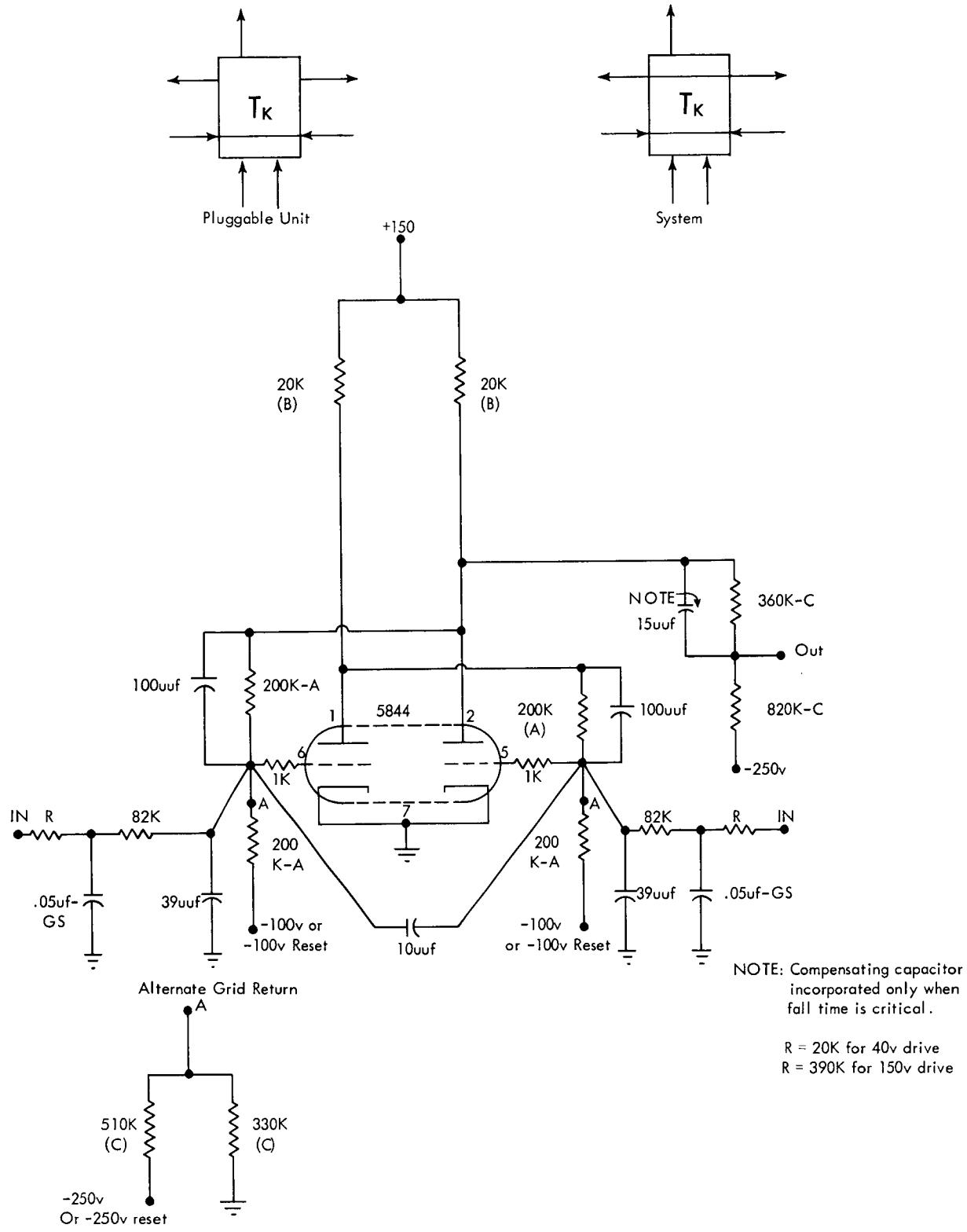
When the key is depressed, the left grid is pulled up to a positive value (tends to go to about +70 volts with tube removed) and thus causes the left tube to conduct. The cathode and left grid voltage are about +13, but the left plate voltage falls to about +45, the right grid about -20, the right plate +145, and output about +14 volts. In this state, the right tube is cut off while the left tube is conducting hard. The junction between the left grid resistor and the 150K input resistor is about +36 volts. This circuit gives a smooth electronic gate output whenever the key is held down. It performs the same functions as the key trigger circuit (Figure B32) but it requires only one input wire.

2.02.04 Trigger (Drum) (T_D)

The special trigger circuit T_D (Figure B31) is used in the drum counter. It is identical to a standard high-speed trigger, except that the plate-to-grid compensation capacitor is 33 uuf instead of 15. This value of capacitance causes the divider to apply a larger signal to the grid to begin the regenerative action. This change was necessary to improve the reliability of the 11-stage binary counter. This counter now operates with relatively large changes in the +150v plate supply. The change increases slightly the rise and fall times of the output.







NOTE: Compensating capacitor incorporated only when fall time is critical.

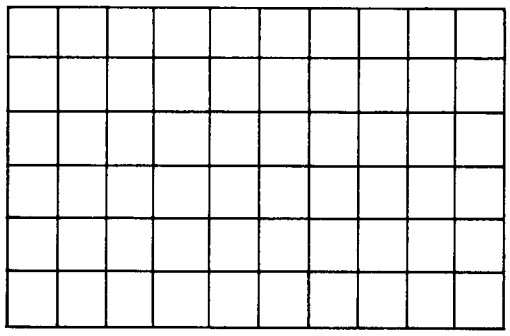
R = 20K for 40v drive
R = 390K for 150v drive

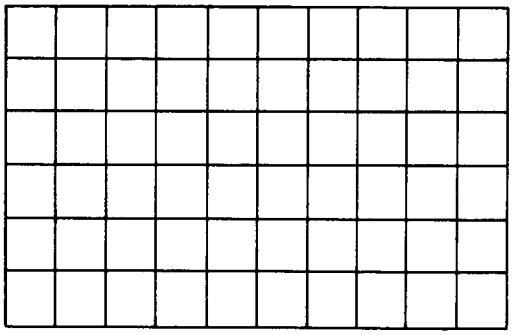
FIGURE B32. KEY TRIGGER (T_K)

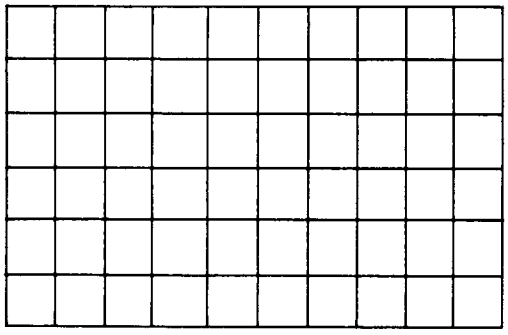
2.02.05 Key Trigger (T_K)

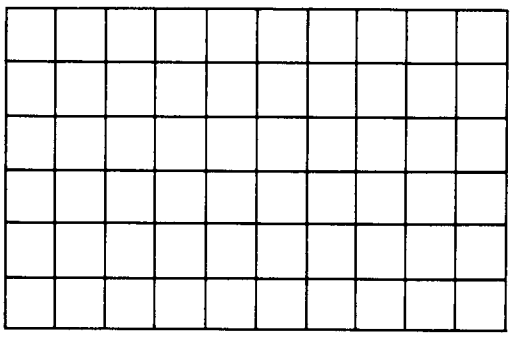
T_K is the symbol for a key trigger (Figure B32). Key triggers are used primarily in the operator's-panel circuits and in the input/output circuits for producing pulses with smooth wave fronts, from input pulses that often contain ragged wave fronts. Circuit breakers in series with the reading brushes, other card machine circuit breakers and switches on the operator's panel feed the key triggers. Operation of these switching devices tends to produce transients because of imperfect contact or switch bounce. The key trigger is operated by feeding a driving voltage through a series 10K resistor to one or the other of the grid inputs. The driving voltage from the operator's panel circuits is +150 volts, while +40 volts is the driving voltage in the distributor. The 10K series resistor, placed as near the switching device as practical, isolates the switching transients from the line or the line transients from the key trigger.

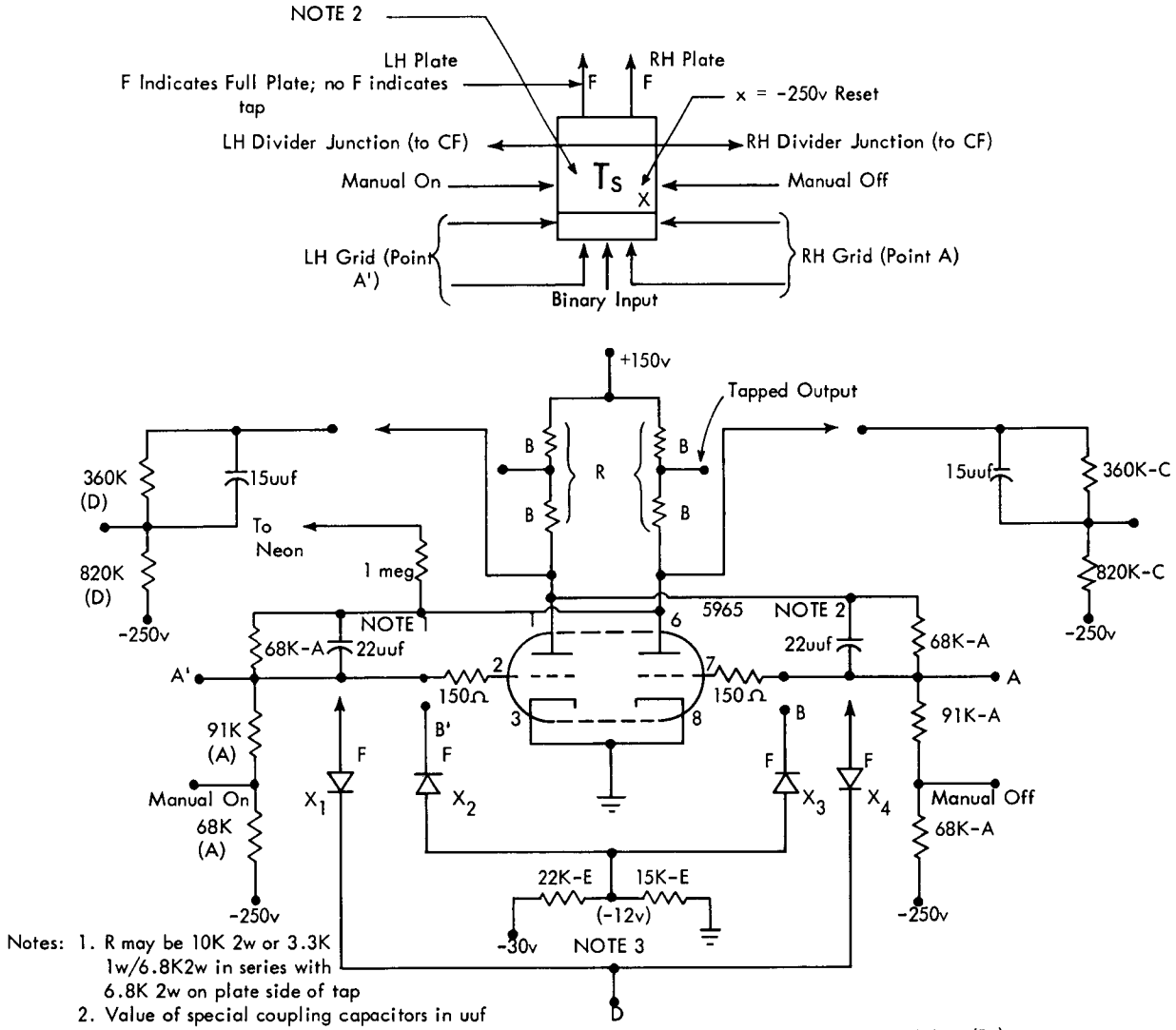
The input to the key trigger is a double integrating circuit, composed of two series resistors and two shunt capacitors. Integrating action helps produce a smooth pulse which promotes positive triggering action if the input pulse remains long enough; therefore, the integrators help to prevent transients from affecting the key trigger. The coupling capacitor between grids also desensitizes the key trigger to transients. A neon lamp may be connected to either plate, as in the high-speed trigger circuit. Inputs are shown drawn at the lower corners of the block, either from the side or from the bottom. The plate voltage swing is from about +135 to +30 volts and the grid voltage swing is from ground to about -30 volts. The rise time of the key trigger is about nine microseconds; the fall time is about 0.6 microsecond.





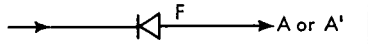
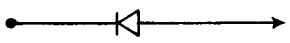
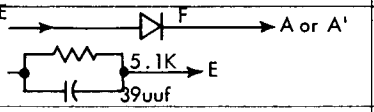
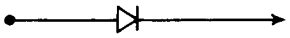
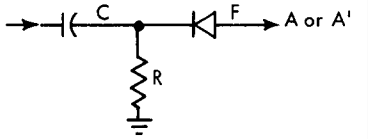
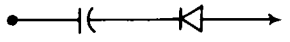
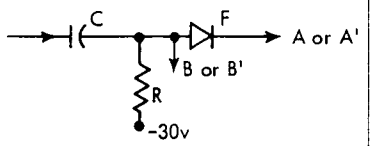
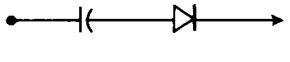
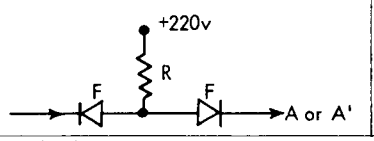
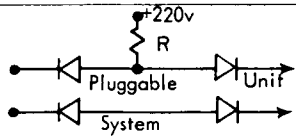






Notes: 1. R may be 10K 2w or 3.3K 1w/6.8K2w in series with 6.8K 2w on plate side of tap
2. Value of special coupling capacitors in uuf
3. -12v divider is used when T_S is used as a counter or driven by another trigger

FIGURE B33. SLOW-SPEED TRIGGER (T_S)

Type	Schematic	Symbolic
-DC		
+DC Standard * If low impedance source is used, insert limiting circuit at E.		
-Shift		
+ Shift		
+DC Special		

Note: Values of R and C are assigned at the discretion of the designer.

FIGURE B34. SLOW-SPEED TRIGGER INPUTS

2.02.06 Slow-Speed Trigger (T_S)

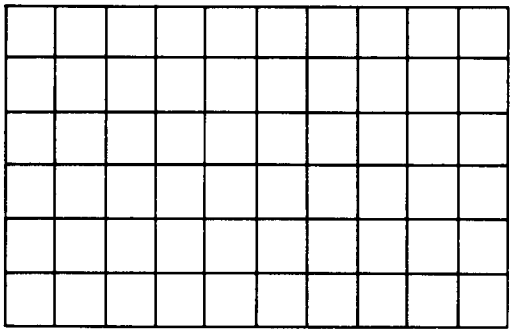
Applications for trigger circuits that do not require the high-speed response of the high-speed trigger use a less expensive circuit, the slow-speed trigger, T_S (Figure B33). Except for the characteristics described below, the slow trigger is identical to the high-speed trigger (Figure B26). The slow trigger has a rise time of about 0.5 microsecond and fall time of about 0.3 microsecond. Three changes are made to produce a slow trigger from a trigger. The plate peaking coils are removed, the plate-to-grid compensation capacitance is increased to 22 uuf, and the clamp diodes on the grids are removed (except for binary applications). These changes produce a savings in components at the expense of slower response.

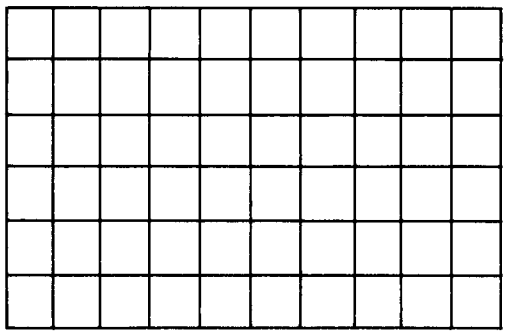
Inputs and Outputs of a Slow Trigger

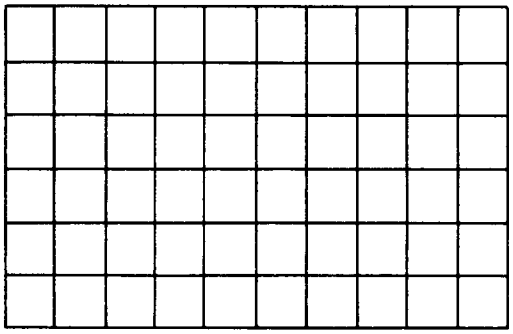
The inputs to the slow trigger (Figure B34) are almost identical to those of the high-speed trigger. The only differences are that the capacitor for the binary input is 33 uuf instead of 15 uuf, and the extra diode of the DC inputs is not used unless the grid clamp diodes are used. The difference in outputs for the slow trigger is that the tapped plate resistance is 6.8K and 3.3K instead of being two 5.1K resistors.

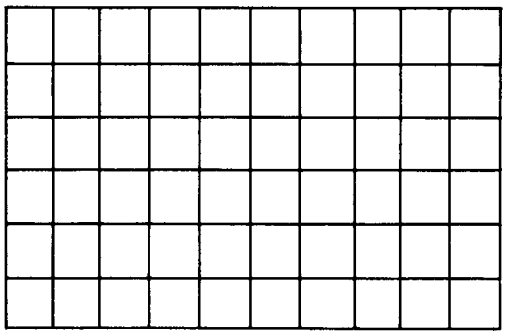
Voltage Levels and Input Requirements

The voltage levels are the same as for the high-speed trigger. The binary input requirement is the same as for the trigger, except that the maximum input frequency should be below 100 kilocycles. With larger input pulses, the slow trigger can operate up to one megacycle. The negative shift input requires a 20v step with a minimum slope of 40 volts/microsecond for frequencies below 100 kilocycles.









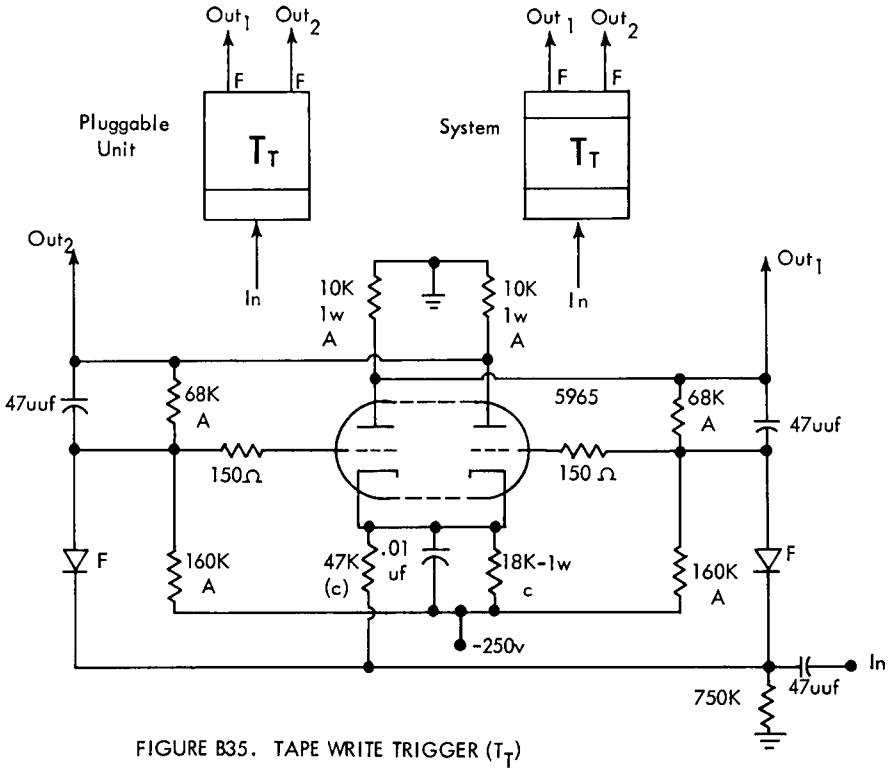


FIGURE B35. TAPE WRITE TRIGGER (T_T)

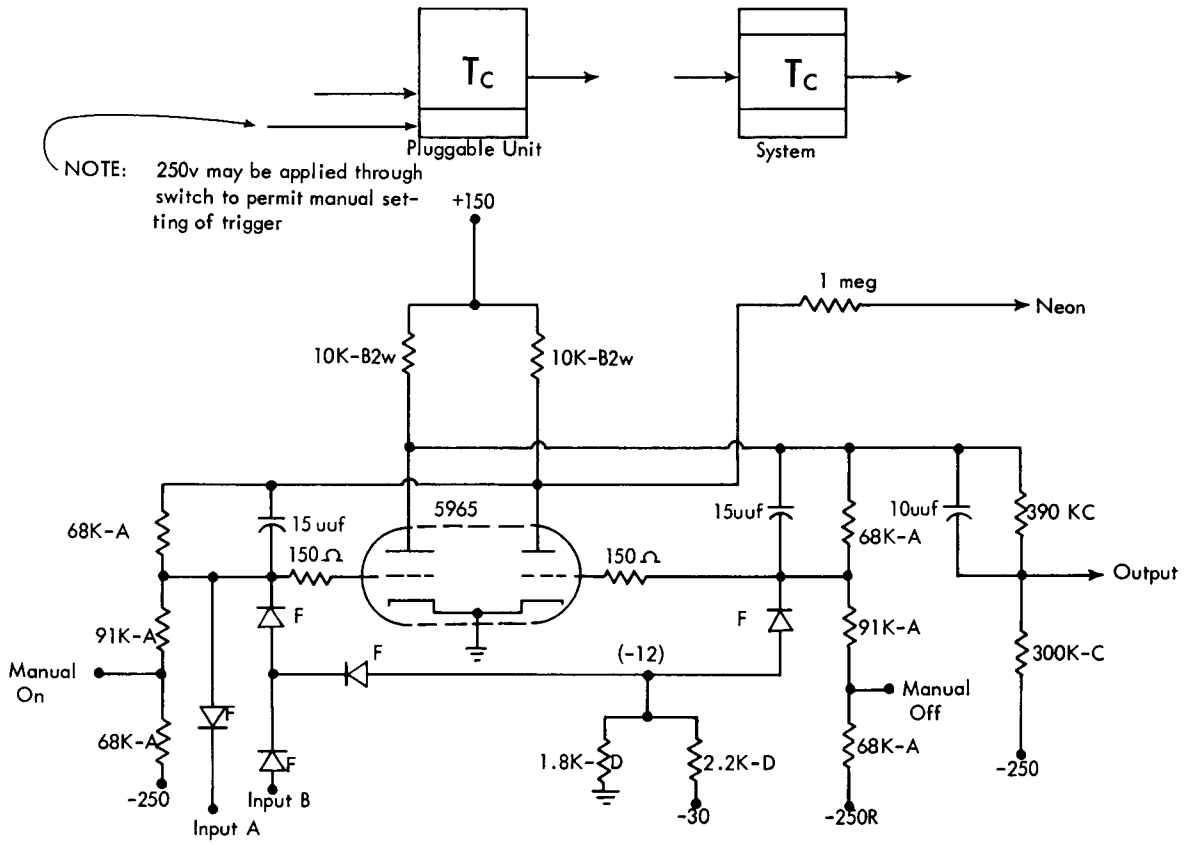


FIGURE B36. TRIGGER (T_C)

2.02.07 Tape Write Trigger (T_T)

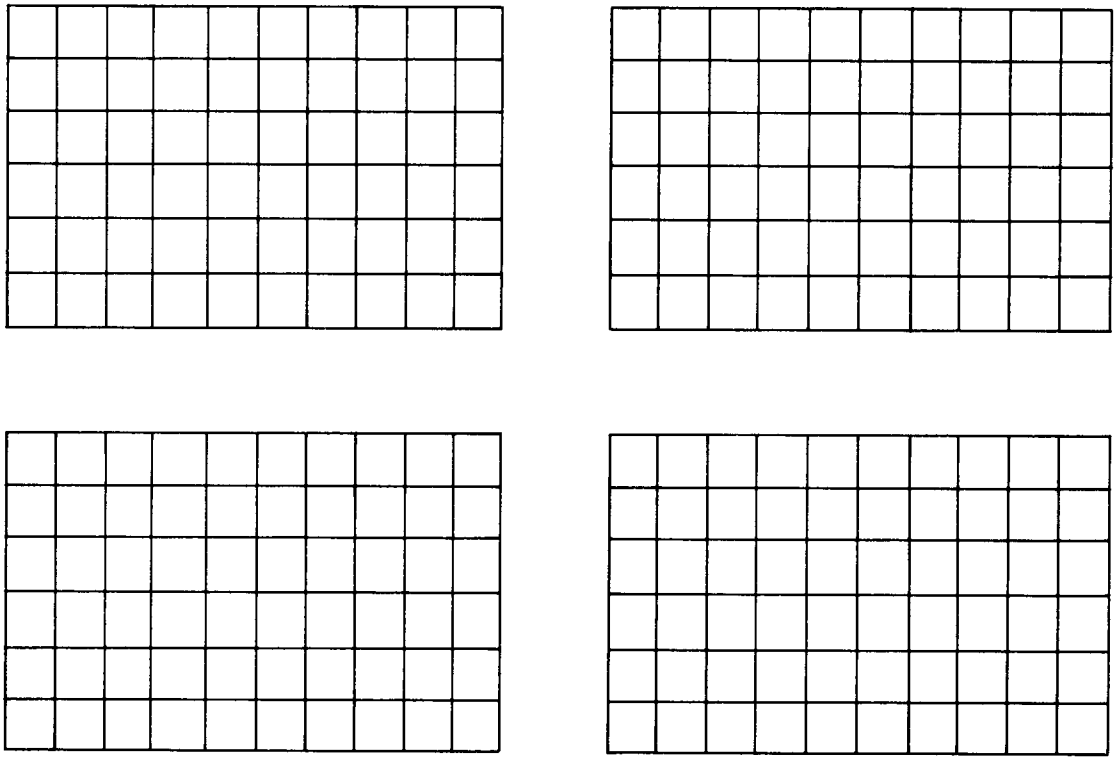
T_T is a binary trigger used to provide a push-pull input to the tape write tube, WT. It is popularly called the tape write trigger (Figure B35). Its input is a standard 10-microsecond, positive pulse, arriving when a binary one is to be written. The fall of this pulse flips the T_T; in so doing, it reverses the inputs to the WT. Overall considerations of the circuits that this trigger must feed dictate that the plate supply should be grounded. The 47K resistor is the differentiating resistor for the binary input, and the one-megohm resistor is added to desensitize the circuit. In other respects, the trigger resembles the high-speed trigger, although no clamping is used on the grids. The approximate DC levels of the plate are -68 volts and -15 volts, while the grids are approximately -100 volts and -120 volts. The cathode, of course, is near -100 volts.

2.02.08 Trigger (T_H)

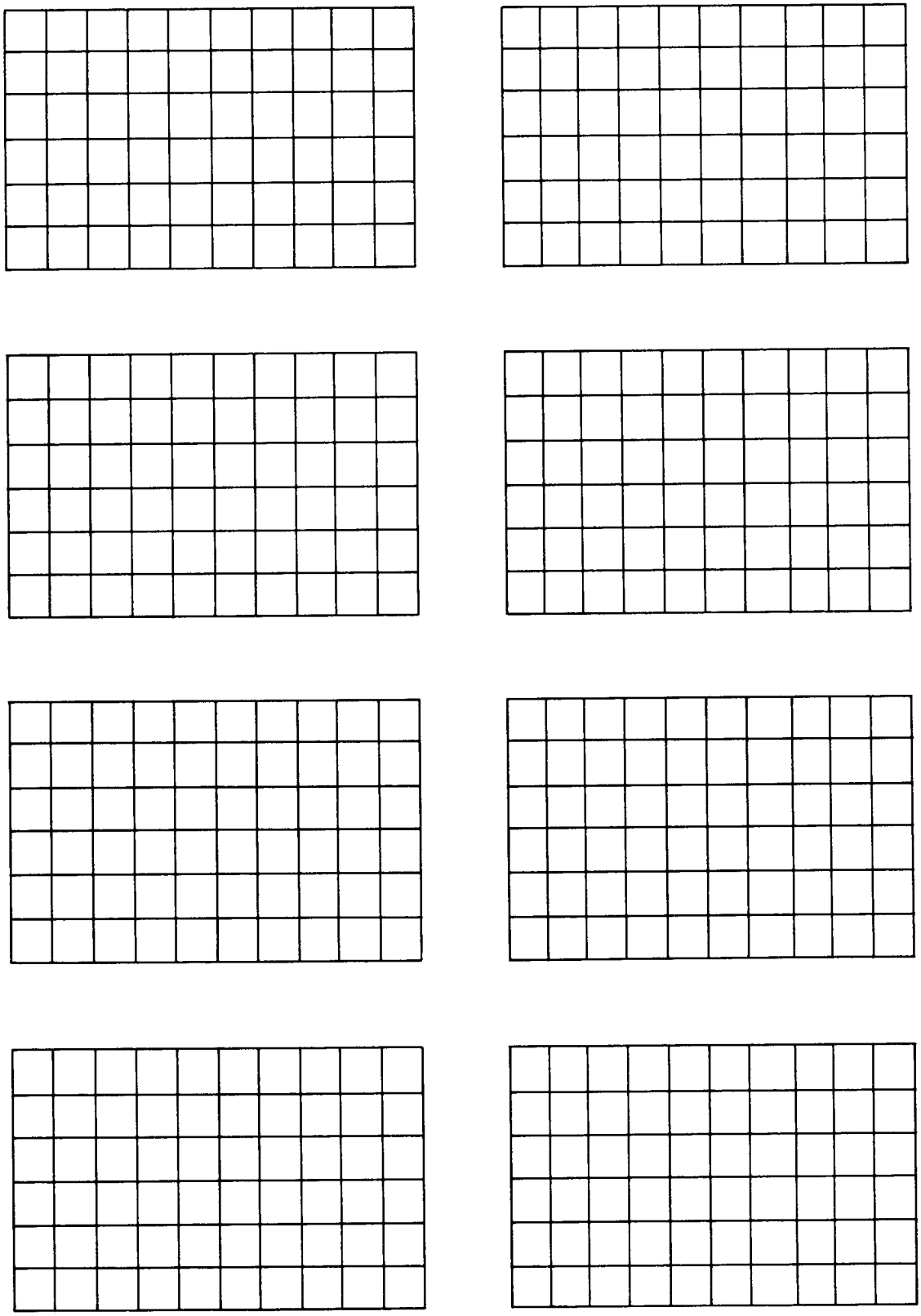
This component was assigned to the 701 field tester only (section 2.01,11, Book B).

2.02.09 Trigger (T_C)

The T_C (Figure B36) is similar to the T_S except that it delivers an output at a lower potential (about -60/-100) to the deflection circuits in the CRT output recorder. It drives a CF_C and indicator neons.



NOTES



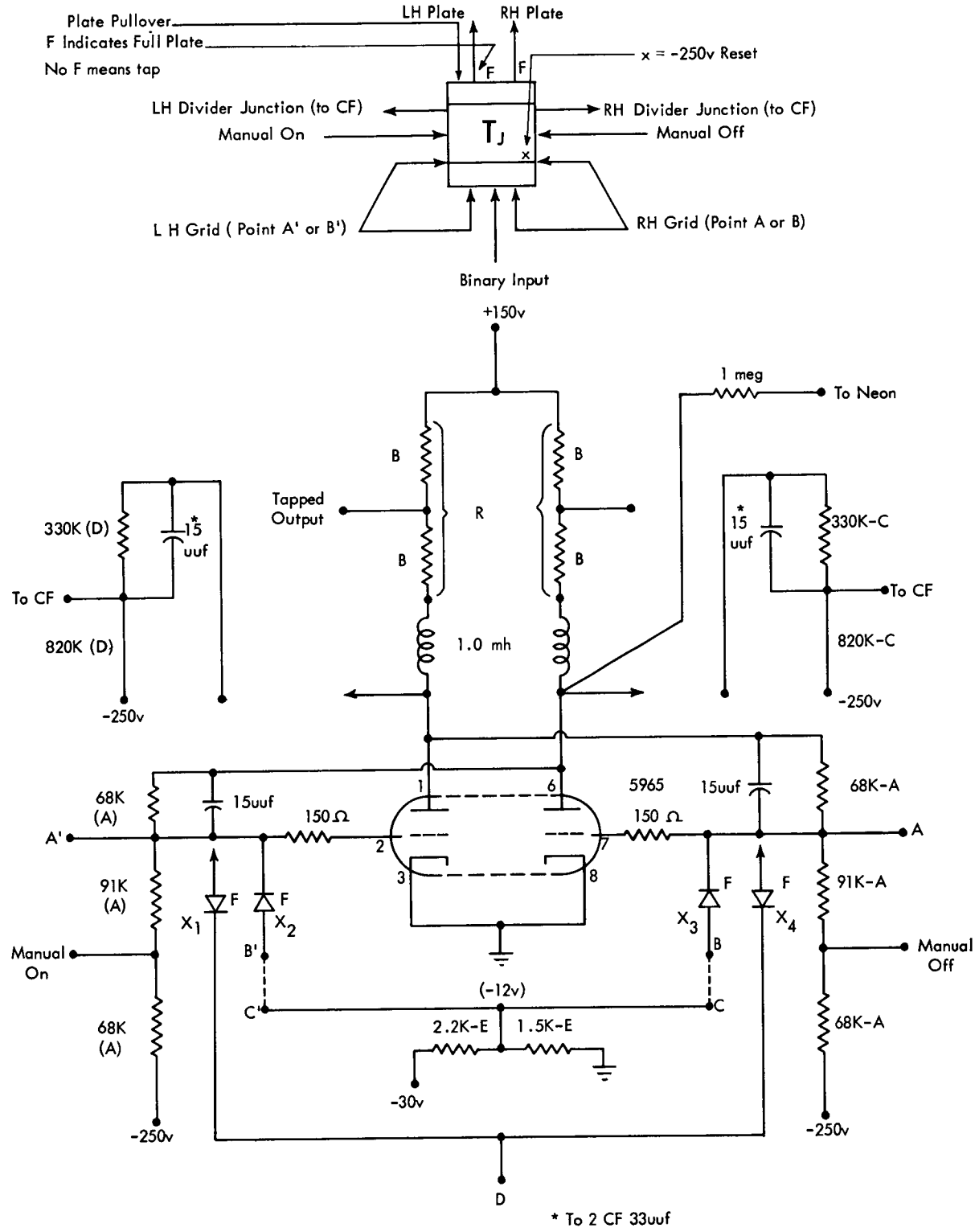


FIGURE B37. TRIGGER (T_J)

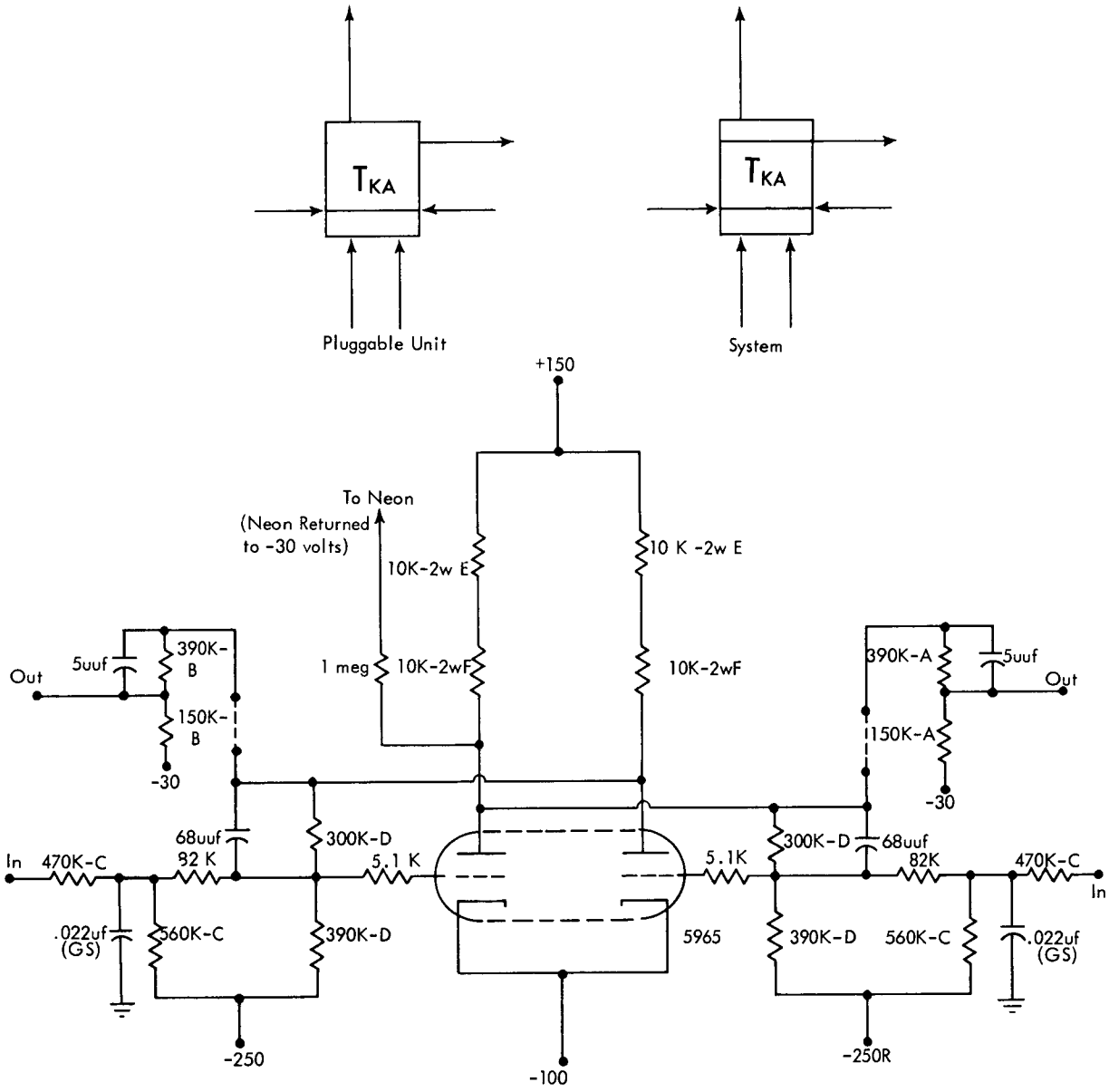


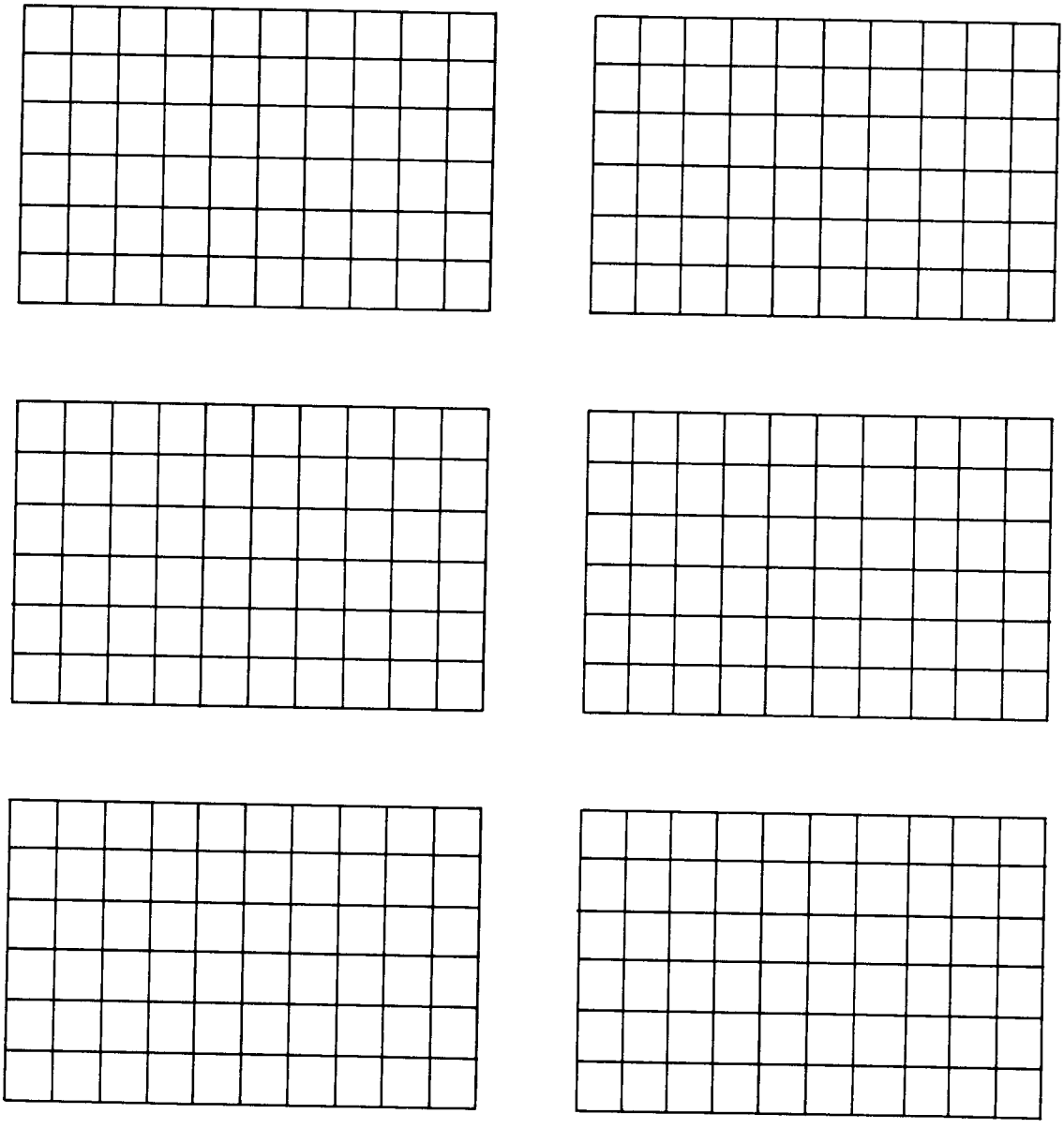
FIGURE B38. KEY TRIGGER

2.02.10 Trigger (T_J)

The operation of this trigger is identical to that of the standard trigger. The divider output provides a higher up level for a CRT output recorder application (Figure B37).

2.02.11 Key Trigger (T_{KA})

The function of the T_{KA} (Figure B38) is identical to that of the T_K key trigger. The 5844 is not easily adaptable to open filament detection so the 12v filament 5965 is used. The increased negative voltage and corresponding change in component values were necessary to obtain a fast output fall time. Plate voltages are about +125 volts and -50 volts; divider output voltages are +13 and -35. The output rises in about five usec and falls in about 0.5 usec.



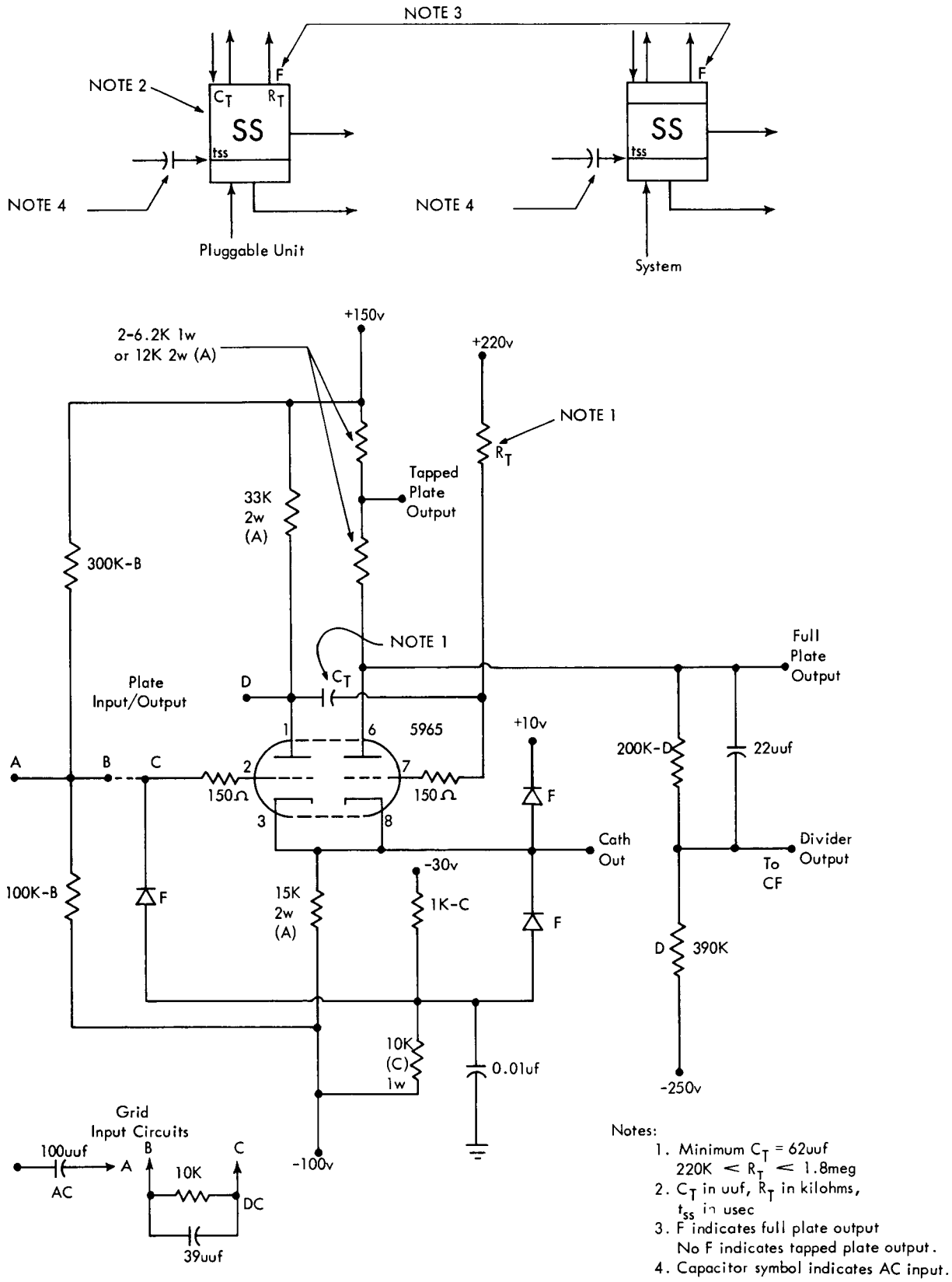


FIGURE B39. SINGLE SHOT (SS)

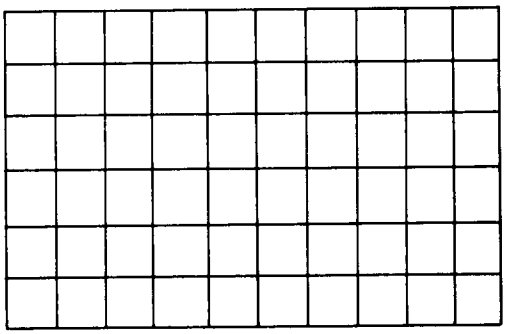
2.03.00 SINGLE-SHOT MULTIVIBRATORS

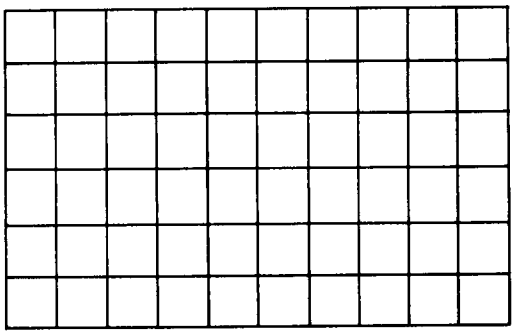
For further information on single-shot multivibrators, refer to section 2.11.00, Book A.

2.03.01 Single Shot (SS)

Circuit Description

The single-shot used in the 701-704 is a cathode-coupled circuit as shown in Figure B39. See Figure B40 for illustrations of single-shot wave forms. In the stable state, the left tube is cut off; the right tube is conducting heavily. In this state, the cathode and right grid voltages are about +10, the left plate voltage is +150, and the right plate voltage is about +60 volts as shown at point 1 in Figure B40. The most common method of firing a single shot is by plate pull-over. When using plate pull-over, the left plate of the single shot is connected to the plate of the pull-over inverter and the load resistor for the left plate also acts as the load resistor for the pull-over inverter. When a positive input arrives on the grid of the pull-over inverter, conduction through the common plate resistor drops the voltage of the left plate of the single shot. This negative shift is coupled through the capacitor to the right grid, Figure B40c, cutting off the right tube. The cathode voltage starts to fall because of the reduction in current through the cathode resistor, Figure B40d. The left grid is held to about -38 volts by a voltage divider, and as the cathode voltage falls, the left tube comes into conduction, pulling its plate voltage down. Current flowing through the cathode resistor from the left tube stops the fall and holds the cathode voltage at -36 volts. A clamp diode in the cathode circuit prevents component variations from causing the voltage on the cathode to fall below -36 volts. The clamp diode on the left grid prevents the Miller capacitance effect from dropping the left grid voltage below -36 volts. The left tube at this time is conducting; it is operating near zero bias. The input pulse may be removed any time after the left tube begins to conduct; the circuit will remain in the quasi-stable state, for the left plate voltage will be held down by the conduction of the left tube. Point 2 in Figure B40 shows the voltages at the end of the initial transition (nominally requiring about 0.5 microsecond to be completed). When the input pulse from the pull-over inverter is removed, the loss in pull-over inverter current flowing through the left plate load resistor may appear as a slight positive shift in the left-plate and right-grid wave forms, as shown in point 3 of Figure B40





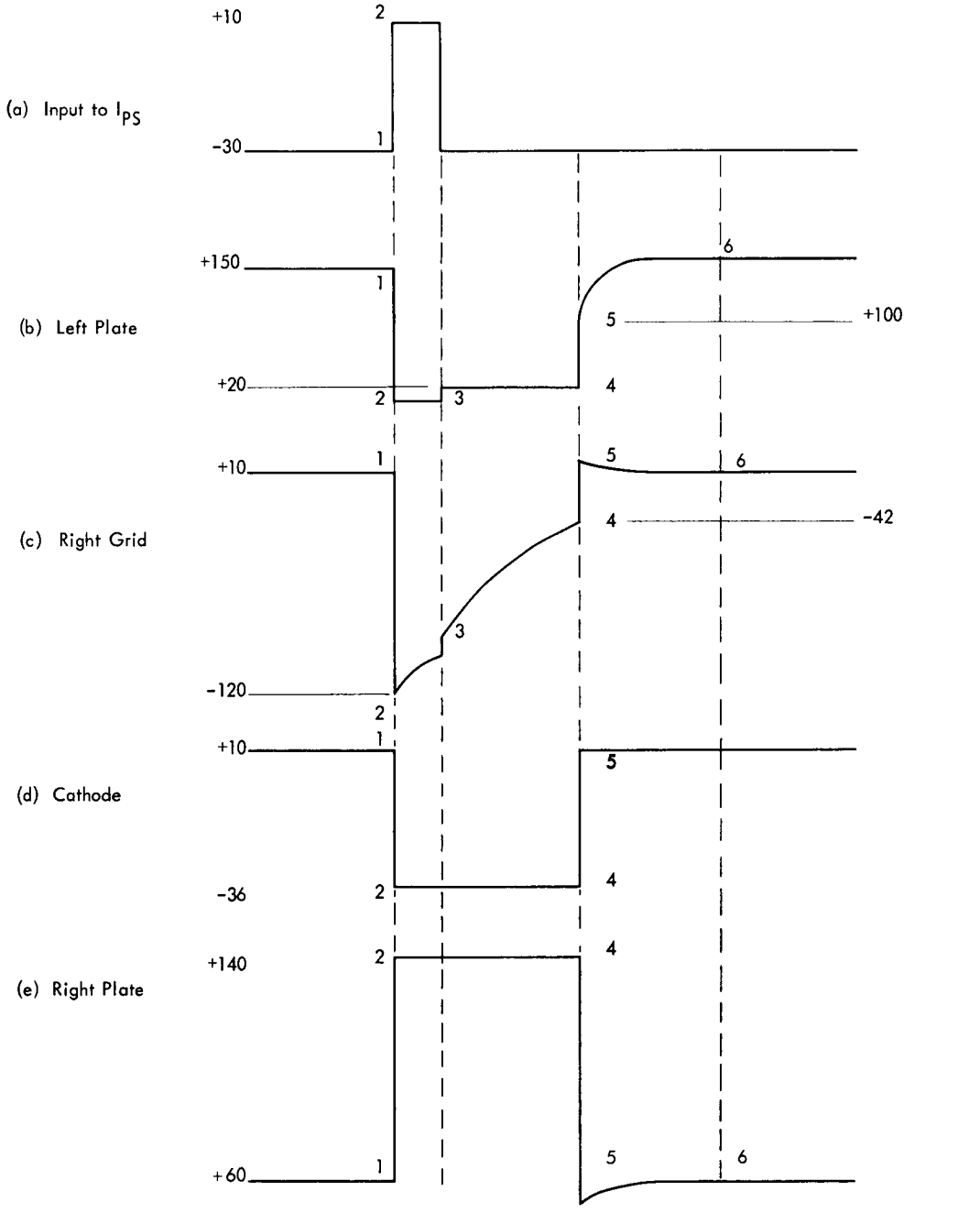


FIGURE B40. SINGLE-SHOT WAVE FORMS

Single Shot Timing

The duration of the single-shot output pulse, t_{SS}, is largely dependent upon the discharging of the capacitor, C_T, connected between the left plate and the right grid. At point 1, the capacitor has an initial charge of 140 volts. At point 2, the capacitor still has the 140v charge, but current flow begins to discharge it. The path for this current is from +220 volts through the resistor R_T connected to the right grid, through the capacitor, through the left tube, and through the cathode resistor to -100 volts. Discharging the capacitor causes the voltage at the grid end to rise. When the voltage at the right grid has risen to -42, the right tube again begins to conduct. The cathode voltage rises again to its original value, cutting off the left tube as it does so. The left plate voltage, therefore, rises toward its original +150v level. The time, t_{SS}, depends upon a large number of factors (Figure B40c).

The first factor that affects timing is the level to which the left plate voltage falls. The lower this voltage goes, the lower the right grid voltage falls, and the more time required to bring this grid voltage back up to -42 volts.

Another factor is the time constant of the circuit through which the discharging current flows, that is, the circuit path mentioned previously. All components in this circuit except the C_T and R_T are fairly constant. R_T and C_T may be varied to determine the duration of the pulse; therefore, they are called the timing resistor and the timing capacitor. The larger R_T or C_T are, the more time required for the right grid voltage to rise to -42 volts. The duration of the single-shot pulse in microseconds is about $0.25\ R_T\ C_T$, where R_T and C_T are in megohms and uuf. The value of cut-off for the right tube in this circuit also affects the timing. All these factors except R_T and C_T are fairly constant and enter into the 0.25 coefficient for the timing equation. Variance in components and voltages, though, can cause the actual value of pulse width to deviate from the calculated value by as much as ±20 percent.

Recovery Time of the Single Shot

Although it was mentioned before that the voltage values at various points in the circuit return to their stable values when the single-shot timing has ended, this generalization is not strictly true. The left plate voltage rises to a new value upon the second transition, in about a half microsecond, but this value is lower than +150 volts (point 5 in Figure B40b). This voltage is determined by the balance of voltages in the circuit connected to this plate. The positive shift at the left plate is coupled to the right grid, which comes positive enough to draw heavy grid current in the right tube. The upper level of the right grid voltage is clamped through the right tube and the +10v clamp diode on the cathode; this clamping action prevents the voltage on the left plate from rising to +150 volts until the coupling capacitor again becomes charged to its original 140v charge. The path for charging current is now from +150 volts, through the left-plate load resistor, through the capacitor, through the grid-to-cathode resistance of the right tube, and finally through the cathode resistor to -100 volts. The charging of the capacitor shows its effect upon the left plate voltage from point 5 to point 6 in Figure B40b. The right-grid wave form shows the clamped overshoot on the grid, and Figure B40e shows the resultant overshoot in the plate voltage of the right tube because of the heavy conduction. The time of recovery, that is, the time required for the left plate voltage to return to +150 volts, can be estimated in microseconds as $0.24\ C_T$, where C_T is in uuf. Note that the timing resistor has no effect

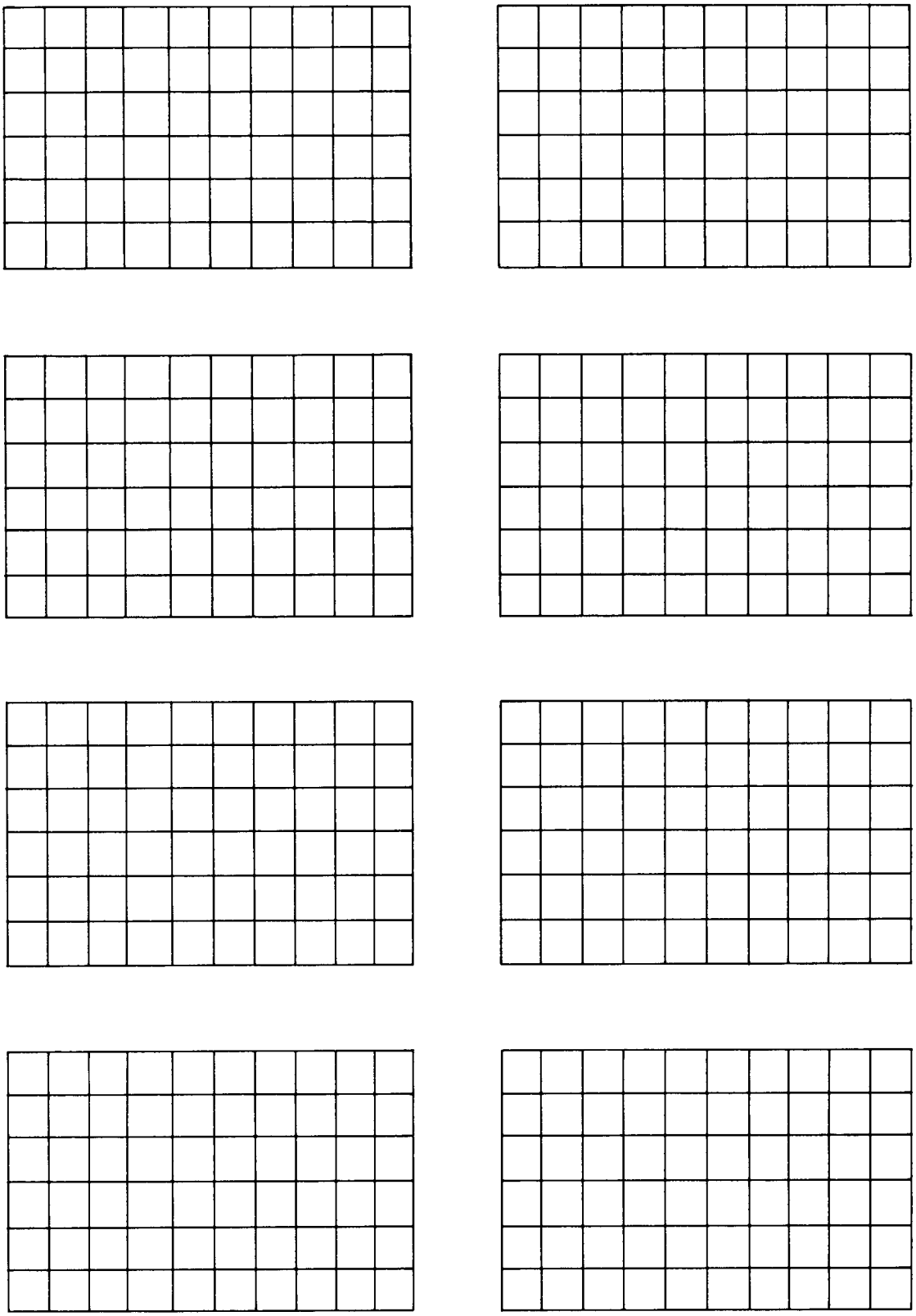
on this time. Recovery time is an important consideration in single-shot operation. If the circuit has not recovered from an operation when a second input pulse arrives, the negative shift on the left plate is smaller, and thus the time of the single shot pulse is shorter. Therefore, for stable operation, the period of the input pulses must be greater than the combined t_{SS} and recovery time.

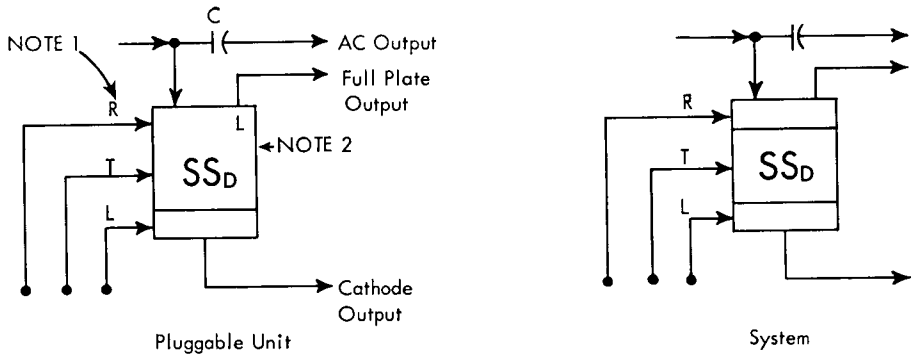
Inputs and Outputs, Block Diagrams

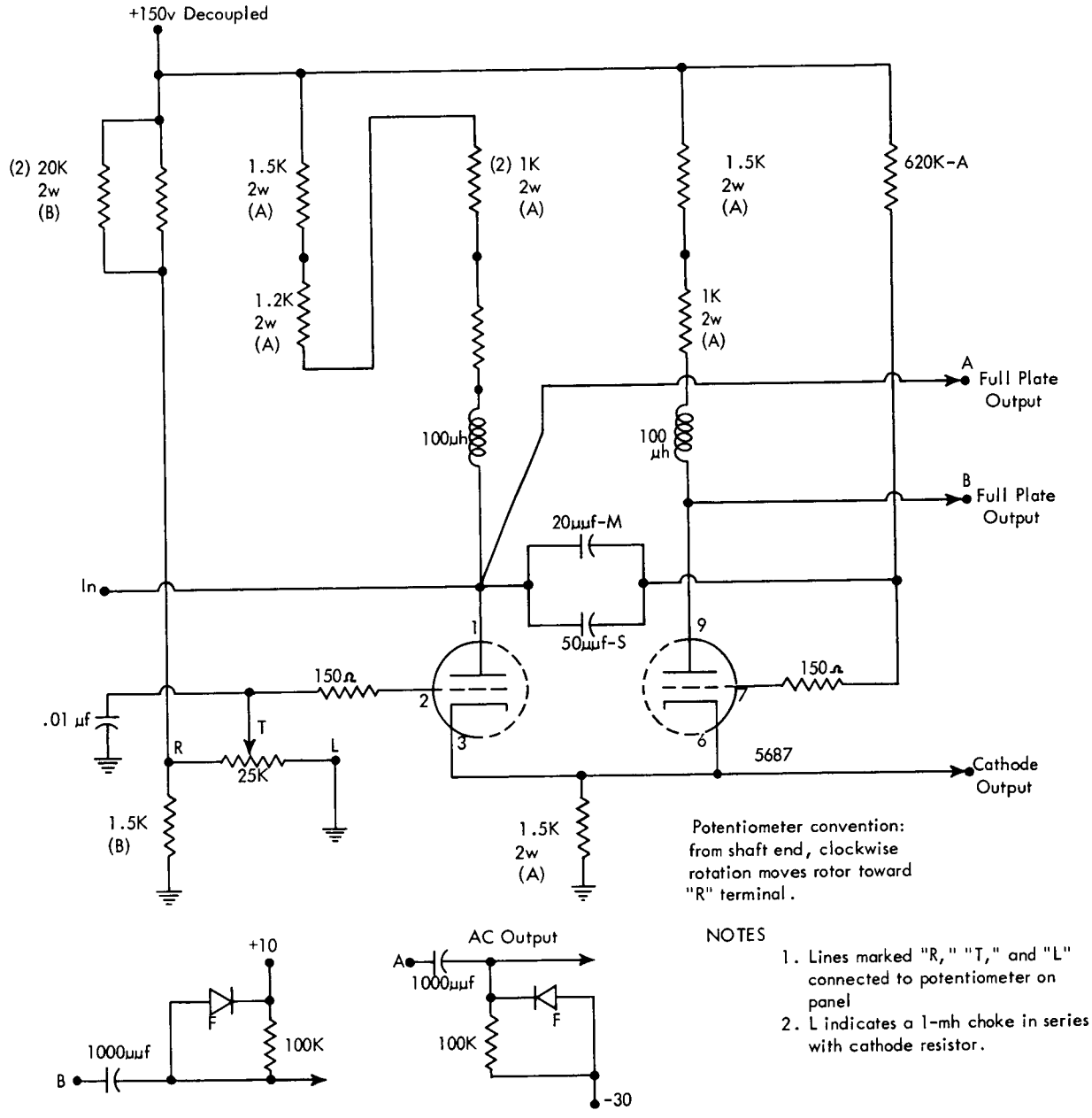
Requirements for a plate pull-over input are that the positive pulse applied to the pull-over inverter must rise above +5 volts and fall below -15 volts for reliable operation. If the pulse width of the input to the inverter is greater than 75 percent of the pulse width of the single shot, then the input to the inverter must be RC-coupled; otherwise, it may be direct-coupled. The plate pull-over input to the single shot is indicated by an arrow into the top of the block at the left. Another input is the grid input shown as an arrow into the left side of the block in the middle or into the bottom of the block at the left. The grid input brings the left tube into conduction, pulling down its plate voltage. From this point, the regenerative action is the same as for a plate pull-over input. The grid input requires at least a 50v, positive pulse for reliable operation; this voltage swing is usually obtained from the full plate output of a key trigger or another single shot. A large positive output pulse may be obtained from the full right plate output, shown by an arrow out of the top of the block at the right. An F is placed next to the output to indicate that it is a full plate output. A 40v, positive pulse for feeding triggers may be obtained from the tapped-plate load-resistor output, indicated by the same output line as the full plate output. A positive grid-level pulse may be obtained from a divider attached to the right plate. This is a nominal +10 to -45v pulse, but it feeds a cathode follower which sets the lower level to -30 volts. The divider output is indicated by an arrow out of the right side of the block in the middle. A standard negative pulse may be obtained by feeding the cathode voltage into a cathode follower. The cathode output is indicated by an arrow out of the bottom of the block in the middle. A large negative pulse may be taken from the full left plate; it is indicated by an arrow out of the top of the block at the left.

A special input may be used to suppress or cancel single-shot action. This input is from a cathode follower and is connected to the cathode of the single shot. If the input to the cathode follower is about +10 volts, its output holds up the cathode of the single shot, even though the single shot is pulsed at the grid or by plate pull-over. With the cathode held up by the cathode follower no regenerative action can occur in the single shot; no output pulse is produced. The left plate voltage of the single shot is pulled down by the pull-over inverter (if plate pull-over is used) but the plate voltage rises again after the input pulse is removed. If the single shot is in its quasi-stable state when the positive gate is applied to the cathode, the single shot is immediately triggered back to its stable state. Thus the +10 volts applied to the cathode can either suppress or cancel the single-shot action.

NOTES







NOTES

1. Lines marked "R," "T," and "L" connected to potentiometer on panel
2. L indicates a 1-mh choke in series with cathode resistor.

FIGURE B41. DRUM SINGLE SHOT (SS_D)

2.03.02 Dot Pulse Single Shot (SS_B)

This component was assigned to 701 electrostatic memory and is not used now.

2.03.03 Drum Single Shot (SS_D)

SS_D is a special single-shot multivibrator (Figure B41) producing an extremely short pulse of variable duration. It is used in the drum system for positioning the drum-read-sample pulse. An I_R serves as a pull-over inverter for the SS_D used to delay the read sample pulse. Its input is a single delayed timing pulse, gated with a 10-microsecond drum read gate. Its peak has been slightly clipped by the drum read gate. This circuit was designed: (1) to produce extremely short pulses of variable duration, and (2) to have a short recovery time (the recovery time not being important in this application).

The width of the output pulse is controlled by varying the bias on the left-hand grid; the more positive the applied voltage to this grid, the wider the pulse. Because the grid voltage may vary, no clamping diode can be used as in the SS circuit. To keep the Miller capacitance effect in the left tube from pulling the left grid down during the initial shift of the circuit, a coupling capacitor is used between the right-hand plate and left-hand grid. This capacitance is larger than is needed to suppress the Miller effect; therefore, it actually pulls the left-hand grid up and thus speeds the response of the circuit. The addition of this capacitor tends to slow the response of the right-hand plate, so the coil is used in that plate circuit to compensate for the capacitance. The coil in the opposite plate circuit compensates for the other coupling capacitor to decrease recovery time. The width of the pulse may be varied from at least two to five microseconds; within this range, the width is quite stable despite variations in plate supply voltage.

2.03.04 Single Shot (SS_O)

The SS_O (Figure B42) is used to give a standard output from amplifiers. This circuit is a cathode-coupled single-shot multivibrator, but its operation is considerably different from that of the standard SS. The basic difference is that the timing is controlled at the left cathode. In this circuit, the left side is that wired to pins 6, 7, and 9; the right side is wired to pins 1, 2, and 3. The operation of the circuit is as follows. A negative pulse is coupled through the input capacitor and is differentiated by the input circuit. The left tube is initially conducting and is cut off by the negative pulse. Its plate rises and pulls up the grid of the right tube (normally cut off). This action causes the right tube to conduct, and in doing so, its cathode rises. This cathode rise is coupled back to the left cathode; this rise further cuts off the left tube. Such regenerative action continues until the left tube is completely cut off and the right is conducting. After this quasi-stable condition is reached, the voltage on the grid of the left tube begins to rise exponentially toward ground potential. At the same time, the voltage on the left cathode falls exponentially toward -100 volts. This action is caused by the charging of the cathode-coupling capacitor through the right tube, and the left cathode resistor. Because the left cathode is falling and the left grid is rising, some point will be reached when the left tube will begin conducting again. This conduction causes the left plate to fall, the right grid to fall, the right cathode to fall, and the left cathode to fall. This regenerative action returns the circuit to its stable state.

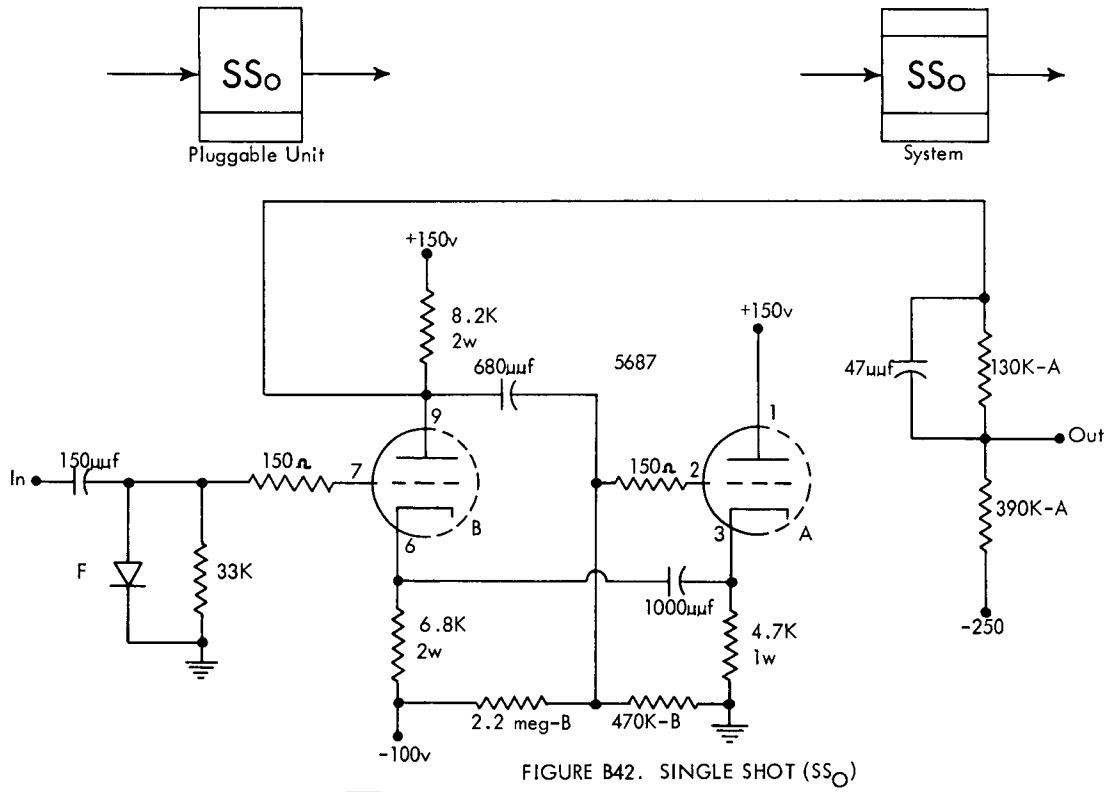
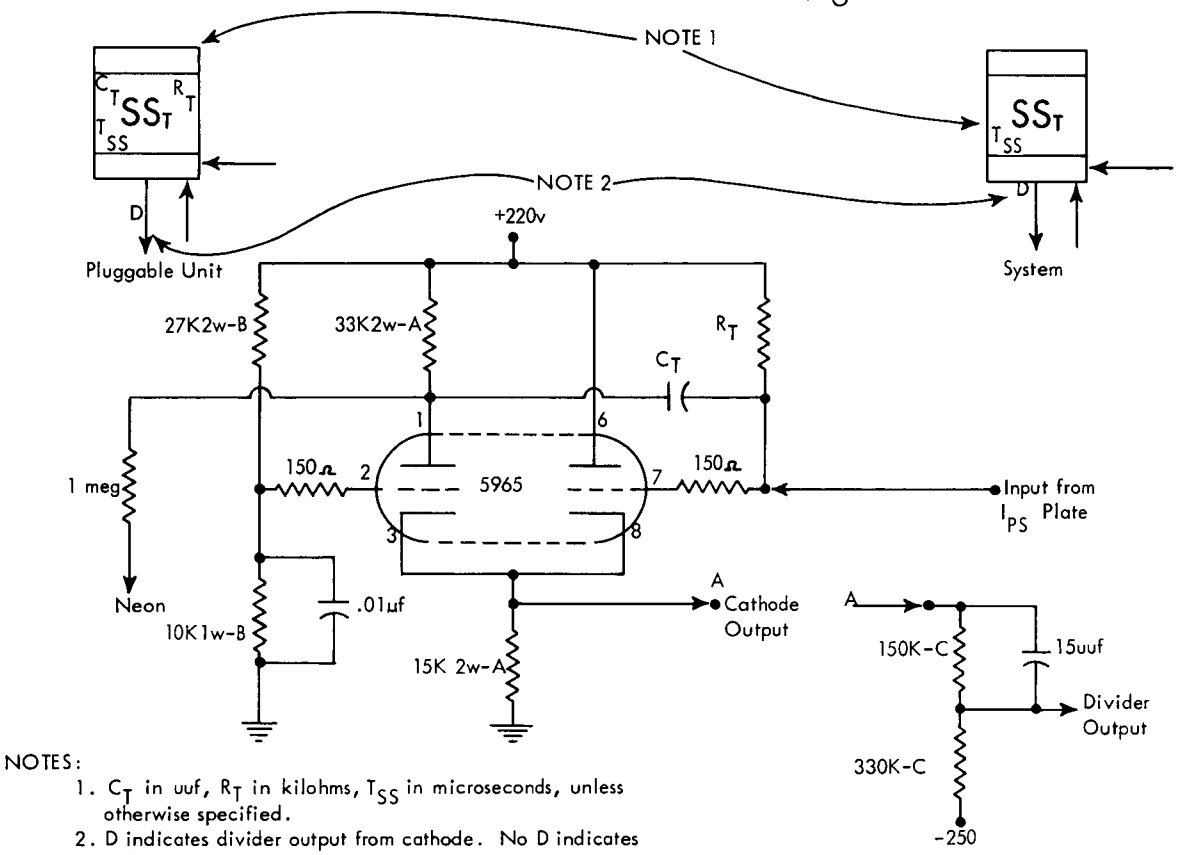


FIGURE B42. SINGLE SHOT (SS_O)



NOTES:

1. C_T in uuf, R_T in kilohms, T_{SS} in microseconds, unless otherwise specified.
2. D indicates divider output from cathode. No D indicates cathode output.

FIGURE B43. SINGLE SHOT (SS_T)

2.03.05 Single Shot (SS_T)

The SS_T is a special single-shot multivibrator (Figure B43) used in the tape circuits for adding time. This single shot resembles the standard single shot, except for a few modifications. The basic difference in this circuit and the SS is that the SS_T is fired by a direct-coupled pull-over inverter connected directly to the timing grid.

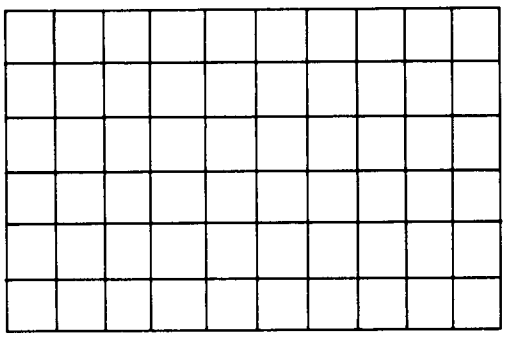
If a positive input is applied to the grid of the inverter, the SS_T flips into its quasi-stable state. As long as this input is retained, the SS_T remains in the quasi-stable state and does not begin its timing period, because the plate of the inverter holds the timing grid at a constant voltage. Not until the input to the inverter is removed does the SS_T begin its normal timing period. Whenever the input to the inverter goes positive, the SS_T flips to its quasi-stable state, regardless of whether it was in the timing cycle or was in its stable state when the positive input arrived.

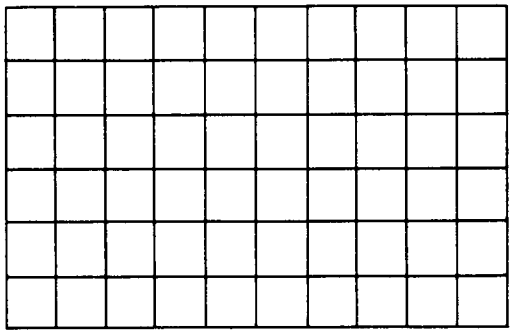
Circuit Description

To make the circuit operation stable, all positive voltage returns are to +220 volts and the cathode voltage return is grounded. The cathode output provides a negative signal. If the circuit is to produce a standard-level signal, a voltage divider (indicated by a D) is used. No resistor is used in the right plate circuit, because no positive output pulse is needed and stability is improved. The left tube conducts quite heavily; therefore, the bypassed low-impedance biasing divider is used at the grid of that tube. A neon bulb returned to +150 volts on the panel is lit when the SS_T is in its quasi-stable state. The timing equation for the SS_T is $t_{SS} = 0.25\ R_T\ C_T$ $\pm$20 percent.

The SS_T is useful for the sensing of EOR or EOF in the tape circuits. For example, in the EOR circuit, a stretched group pulse of 32 microseconds width causes the SS_T to flip. As long as a stretched group pulse arrives within 400 microseconds after the fall of the preceding one, the SS_T is flipped back to its quasi-stable state without ever completing its timing period and returning to its stable stabe. But if this 400-microsecond time is exceeded, the SS_T returns to normal and thus signals an EOR condition. A 30 millisecond SS_T is used in the EOF sensing circuit.

Because the output of a SS_T is abnormal for a period equal to the time of an input pulse plus the time of the circuit itself, it can be used conveniently to add time when the total is too large a value for one standard SS circuit alone. This is done in the EOF delay circuits.





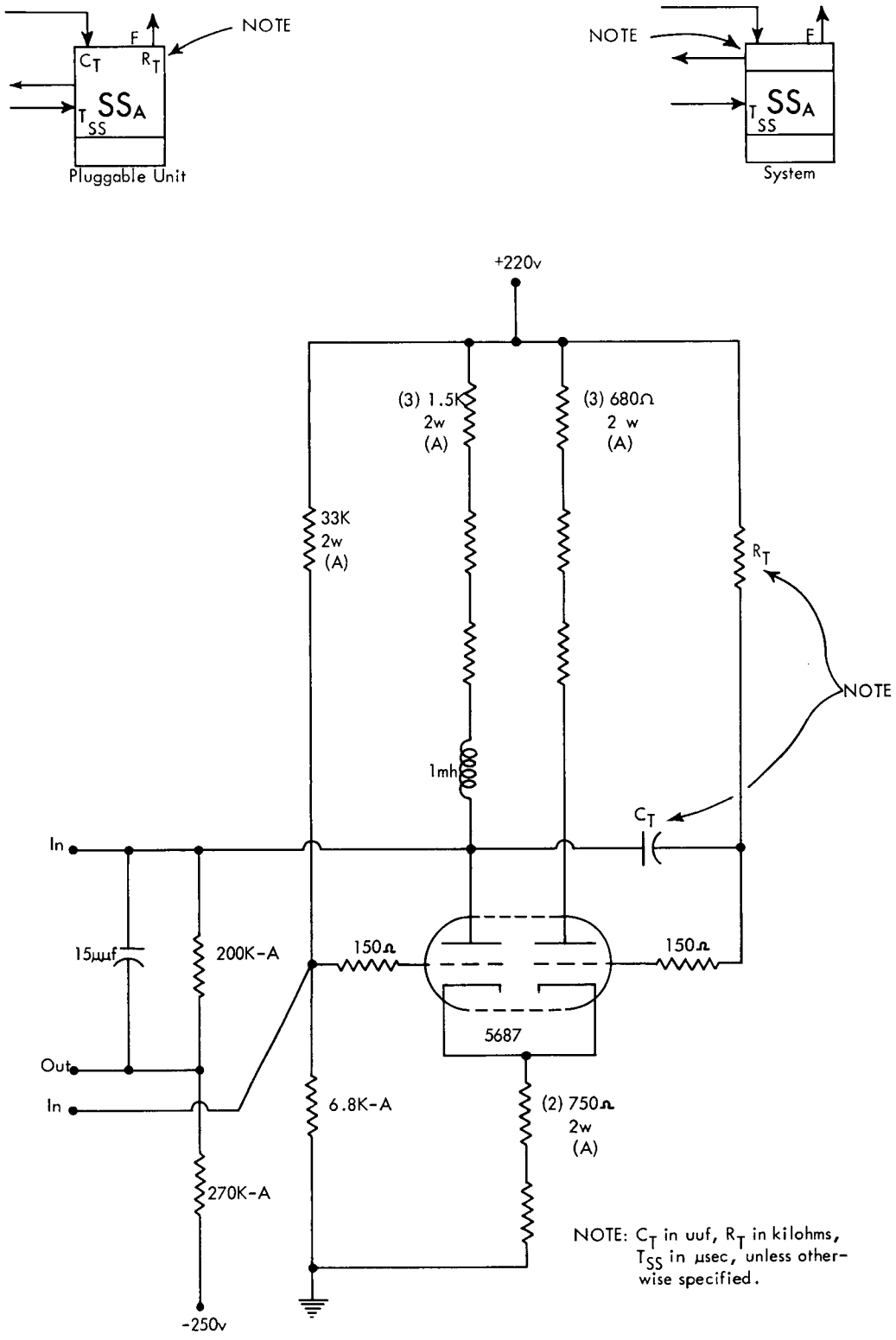


FIGURE B44. SINGLE SHOT (DRUM) (SS_A)

2.03.06 Single Shot (Drum) (SS_A)

SS_A is the symbol for a special single-shot multivibrator circuit (Figure B44) used to delay the picking of drum relays. It evolved from the SS_D, and still retains many of the properties of the SS_D. Some of these are a short recovery time, fast transitions, and high stability. The coil in the left plate circuit and the +220v plate return help decrease recovery time. This circuit is fired by a pull-over inverter at the left plate. The output is also taken off the left plate through a voltage divider. The divider connected to the left plate should give a +20 volt to -49 volt output with the plate swing as shown. As in other single-shot circuits, a considerable overshoot is present when the positive shift of the left plate voltage couples to the right grid and causes the right tube to conduct very heavily for a short period.

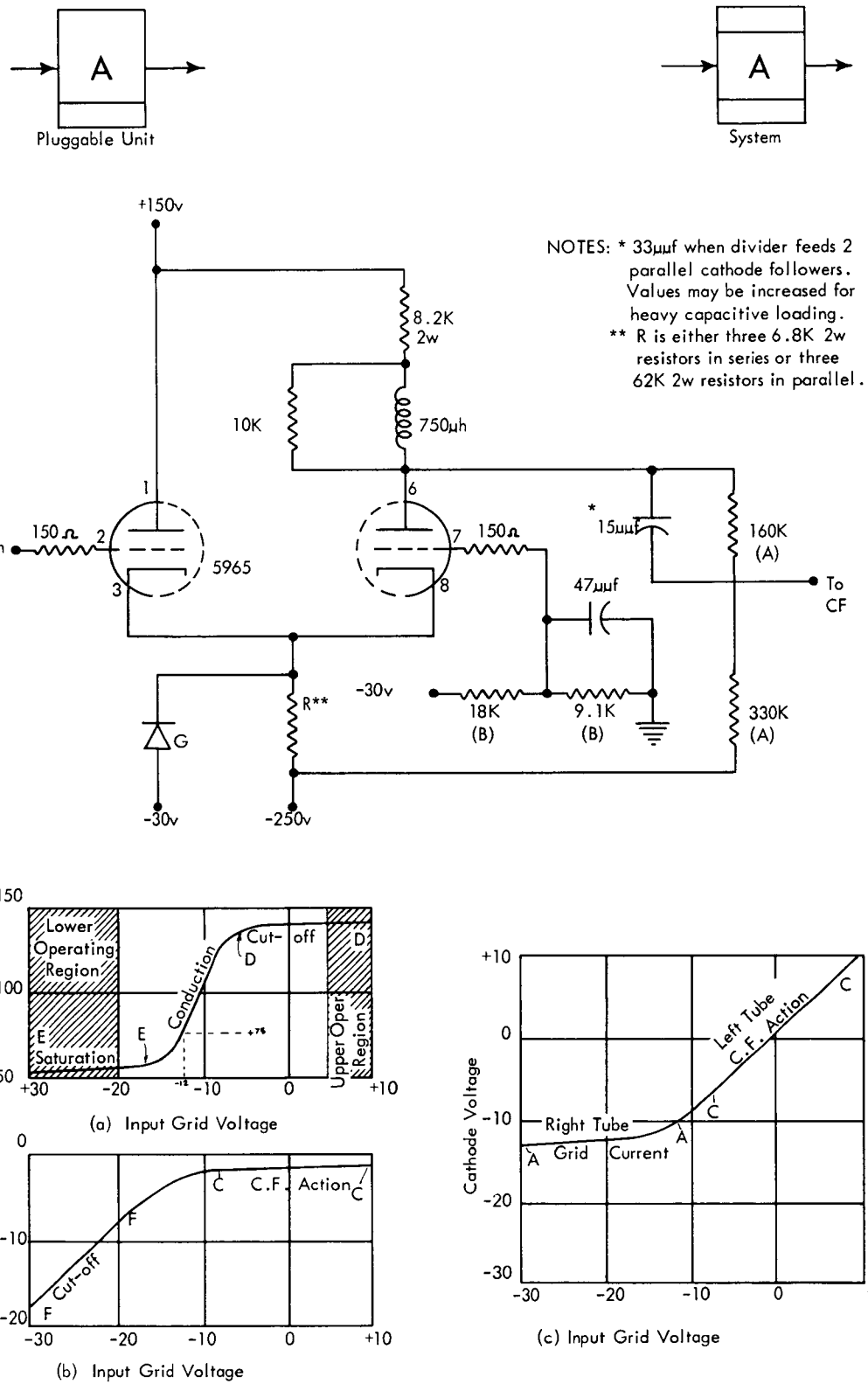


FIGURE B45. GROUNDED-GRID AMPLIFIER (A)

2.04.00 AMPLIFIERS

2.04.01 Grounded-Grid Amplifier (A)

The grounded-grid amplifier, A, (Figure B45) is used as a level setter; that is, when the upper or lower voltage levels of the signals fall or rise beyond certain prescribed values, the amplifier is used to restore the signal levels. An important feature of the amplifier is that it does not invert the signals; positive signals are amplified as positive signals and vice versa. Level setting without inversion is sometimes accomplished with two inverters (I or I_S). Two inverters use fewer components and give sharper rise and fall characteristics to the pulses, but delay is increased. Therefore, two inverters may be used only where delay is not important. On the other hand, the amplifier produces less delay and has about six uuf of input capacitance compared to about 35 uuf for the inverter.

Circuit Description

The input tube (left tube) of an amplifier acts as a cathode follower circuit; the output tube (right tube) acts as an inverter, receiving an input pulse at its cathode instead of its grid. The fact that input signals do not arrive at the right grid accounts for the name, grounded-grid amplifier. The grid is not grounded in the sense that it is connected to zero volts, but is connected through an equivalent six-kilo-ohm resistance to -10 volts. Figure B45 is used in the explanation of this circuit. The curves shown are the result of measurements taken on only one amplifier. They are all plotted as a function of input voltage.

When the input voltage is +10 volts, the left tube acts as a cathode follower and pulls up the cathode voltage to slightly above ten volts. Since the grid of the right tube is connected to -10 volts, the right tube is cut off. Its plate voltage is pulled down to +140 volts because current flows through the output voltage divider. If the input voltage is reduced, the left tube still acts as a cathode follower in the region CC in Figures B45b and B45c; that is, the cathode follows the input voltage as in Figure B45c. As the input voltage is reduced to about -5 volts, the cathode falls far enough for some current to begin to flow in the right tube also. The region DD in Figure B45a shows that the right tube is cut off but, in the region from D to E, the right tube is conducting. When the right tube conducts, its current interferes with the cathode follower action of the left tube by holding the cathode voltage up, even though the grid input voltage may continue to fall. This occurs in the region FC of Figure B45b. When the input voltage drops to slightly below -10 volts, the cathode voltage drops to about -10 volts and the right tube begins to draw grid current. If the input voltage drops any farther, the cathode voltage drops only slightly because it is clamped by the grid circuit to -10 volts (Figure B45c, region AA). Impedance in this clamping circuit causes a voltage drop of two to three volts; therefore, the lowest point to which the cathode voltage may fall is about -13 volts. But if the input voltage continues to drop, the input tube becomes cut off as shown in the region FF in Figure B45b. In this region, the right tube is conducting heavily because it is operating under conditions of positive

grid-to-cathode bias. Its plate current curve in Figure B42a shows that saturation is reached in the region EE, and that the plate voltage falls no lower than about +60 volts. This plate voltage is fed to a divider, which should feed a cathode follower.

If an amplifier is to function as a -30v level setter, the lower level of the divider output voltage cannot be above -33 volts; therefore, the plate voltage cannot be above +75 volts. From Figure B42a note that the grid input cannot be above about -12 volts if the plate level is to remain below +75 volts. For reliability and safety factor, the lower level of the voltage input to the grounded-grid amplifier must not rise above -20 volts. Figure B42a shows that the input voltage could vary considerably around this value without the plate voltage's varying appreciably. The upper level of the input voltage should not fall below +5 volts, and Figure B42a shows that around this point also the input may vary considerably without the output's varying appreciably. The shaded regions in Figure B42a are the safe operation regions. Therefore, the nominal input voltages for proper operation of the amplifier are from +5 to +15 volts and from -20 to -30 volts. The nominal divider output voltages for these input voltages are +14 and -36 volts; the divider output voltages should not change appreciably if the input voltages are held within the limits just specified.

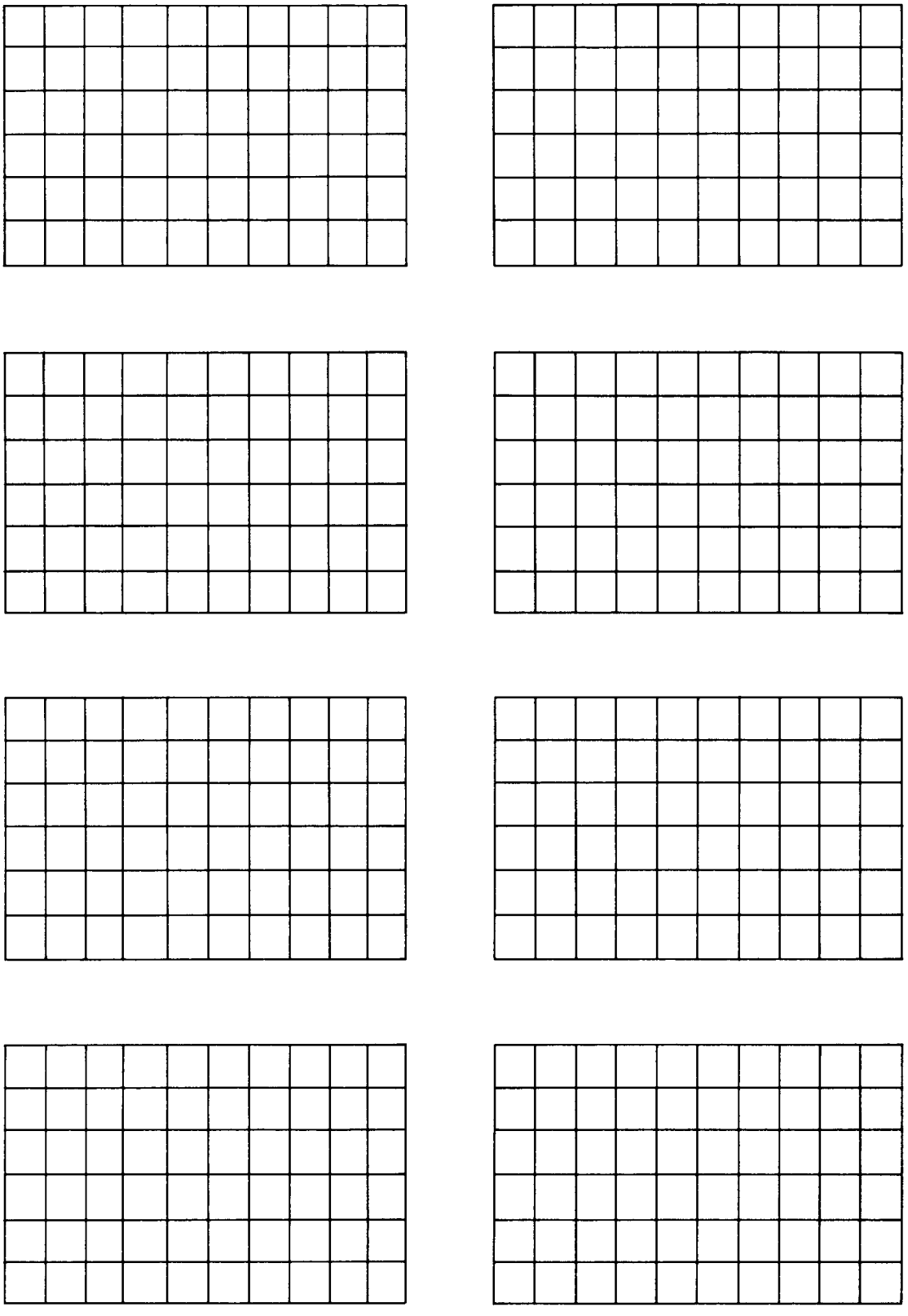
High-Speed Operation

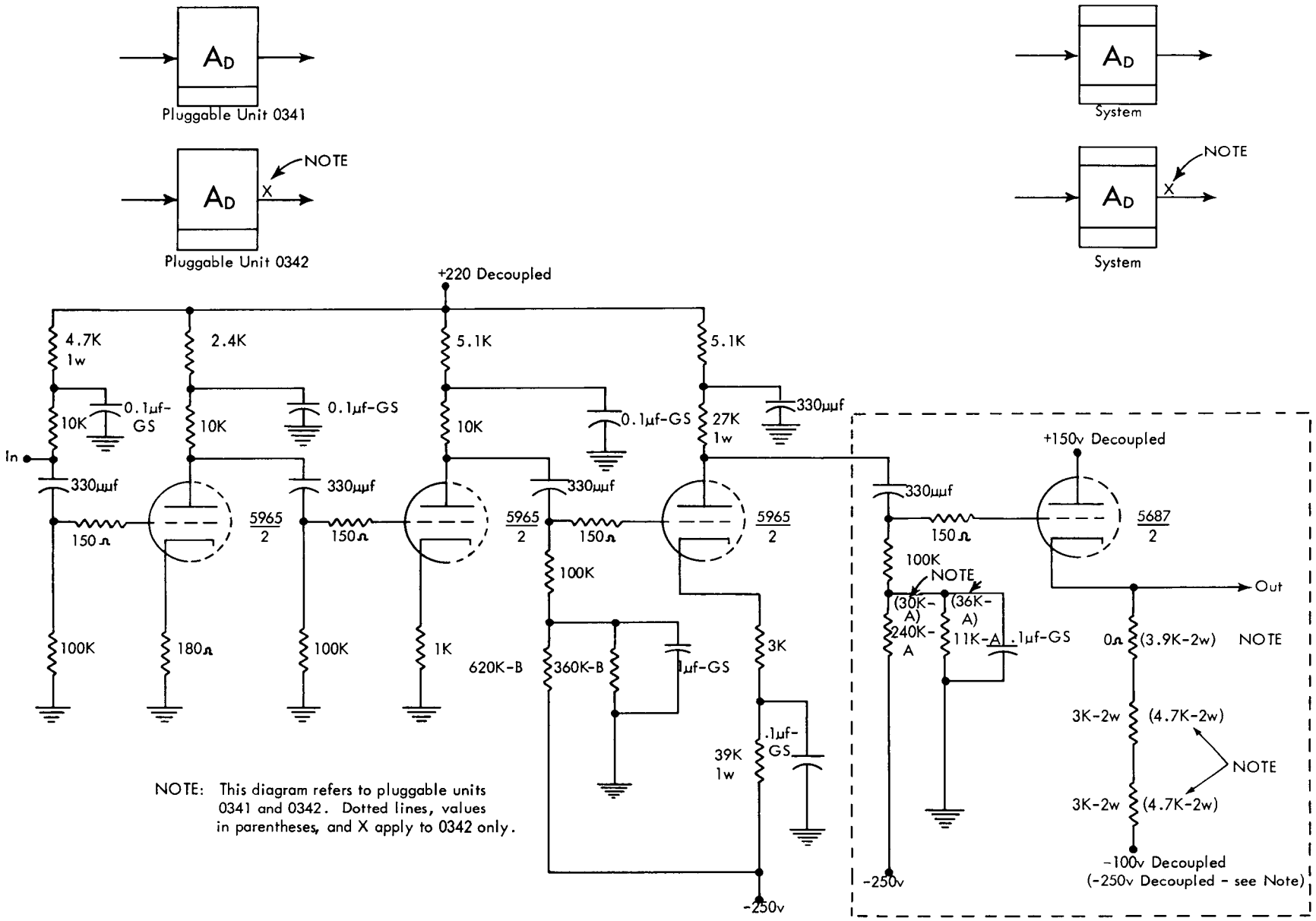
When a pulse is applied to the grid of the amplifier, the conditions described above change from the one extreme to the other. The rise time of the output pulse is reduced by peaking action of the coil in the plate circuit. Ringing of the output is prevented by the damping resistor shunting the coil. As in the inverter, the coil is wound on the resistor. Fall time of the output is reduced by the capacitor connected to the right grid. The capacitor provides a low-impedance path for grid current for a short time, thus enabling the tube to draw more plate current to drop the plate voltage more quickly. The nominal rise and fall times of the output of the amplifier are 0.15 microsecond and 0.3 microsecond, respectively. The diode on the cathodes prevents damage to tubes if one half or the other is pulled out (the half tubes are not necessarily in the same envelope) by preventing the cathode from falling below -30 volts. Delays are produced by this circuit in much the same manner as in the inverter, and they may be estimated as roughly two-thirds of the rise and fall times of the input transition.

Amplifier as a Clipper

Although the amplifier is not generally thought of as a clipping type of circuit, it may be used for that purpose. Figure B42a shows that the circuit for which the data were taken amplifies only input signals in the approximate region ED, and that any noise or imperfections in input signal that exist in the operation regions do not appear in the output voltage.

NOTES





NOTE: This diagram refers to pluggable units 0341 and 0342. Dotted lines, values in parentheses, and X apply to 0342 only.

FIGURE B46. DRUM AMPLIFIER (A_D)

2.04.02 Shaping Amplifier (A_A)

This component was assigned to 701 electrostatic memory and is not used now.

2.04.03 Drum Amplifier (A_D)

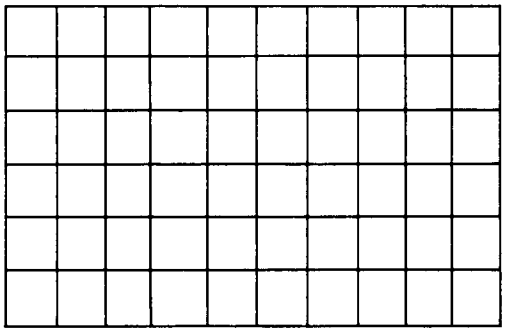
A_D stands for the drum amplifier circuits (Figure B46). This circuit is popularly referred to as the main amplifier (abbreviated main-amp). The voltage amplifier portion of the main-amp is a three-stage, capacitively-coupled circuit. The input to the circuit is connected to the common-plate load resistor of 10K for the four pre-amps which feed the main-amp. The first two stages are biased to ground, and the third is biased to -92 volts with respect to ground. Each plate is bypassed with a RC-decoupling circuit to keep interaction between stages at a minimum. In addition, the cathode return for the third stage is also decoupled.

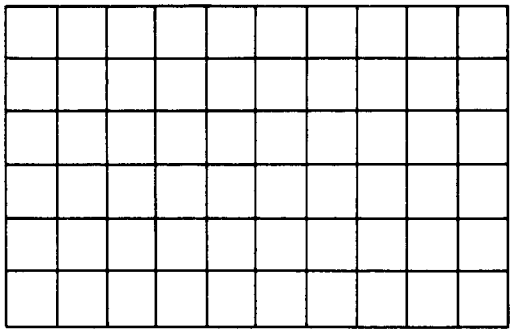
The fourth stage of the circuit is merely a cathode follower with a grid input biased at -10 volts. With a five-volt rise through the circuit, the output swings around -5 volts. In the case of the main-amps that feed the timing or index pulse shapers, the input to the cathode follower is biased at -54 volts, and the output swings around about -50 volts. This change is indicated by an X placed above the output line on the block symbol.

All stages of the amplifiers use cathode degeneration for the purpose of insuring best operation and for providing gain stability. The approximate gain of the first stage is eleven; that of the second stage, seven; that of the third stage, four. The over-all gain of this circuit and the PA should be at least 2000.

2.04.04 Amplifier (A_E)

This component was assigned to the 701 field tester only (section 2.01.11, Book B).





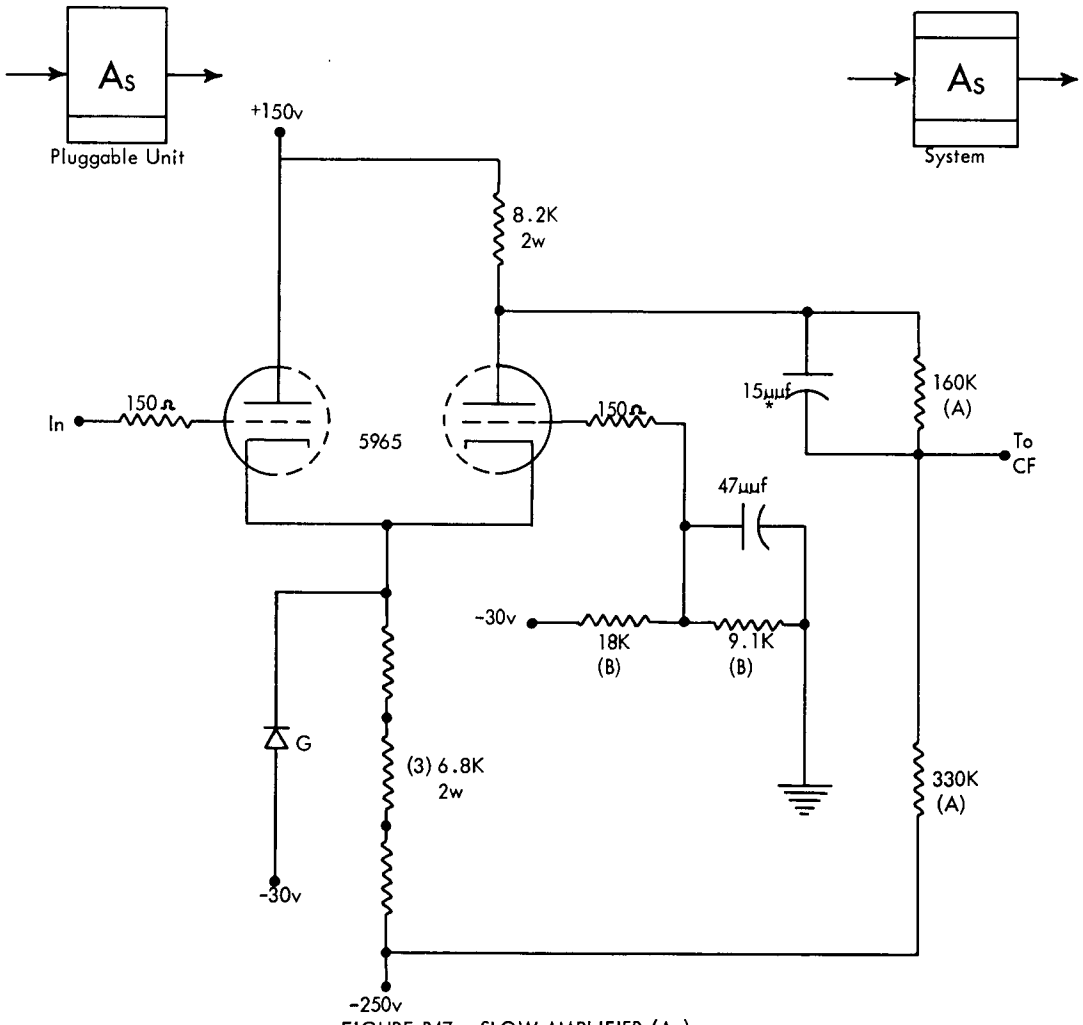


FIGURE B47. SLOW AMPLIFIER (A_S)

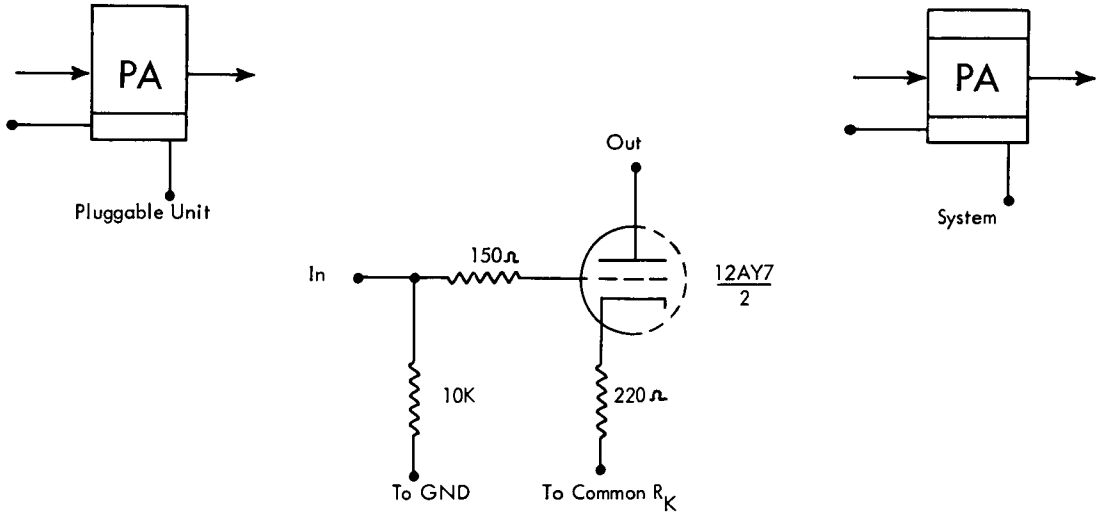


FIGURE B48. PRE-AMPLIFIER (PA)

2.04.05 Slow Amplifier (A_S)

When the speed of the grounded-grid amplifier is not needed, a slow amplifier, A_S (Figure B47) is used. The only difference between this circuit and the amplifier A (Figure B45) is the absence of the coil and its shunting resistor from the plate circuit. The rise time of the plate voltage is about 0.5 microsecond and the fall time, as in the amplifier, is about 0.3 microsecond. (The coil does not affect fall time). Delay and voltage values are the same as for the amplifier.

2.04.06 Clamp Power Amplifier (CPA)

The clamp power amplifier, CPA, (Figure B49) resembles the SPA. Since the pulse is of a shorter duration, plate-current-limiting resistors are not needed, and the plate is connected directly to the pulse transformer primary. Peaking is present in the negative direction for this circuit, but a damping resistor is not needed, since the tubes are sufficient for this purpose. The master clamp (sometimes called the inverted clamp) pulse is shown as it enters the 90-ohm transmission line. The pulse transformer is used here for the same reasons that the pulse transformer is used for the inverted sync pulse.

2.04.07 Differential Amplifier (DA)

This component was assigned to 701 electrostatic memory and is not used now.

2.04.08 Pre-Amplifier (PA)

PA is the symbol for a drum pre-amplifier circuit (Figure B48). Each pre-amplifier circuit (abbreviated pre-amp) is incomplete within itself. The four pre-amps, one for each drum, for each track are located adjacently in one pluggable unit and feed a common plate load resistor of 10K. This can be seen as the resistor connected to the input in Figure B46, the schematic of A_D. The two pre-amps in each pluggable unit associated with the same drum have a common 27K cathode resistor connected to 100 volts. In addition, this common connection may be connected directly to ground by read relay switching. The line shown on the block directly below the input line indicates the special ground return for the 10K resistor in the input to the pre-amp.

Since the pre-amps are designed to operate satisfactorily with input signals of the order of 10 to 40 millivolts, they must be relatively free from noise. Two precautions are taken to prevent excessive noise. The first is careful placement of the ground returns in the pluggable unit. The second is the selection of the 12AY7 tube for the pre-amps. This tube is carefully manufactured with special attention given to the reduction of microphonics, internal noise, and hum. Degenerative feedback is provided by the 220-ohm resistor in each cathode circuit to assist class A operation and to stabilize gain.

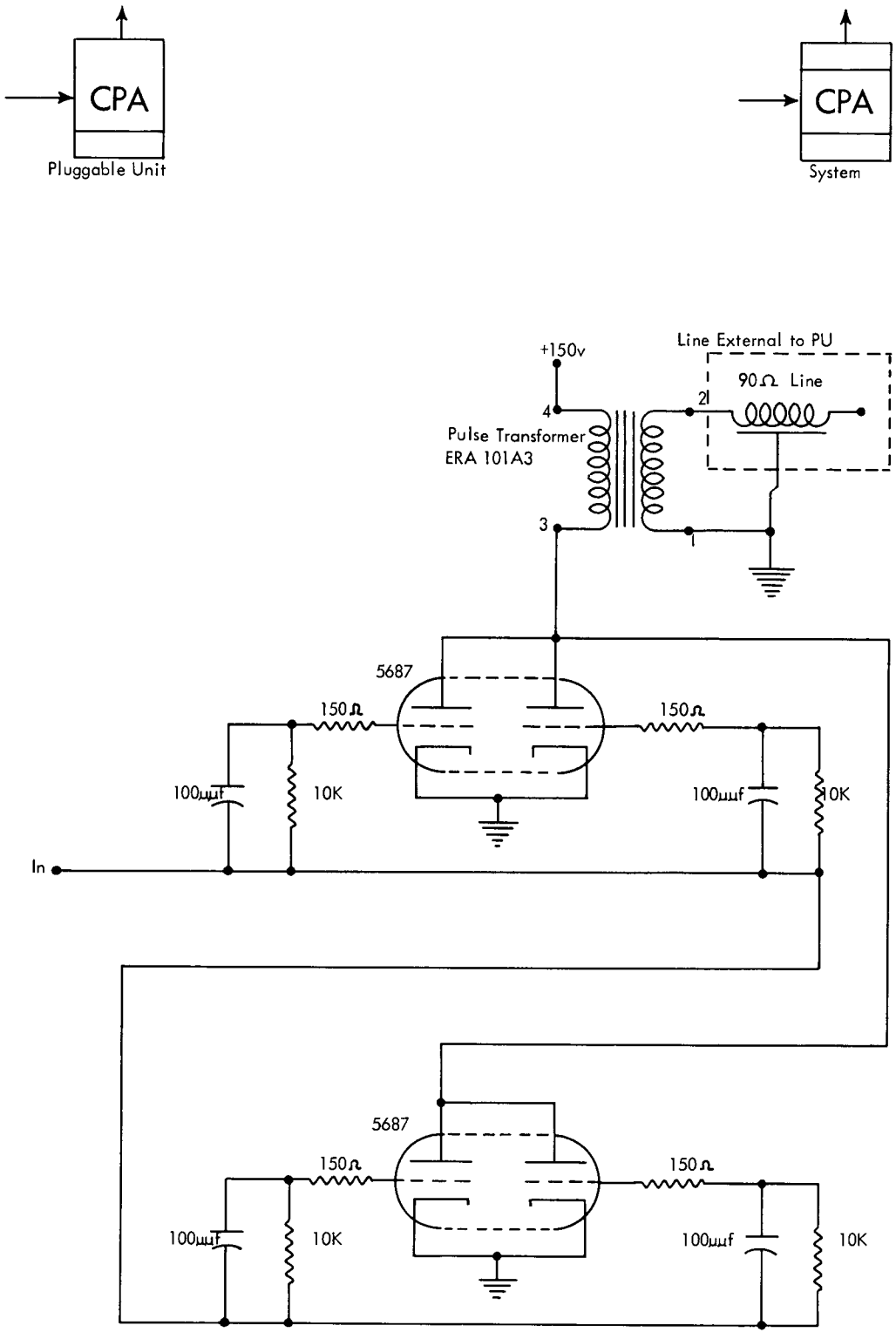


FIGURE B49. CLAMP POWER AMPLIFIER (CPA)

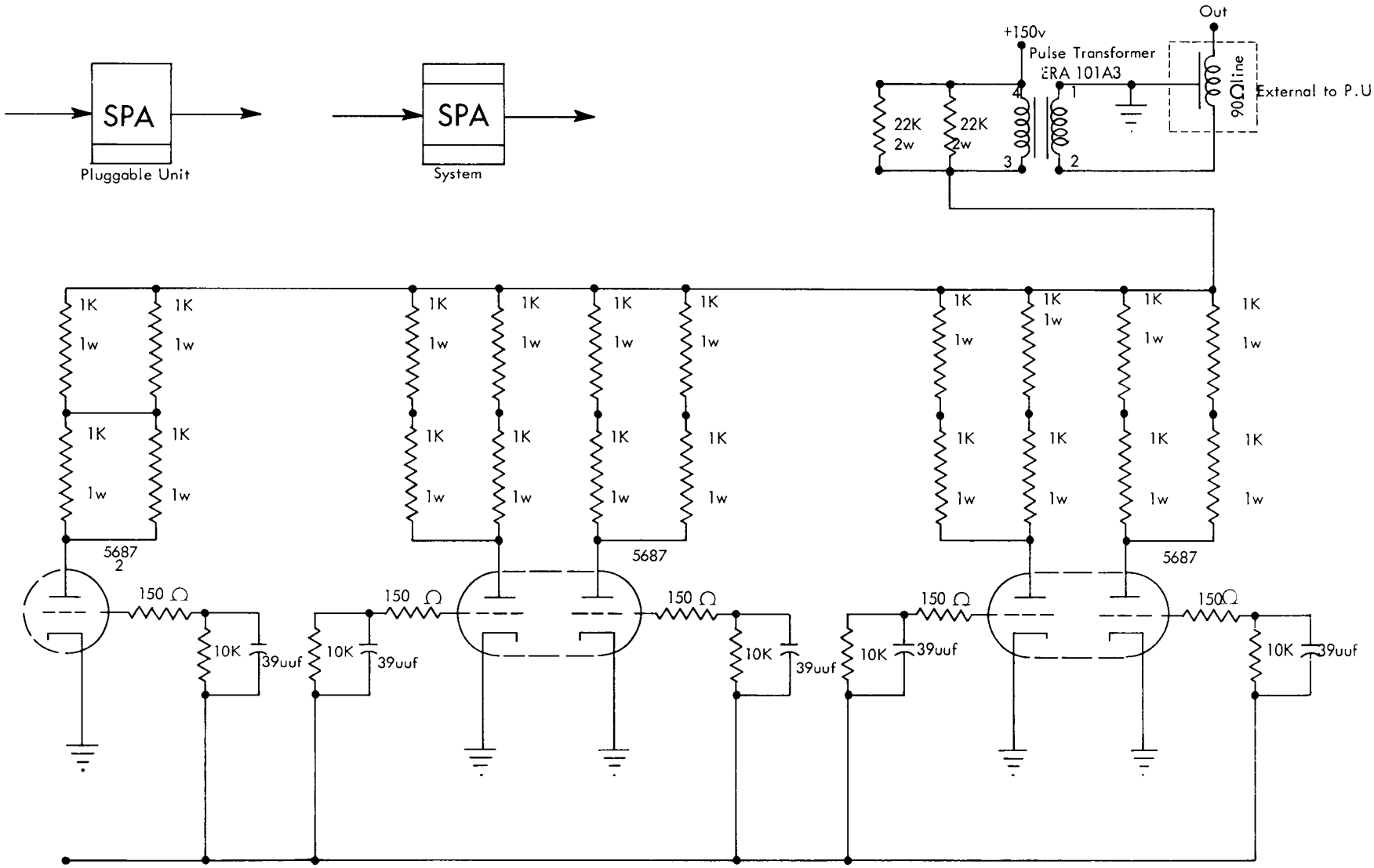


FIGURE B50. SYNC POWER AMPLIFIER (SPA)

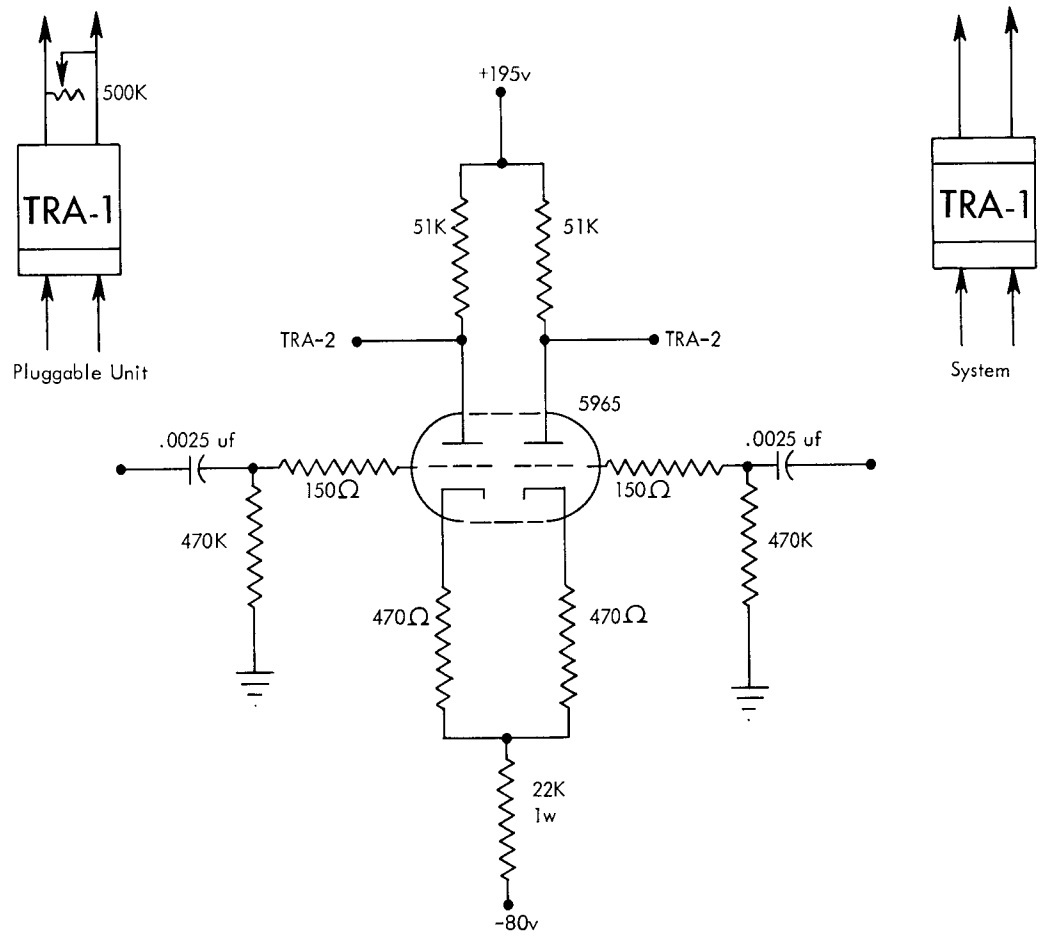


FIGURE B51. TAPE READ AMPLIFIER 1 (TRA-1)

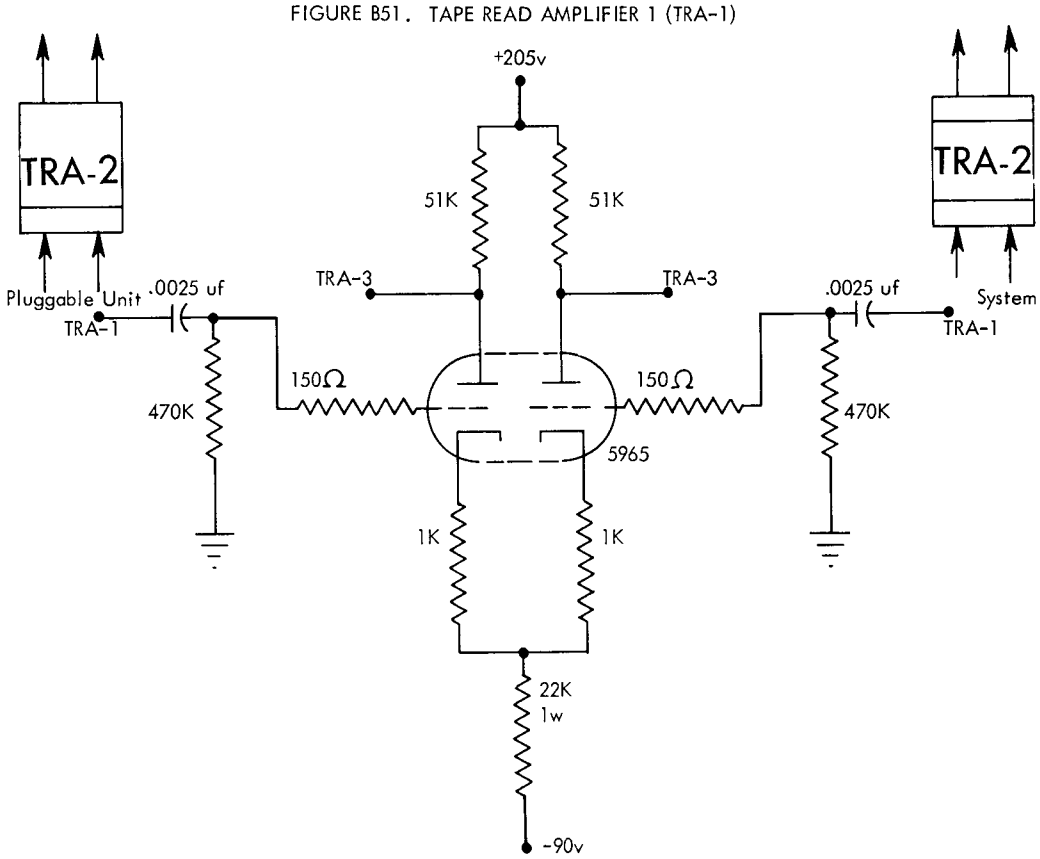


FIGURE B52. TAPE READ AMPLIFIER 2 (TRA-2)

2.04.09 Sync Power Amplifier (SPA)

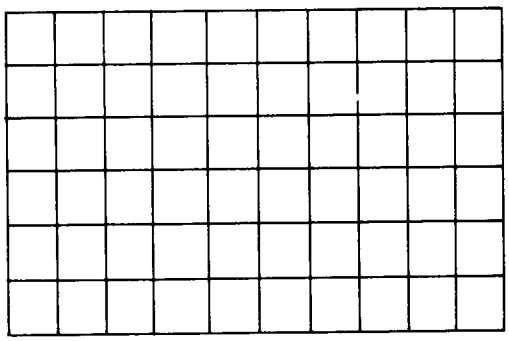
The sync power amplifier, SPA, (Figure B50) drives the pulse transformer which feeds a transmission line carrying the master sync pulses. Parallel inverters, with a small plate load resistance to limit current, make up the amplifier. The primary of the transformer, shunted by a 1.1K damping resistance, is also located in the plate circuit. This transformer is needed for isolating the plate potential from the transmission line, for impedance matching, for inverting the signal, and for providing the proper signal amplitude to the transmission line. This circuit does considerable peaking; therefore, the plate voltage rises considerably above the +150v plate voltage supply level. The master sync (sometimes called inverted sync) pulses output from the pulse transformer is fed through 90-ohm, coaxial transmission line to the sync inverters in the arithmetic column units. This entire group of circuits for master sync pulse generation is used to give the proper pulse amplitude, width, and shape (especially the sharp rise of the output) to the master sync pulse and to drive the circuits mentioned previously.

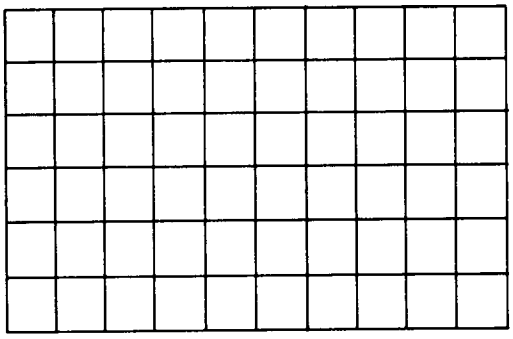
2.04.10 Tape Read Amplifier 1 (TRA-1)

The first stage of the circuits is TRA-1 (Figure B51). It is a capacitively-coupled, push-pull amplifier employing degenerative feedback in the cathode circuit. The capacitive coupling is used to pass the read pulses, and to suppress 60- and 120-cycle noise from the read lines. The value of the resistor in the coupling circuits is chosen so that there will be no overshoot of the input pulse, and so that the loading on the read pulse will not be excessive. The individual resistors in each cathode circuit supply degeneration to stabilize gain. The common cathode resistor is used for degeneration to reduce the gain of in-phase signals on the inputs. Because of the asynchronous nature of tape recording, wave forms appear quite blurred. The output of TRA-1 has a gain of about 12. Again, the reader must be cautioned that this is only a sample value for gain. The DC level on the plate is about +95 volts, and the cathode level is about +1 volt.

2.04.11 Tape Read Amplifier 2 (TRA-2)

The second stage of the tape amplifiers is TRA-2 (Figure B52), which closely resembles TRA-1. The gain of this circuit in this case is only about 10, since the resistor in the cathode circuit is larger, while the plate resistors are the same. The potentiometer between plates is used to control the gain of this stage and thus the overall gain. In TRA-2, the DC level of the plate is also about +95 volts, but the cathode level is around +2.5 volts.





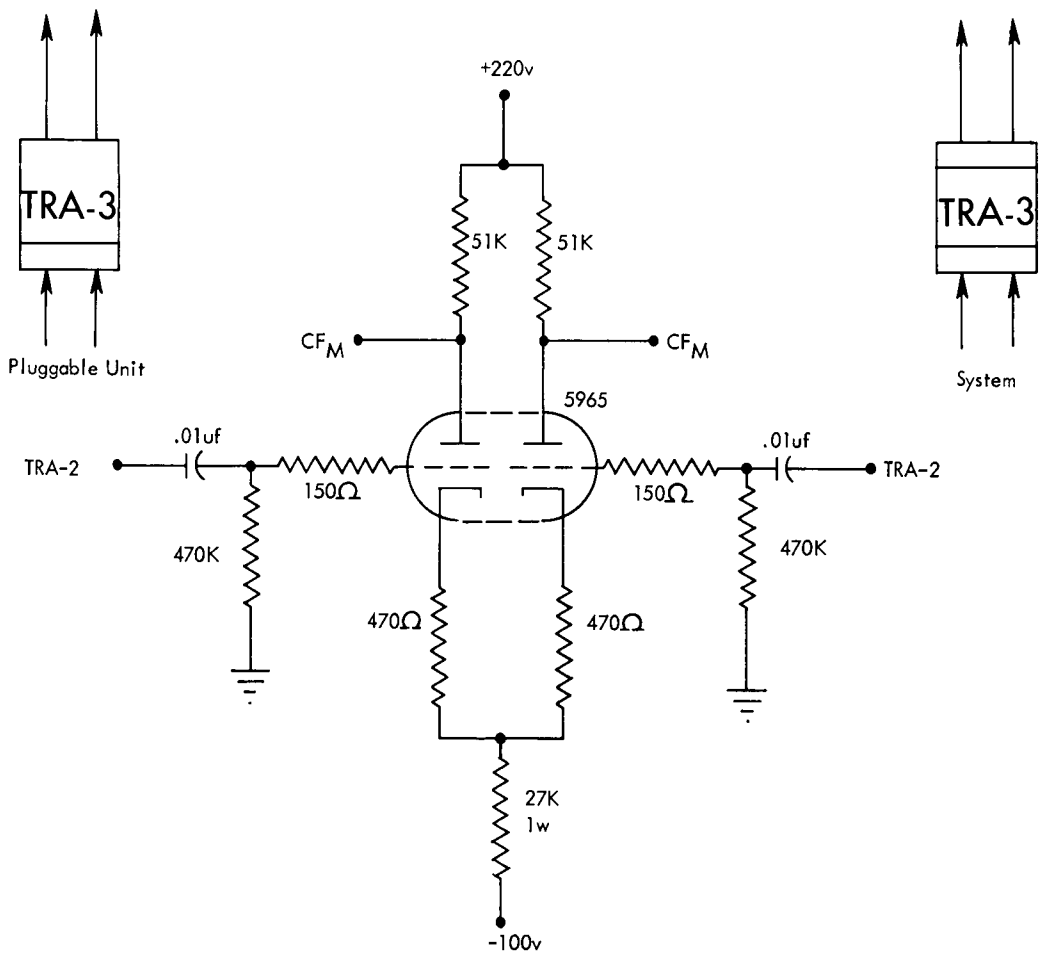


FIGURE B53. TAPE READ AMPLIFIER 3 (TRA-3)

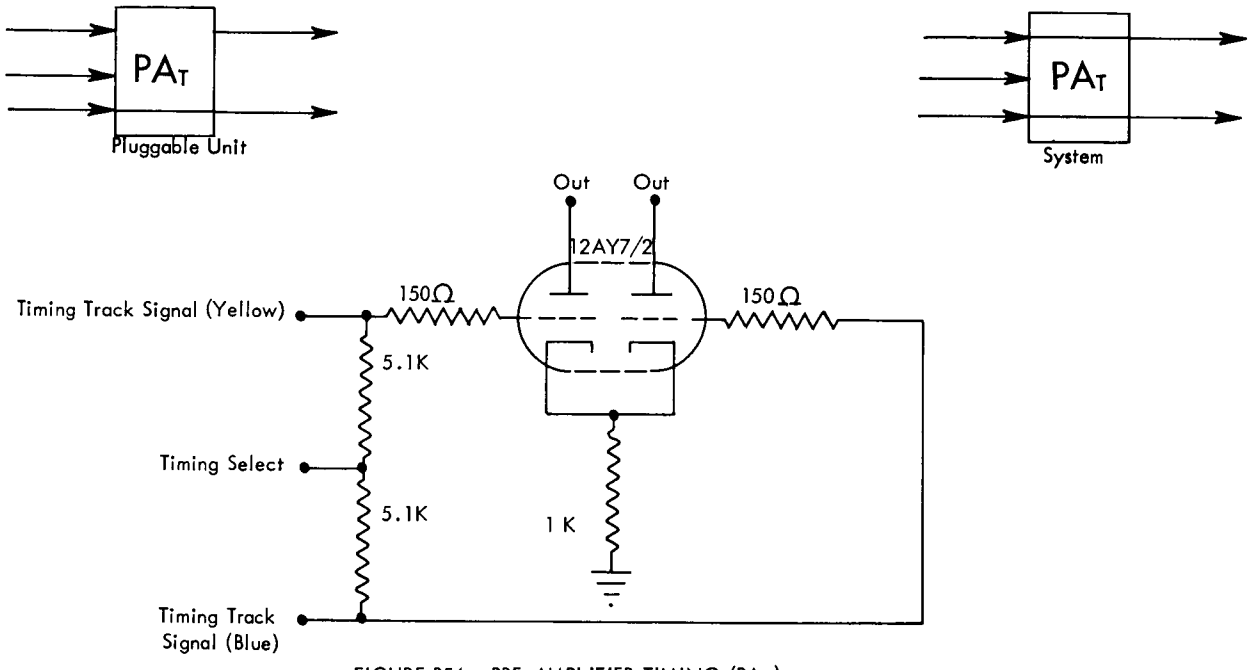


FIGURE B54. PRE-AMPLIFIER TIMING (PA_T)

2.04.12 Tape Read Amplifier 3 (TRA-3)

The third stage of the tape amplifiers is TRA-3 (Figure B53), which closely resembles the other two amplifiers. Since by now the signal-to-noise ratio is relatively large, the coupling capacitor is larger. An approximate gain for this circuit is 20. The plate level is about +120 volts, and the cathode is about +4 volts.

Since these three amplifiers are push-pull with cathode degeneration, a loss of signal from the output of one of the first stages will not be seen easily at the output of the TRA-3. Signal amplitudes at the plates of TRA-3 should be relatively equal, and any great inequality may indicate possible faulty operation in earlier stages. The overall gain of the tape amplifier circuits should be at least 2000.

2.04.13 Video Amplifier (VA)

This component was assigned to 701 electrostatic memory and is not used now.

2.04.14 Amplifier (CPA_T)

This component was assigned to the 701 field tester only (section 2.01.11, Book B).

2.04.15 Amplifier (SPA_T)

This component was assigned to the 701 field tester only (section 2.01.11, Book B).

2.04.16 Amplifier (DA_T)

This component was assigned to the 701 field tester only (section 2.01.11, Book B).

2.04.17 Amplifier (BSA)

This component was assigned to the 701 field tester only (section 2.01.11, Book B).

2.04.18 Pre-Amplifier Timing (PA_T)

PA_T is the symbol for a drum timing pulse pre-amplifier (Figure B54). There are two of these in the 733, one for each physical drum. These two circuits components are located in the same pluggable unit. This circuit operates similarly to the differential amplifier, DA. The output of this circuit is fed to the timing pulse amplifier which furnishes the plate load for the PA_T. The timing track signal is fed to the grids of the PA_T from the read winding of the timing track read/write head. The read winding is not grounded directly but through resistors in the switch timing circuit ST. During reading from or writing on the drum, the timing track must be read. This presents no problem on reading from the drum. On write, since all 36 heads are impulsed at the same time, the induced voltage in the timing track read windings and associated circuits is large. The effect of this voltage is to drive the two input grids of the PA_T in phase. The output of following circuits depends on the difference in voltage appled to the grids of the PA_T. No output will come with in-phase voltages. This induced voltage is further compensated for by the 1K negative feed-back resistor

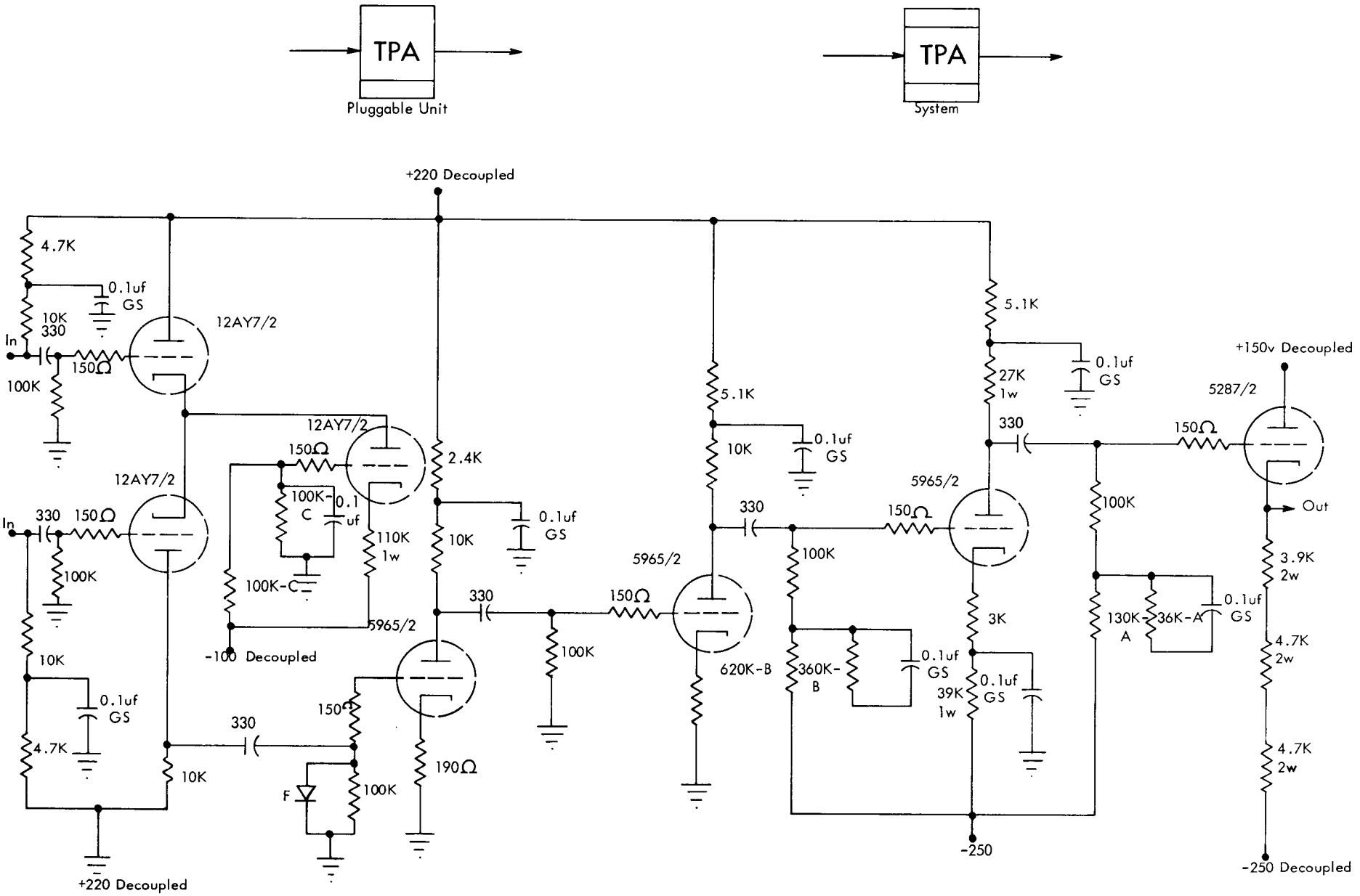


FIGURE B55. TIMING PULSE AMPLIFIER (TPA)

in the cathode of the PA_T. The output of this circuit is also affected by the difference in the mu of the two halves of the same tube. The signal applied to one grid might cause a larger current to flow than when it is applied to the other grid. If a push-pull signal is applied to this circuit, the total plate current should be the same as when no signal is applied. As one half of the tube conducts more, the other should conduct less by the same amount. If this is not the case, as in the case when the two mu's are different, common mode variation occurs. This condition is compensated for in the R_K and in circuits to follow this stage.

2.04.19 Timing Pulse Amplifier (TPA)

The TPA is shown in Figure B55. Except for the input stage, this amplifier is similar to the drum amplifier (AD). The output of this stage is developed across the 10K resistor in the lower half of the first duo-triode circuit. Now, if the voltages induced from the write circuits are large enough, some of this voltage is fed through the PA_T into the first stage of the TPA. This voltage, along with the common mode variation is fed into the two input terminals approximately in phase. Consider an instance when the two grids take a positive excursion. The top half of the tube, being a cathode follower, pulls the cathode in the positive direction. This cathode shift is about the same in magnitude as the input shift. This same shift is also applied to the lower half of the tube. Both grid and cathode go positive by the same amount. The current across the 10K plate resistor changes very little. The unwanted signal is rejected.

It might appear that a positive or negative shift being applied to both grids of the tubes would cause an increase in the total cathode current. If this were true, the selected operating point for the tube would be left. The triode in the cathode circuit prevents this. This circuit is a constant current device. If the plate of this constant current tube is pulled more positive, as in the case mentioned above, this tends to increase the current being drawn through the tube. This increased current increases the voltage drop across the 110K resistor in the cathode of the tube. With the grid voltage fixed by the divider network at about -50 volts, this positive shift of the cathode tends to decrease the current being drawn through the tube. This tends to keep the total current being drawn through the three tubes constant. The best operating point can be maintained in this manner. The apparent cathode resistor is high. This gives a nearly linear output for the differential input signal.

Consider now an instance when the lower input receives a positive shift and the upper input receives a negative shift. The upper tube, the cathode follower, applies a negative shift to the cathode of the lower tube, the amplifier. The input to the lower tube is positive. The two signals being applied to the grid and cathode out of phase tend to cause all the current through the tube circuit to be drawn through the lower tube and the constant current source tube. This causes a negative shift to be developed at the plate of the amplifier or lower tube. This shift is fed through the 330-uuf capacitor into the grid of the next stage of the amplifier. From there, the pulse goes to the other amplifier stages and is powered by the output cathode follower.

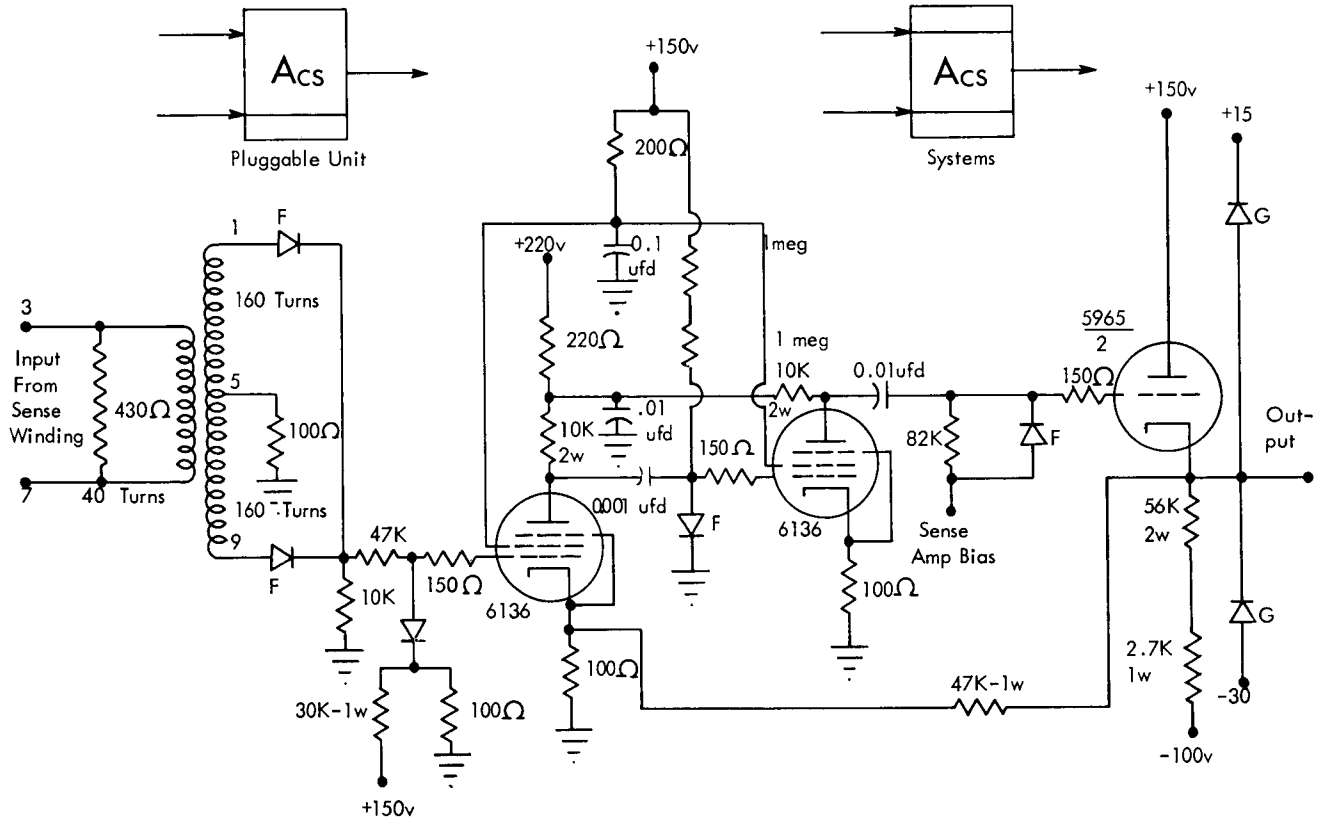


FIGURE B56. SENSE AMPLIFIER (A_{CS})

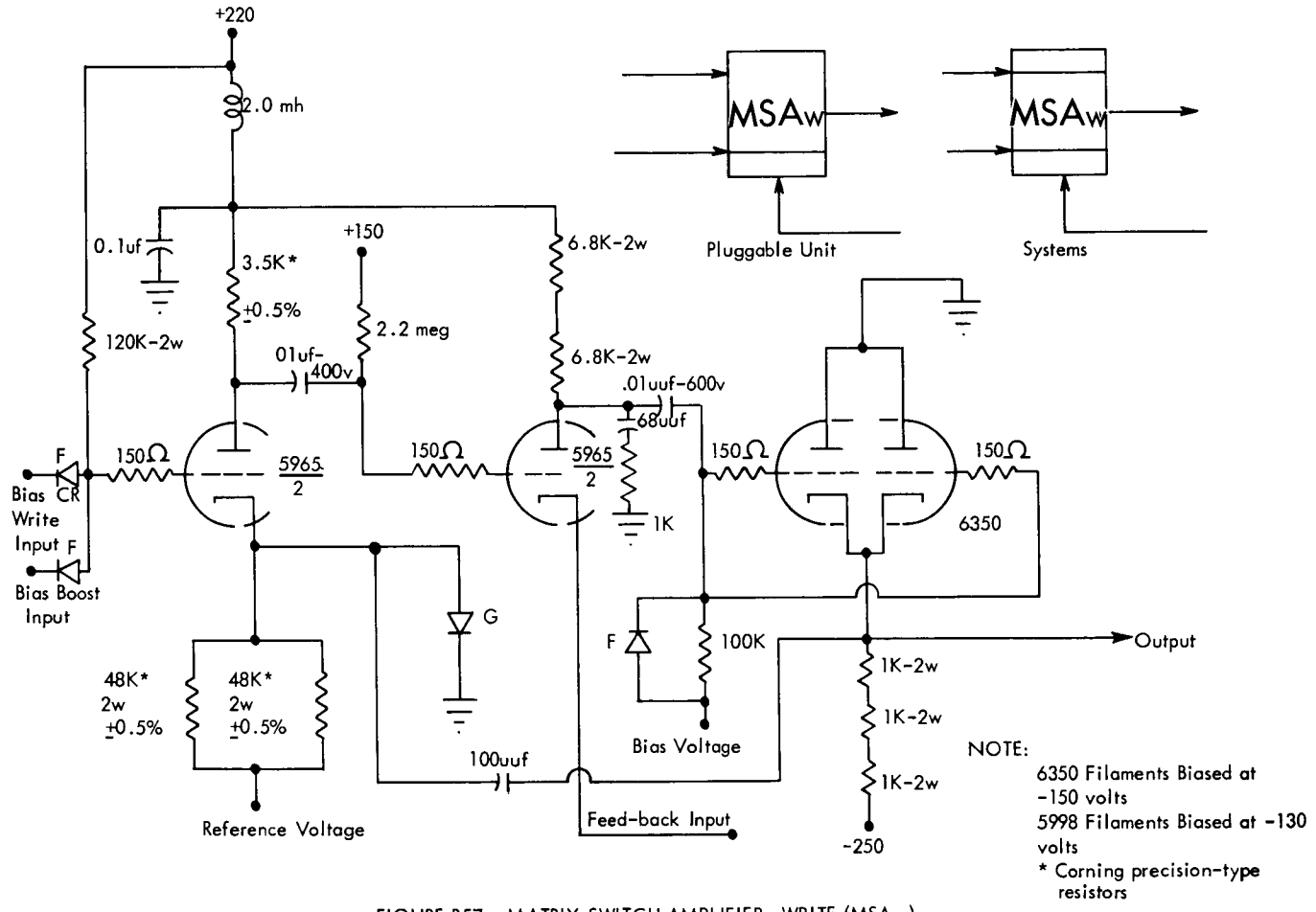


FIGURE B57. MATRIX SWITCH AMPLIFIER, WRITE (MSA_W)

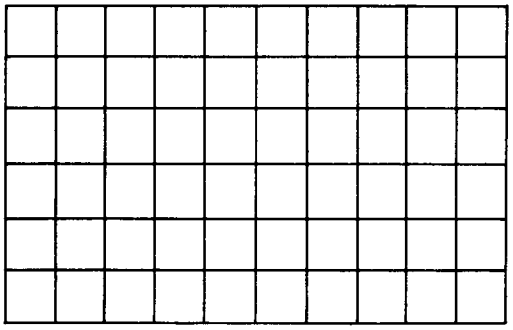
2.04.20 Sense Amplifier (A_{CS})

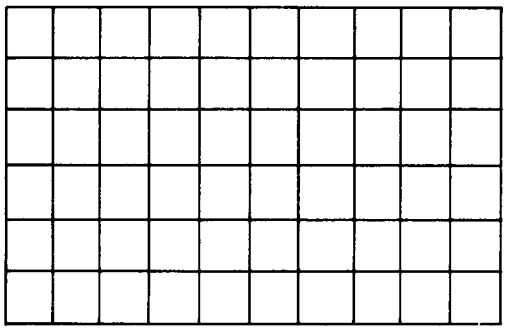
A_{CS} is the symbol for the core storage sense amplifier (Figure B56). The ends of the sense winding are connected to the primary of the input transformer. Any signal on the primary is amplified and detected at the output of the transformer. This appears as a positive signal applied to the grid of the first stage of the amplifier. This tube is already conducting lightly and this positive shift of the grid causes it to conduct more heavily. The output is fed through the 0.001-uf capacitor to the grid of the second stage of the amplifier. This signal, being negative, causes a positive output which is fed to the cathode follower output stage. This output at the cathode follower is clamped between -30 volts and +15 volts. To stabilize the gain, there is negative feedback between the output and the first amplifier stage cathode. This amplifier is used in the core storage unit. The output determines what is set in the storage buffer triggers on a read cycle.

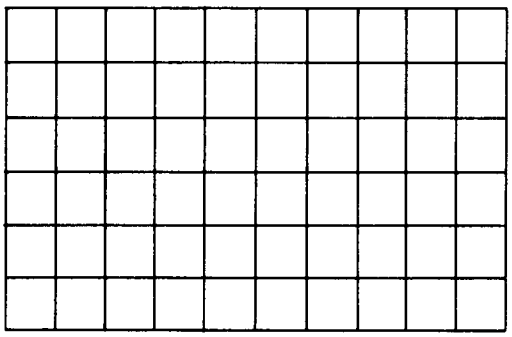
2.04.21 Matrix Switch Amplifier, Write (MSA_W)

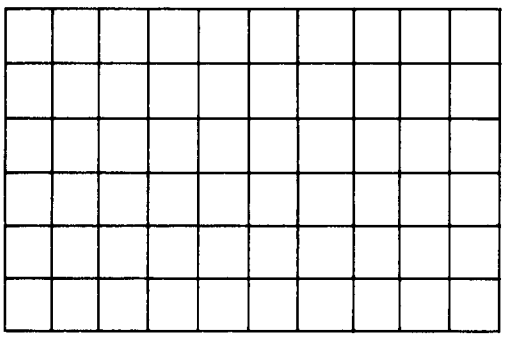
The MSA_W (Figure B57) is identical with the MSA_R (Figure B58) with two exceptions. First, of course, its function is different in that it is used to drive the P_2 switch core windings. Second, there is an additional input called bias boost. When this amplifier is being used for write, the bias boost input is clamped at ground, thereby allowing only 0 volts to be applied to the input.

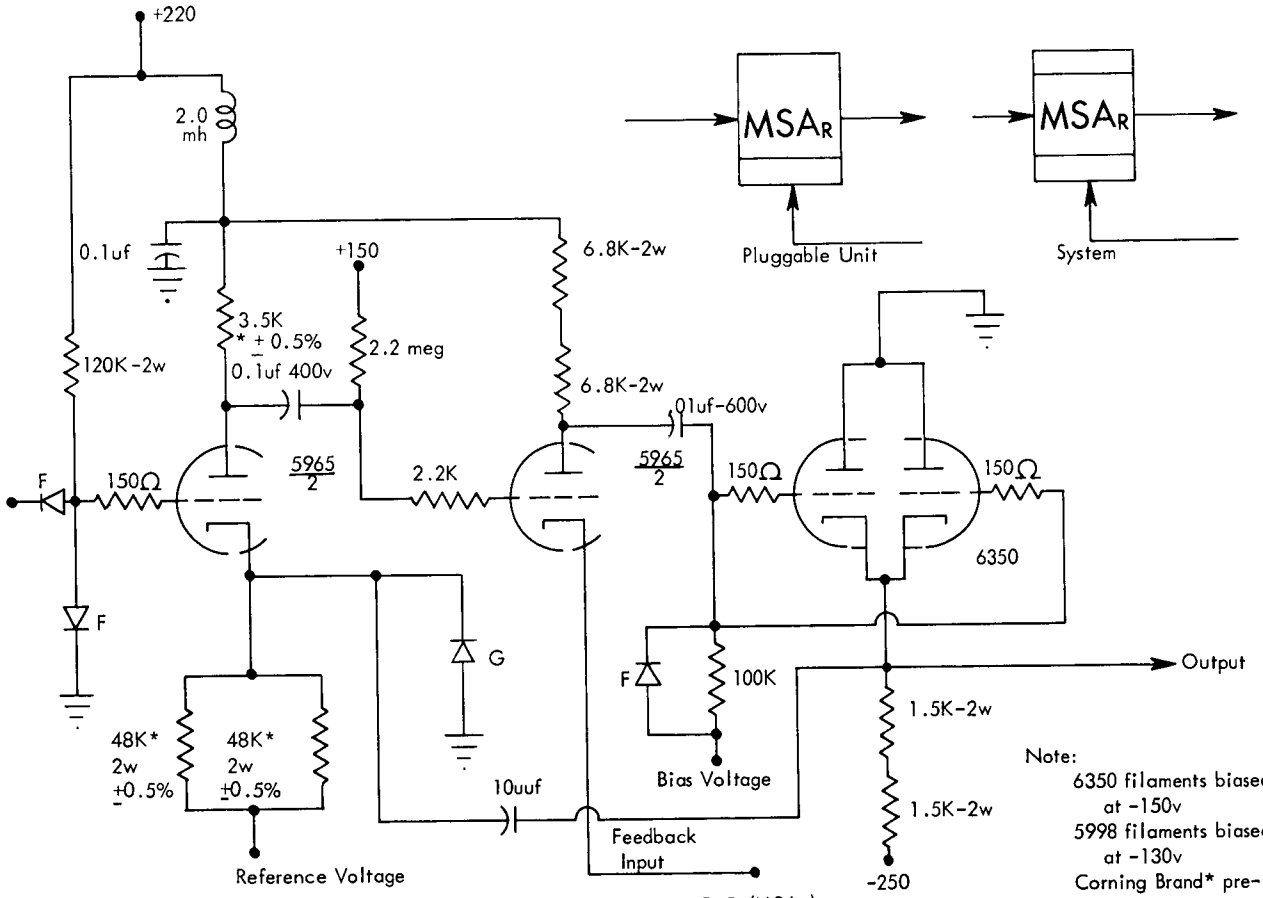
However, when the amplifier is used for read bias, the bias boost input comes up to +10 volts, allowing +10 volts to be applied to the input. The read bias boost is a safety factor, to make sure that no extra switch cores are flipped during the read portion of a use cycle.





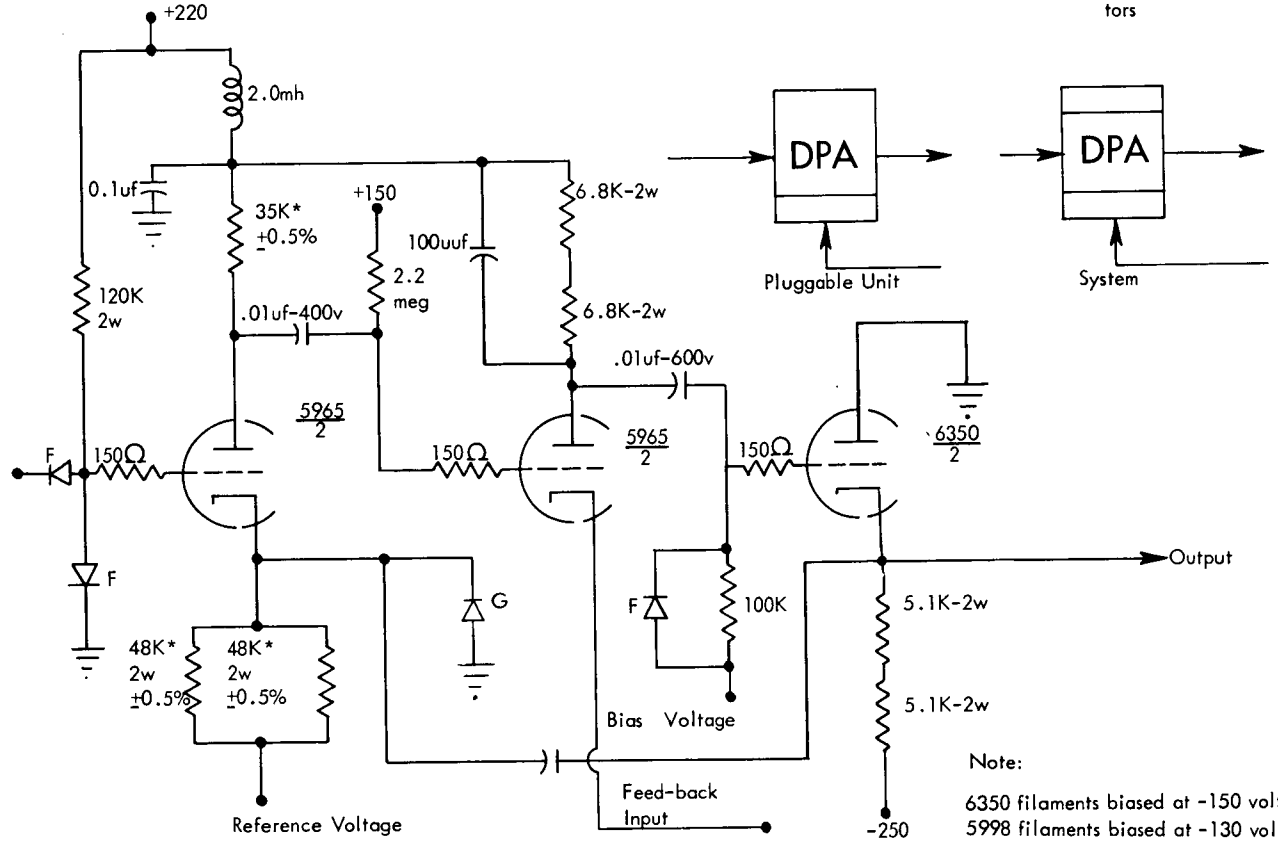






Note:
6350 filaments biased at -150v
5998 filaments biased at -130v
Corning Brand* precision-type resistors

FIGURE B58. MATRIX SENSE AMPLIFIER, READ (MSA$_R$)



Note:
6350 filaments biased at -150 volts.
5998 filaments biased at -130 volts
Corning Brand* precision-type resistors

FIGURE B59. DIGIT PLANE AMPLIFIER (DPA)

*Corning Brand is a registered trade mark of the Corning Glass Works, Corning, New York.

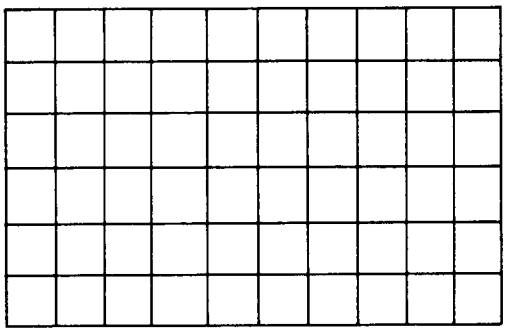
2.04.22 Matrix Switch Amplifier, Read (MSA_R)

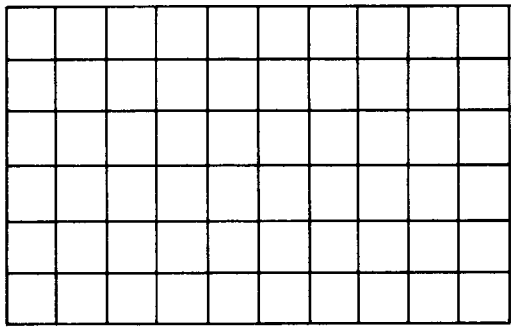
The MSA_R (Figure B58) is in the magnetic core storage unit. Its function is to amplify the read address decoder output to the proper levels for use at the input of the driver tubes. The MSA_R is very similar to the DPA (Figure B59) except that it drives the P1 windings of the switch cores rather than the inhibit windings. The slight component variation between the two circuits is caused by different load and duty cycle requirements.

2.04.23 Digit Plane Amplifier (DPA)

The digit plane amplifier (Figure B59) is used in the magnetic core storage unit. It provides the inhibit and the post-write disturb currents for the cores. Normally, the first stage of the driver amplifier is held at cut-off. The second stage is conducting and the output of the third stage is about -150 volts. The output or driver tube has its cathode tied to -100 volts so the driver tube is normally cut off. When a positive signal is applied to the input of the circuit, the first stage conducts giving a negative shift at its output. This is fed to the grid of the second stage (normally conducting) and cuts this tube off. This produces a positive output from this stage which feeds into a cathode follower. This cathode follower output is DC-coupled to the grids of the driver tube. Now the driver tube conducts, causing current to flow in the digit plane winding of the cores. From the output stage, a negative feedback voltage is obtained and fed into the cathode of the second stage of the circuit. This is done to stabilize the gain of the amplifier. Feedback between the cathode of the first and third stage is used to prevent oscillation. Precision type resistors are used in the first stage as the current in this stage is critical. The plate swing of this first stage must be practically 20 volts.

The amplifier section of the digit plane driver circuit is located in a pluggable unit. The final stage or the driver tube is located in the driver panel.





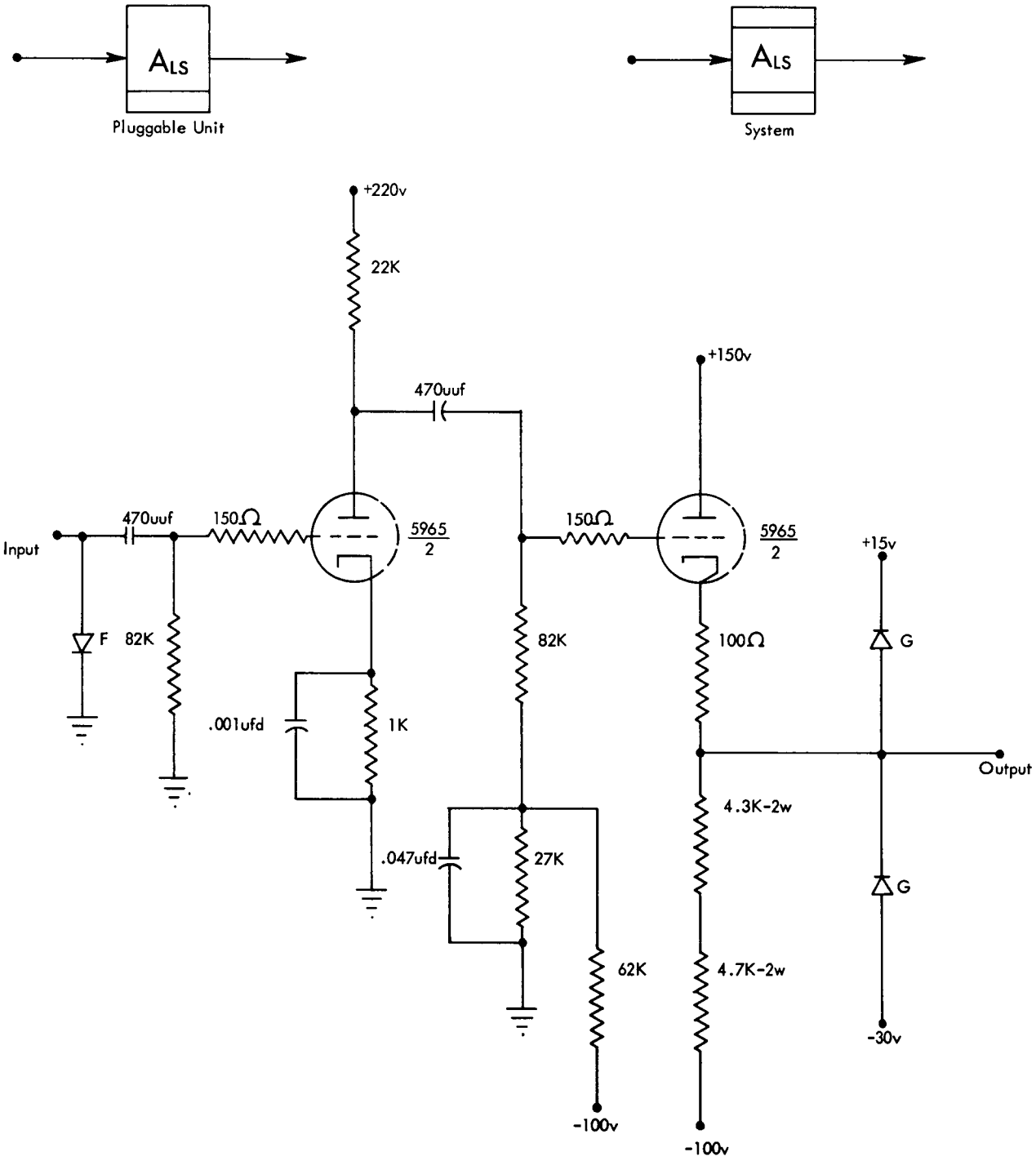


FIGURE B60. LEVEL SETTING AMPLIFIER (A_{LS})

2.04.24 Level Setting Amplifier (A_{LS})

The level setting amplifier (Figure B60) is a modified amplifier designed to convert the 0v to -5v outputs from the transistorized sense amplifiers to the +10v to -30v normal machine signal levels.

2.04.25 Matrix Switch Amplifier, Read X (MSA_{RX})

This component is the same as the MSA_R (Figure B58) with certain modifications compensating for the change in load caused by the increased number of ferrite cores in the memory array X lines.

2.04.26 Matrix Switch Amplifier, Read Y (MSA_{RY})

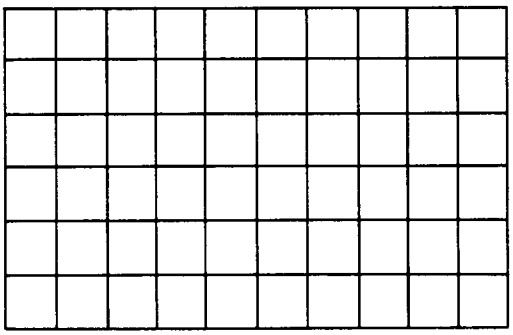
This component is the same as the MSA_R (Figure B58) with certain modifications to compensate for the change in load caused by the increased number of ferrite cores in the memory array Y lines.

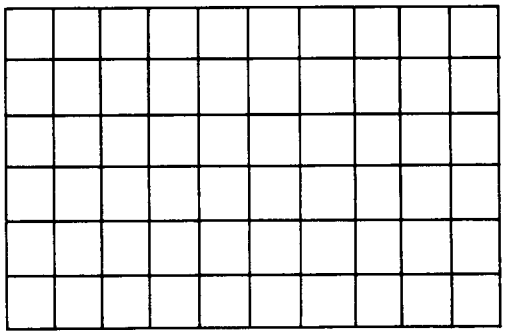
2.04.27 Matrix Switch Amplifier, Write X (MSA_{WX})

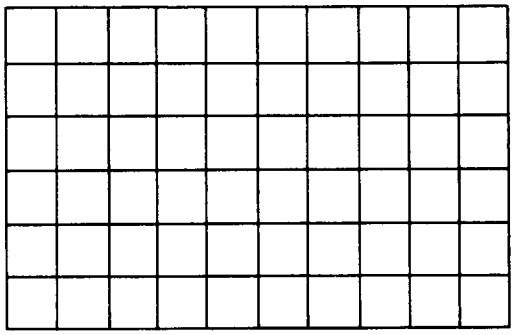
This component is the same as the MSA_W (Figure B57) with certain modifications to compensate for the change in load caused by the increased number of ferrite cores in the memory array X lines.

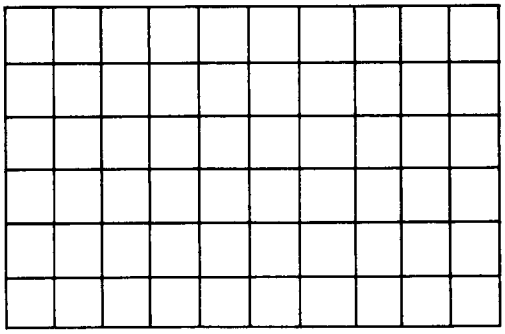
2.04.28 Matrix Switch Amplifier, Write Y (MSA_{WY})

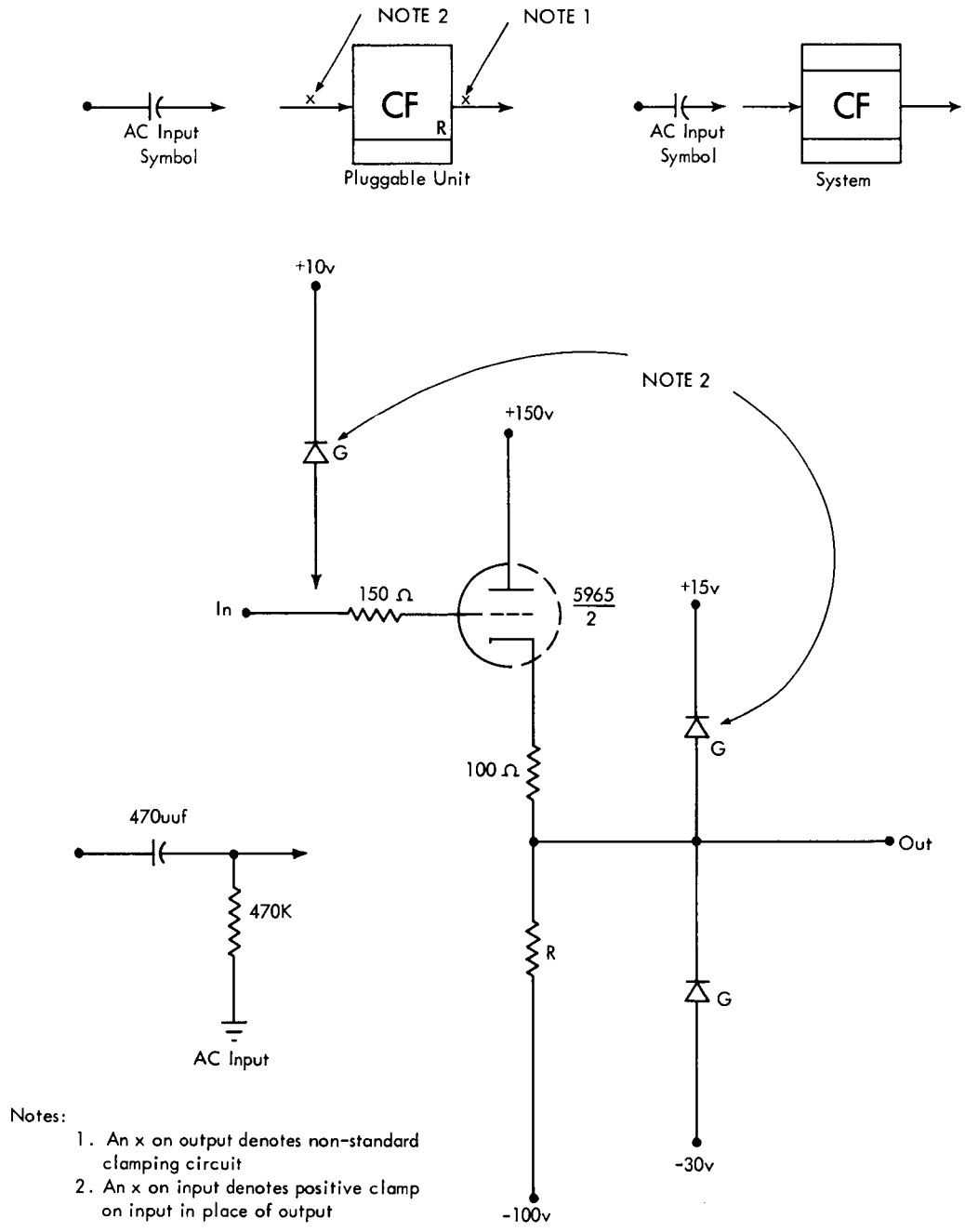
This component is the same as the MSA_W (Figure B57) with certain modifications to compensate for the change in load caused by the increased number of ferrite cores in the memory array Y lines.











Notes:

1. An x on output denotes non-standard clamping circuit
2. An x on input denotes positive clamp on input in place of output

FIGURE B61. CATHODE FOLLOWER (CF)

2.05.00 CATHODE FOLLOWERS

The operation of the standard cathode follower is discussed in section 2.09.00, Book A.

2.05.01 Cathode Follower (CF)

The standard cathode follower output contains two catcher diodes as shown in Figure B61. The diode connected to -30 volts protects the other catcher and the diodes following this circuit by clamping the output voltage to -30 volts when the tube is removed or when the cathode follower input goes very negative. This negative voltage catcher also helps set the standard, -30v output signal. The diode connected to +15 volts clamps the output at +15 when the input goes very high and thus protects the other diode or any diodes fed by this circuit from overvoltage. These two diodes actually protect each other. When cathode followers are paralleled, only needed diodes are used. In this case, enough +15 volt returned diodes are used to carry the 24 milliampere, zero-bias current for each 5965 half-tube. The -30v returned diodes must handle the clamping current through the equivalent cathode resistance when all tubes are removed. If the diode configuration for each tube-half is not exactly as shown on the schematic, then an **X** is placed above the output line on the pluggable unit block diagram. Then the actual configuration used is drawn on the block diagram following the cathode follower block. When crystal diodes are paralleled, a resistor (usually 100 ohms) is placed in series with each to tend to equalize the currents through each diode. Otherwise, a low forward resistance of one may cause it to pass more than rated current.

Inputs to a cathode follower may be drawn into the block at either side or the bottom, and the output should be from the opposite side from the input. An RC-coupled input (AC input) is sometimes used, and it is indicated by a series capacitor in the input line.

2.05.02 Cathode Follower (CF_B)

This component was assigned to 701 electrostatic memory and is not used now.

2.05.03 Cathode Follower (CF_D)

This component was assigned to 701 electrostatic memory and is not used now.

2.05.04 Cathode Follower (CF_E)

This component was assigned to 701 electrostatic memory and is not used now.

2.05.05 Cathode Follower (CF_L)

This component was assigned to 701 electrostatic memory and is not used now.

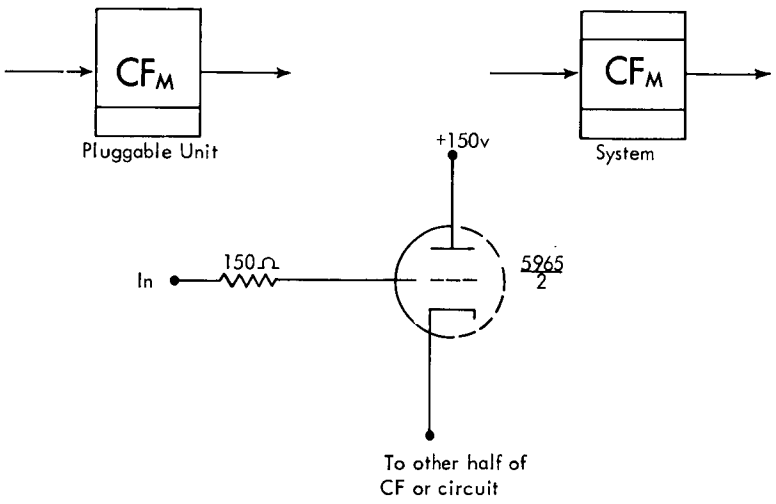
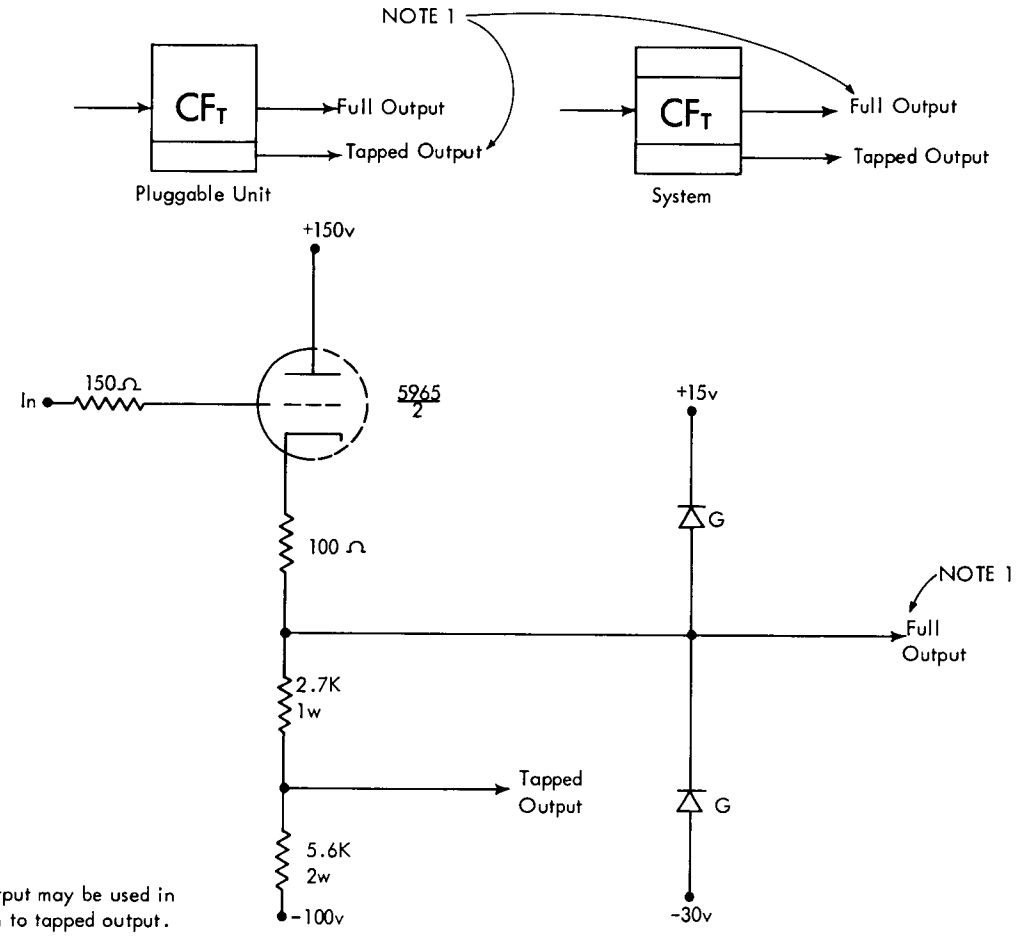


FIGURE B62. CATHODE FOLLOWER (CF_M)



Note: Full output may be used in addition to tapped output.

FIGURE B63. CATHODE FOLLOWER (CF_T)

2.05.06 Cathode Follower (CF_M)

In the 726 tape system, the CF_M (Figure B62) is used as a mixer where two CF_M's share a common load resistor and the inputs are the two push-pull outputs of the TRA-3. Noise is clipped by a variable bias on the grids of the CF_M's.

In core storage, the CF_M is used to drive a delay line and the load is the delay line's terminating resistor.

2.05.07 Cathode Follower (CF_S)

This component was assigned to 701 electrostatic memory and is not used now.

2.05.08 Cathode Follower (CF_T)

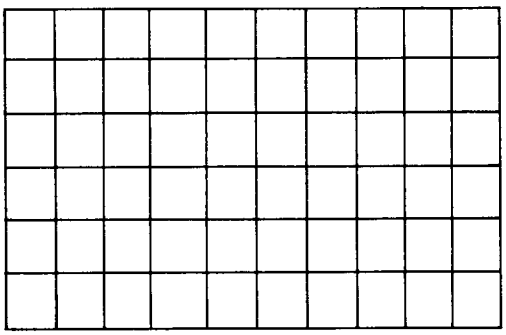
Cathode followers feeding binary inputs to triggers must have tapped outlets so that the binary inputs are not overdriven. CF_T is the symbol for the circuit (Figure B63) used for these applications. It is a standard cathode follower with the output taken between the 2.7K and 5.6K resistors in the cathode circuit. The 5.6K resistor is connected to -100 volts. This tapped output gives a nominal signal output of about -25.5 volts to -55.5 volts with +10 volts and -30 volts on the normal output. The clamp diodes are retained as connected in the standard circuit. There are some applications for this circuit where both the tapped and non-tapped outputs are used.

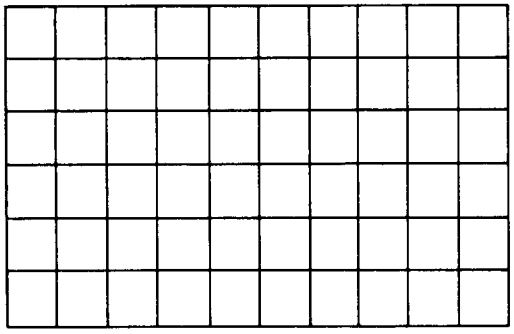
2.05.09 Cathode Follower (CF_Y)

This component was assigned to 701 electrostatic memory and is not used now.

2.05.10 Cathode Follower (CF_Z)

This component was assigned to 701 electrostatic memory and is not used now.





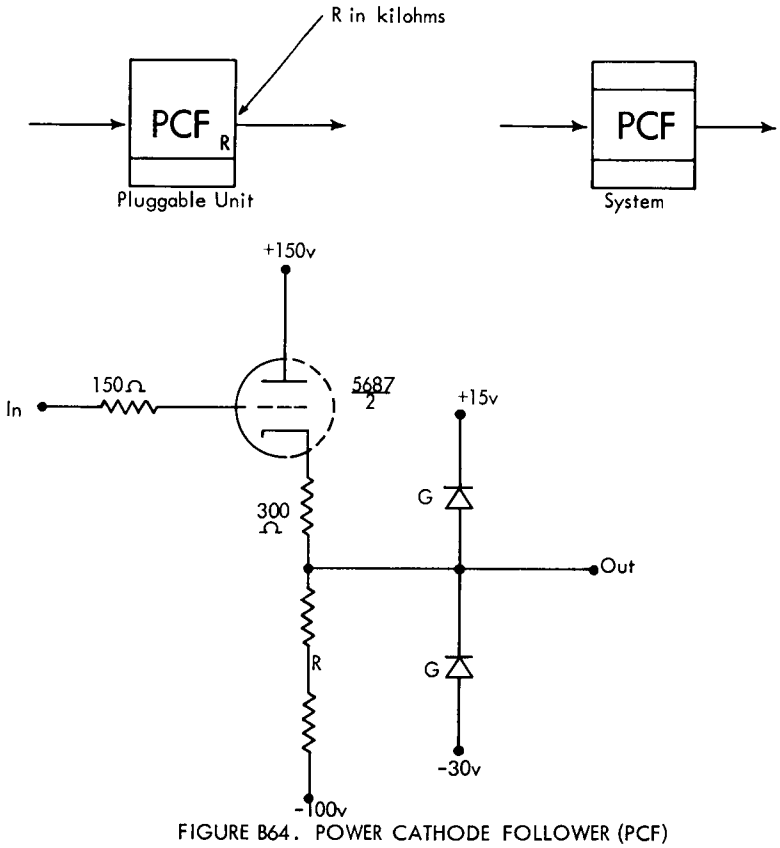


FIGURE B64. POWER CATHODE FOLLOWER (PCF)

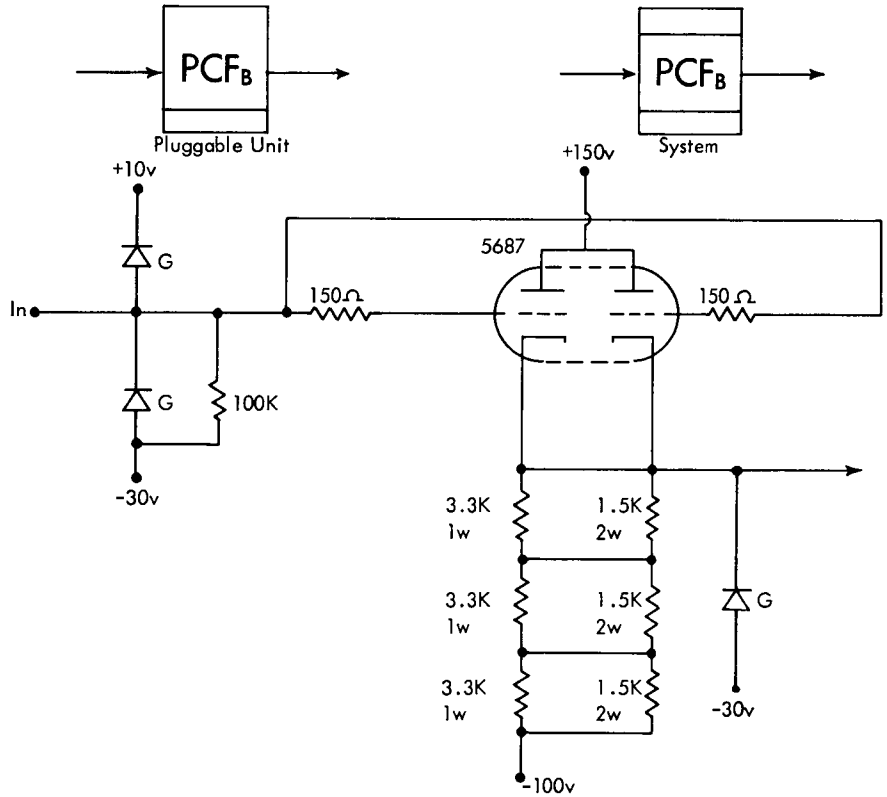


FIGURE B65. POWER CATHODE FOLLOWER (PCF_B)

2.05.11 Power Cathode Follower (PCF)

The power cathode follower PCF (Figure B64) operates similarly to the cathode follower (Figure B61). This circuit is called a power cathode follower because it uses a 5687 tube. The usual value of the cathode resistor is 6K and the usual value of the bias resistor is 300 ohms. The voltage rise through a PCF is greater than through a CF. Because of the tolerances allowed in testing 5687 tubes, the rise from a -30v input can be as much as five volts for an unloaded PCF with a 6K cathode resistor. With a +10v input, the output should also be +10 volts under the above conditions. The action of the PCF under capacitive loading is also similar to that of the CF. Power cathode followers may be paralleled; in this case, the 15v returned catcher diodes must be able to carry the 80 milliampere zero-bias current of each half-tube. If the diode configuration per half-tube is not identical to that shown in Figure B64, then the X is placed outside the block and the actual configuration is drawn upon the pluggable unit block diagram.

2.05.12 Power Cathode Follower (PCF_A)

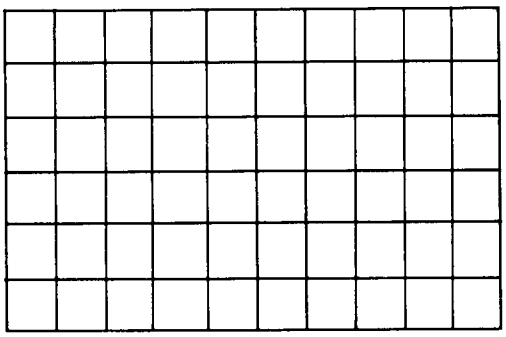
The power cathode follower PCF_A is a basic PCF (Figure B64) with the bias resistor left out.

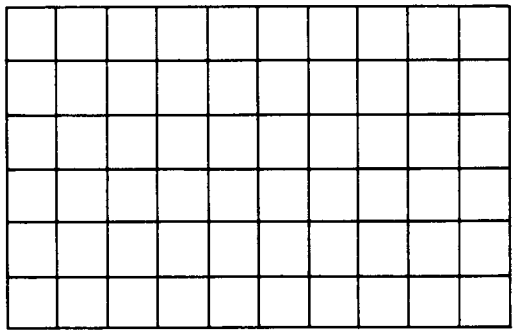
2.05.13 Power Cathode Follower (PCF_B)

The output from the sync clipper must be powered so that it may drive an inverter and also feed another pluggable unit. A special cathode follower, PCF_B (Figure B65), supplies this power. Its input diodes serve as DC restorers to keep the signal at a nominal +10v to -30v level. The equivalent cathode resistance is about 3.1K, 9 watts. A slight voltage rise is realized through the circuit. This output, called the inverted clamp input, feeds further shaping circuits for the sync pulse; it also feeds the clamp generator and the clock drive circuits.

2.05.14 Power Cathode Follower (PCF_C)

The inverted clamp input pulse also feeds a special cathode follower, PCF_C (Figure B66), that powers the clock drive pulses. Its input is conductively coupled. If the pluggable unit which feeds this unit is removed, the input is held to -30 volts. The capacitor across the cathode bias resistor speeds the rise of the output. This rise must be fast, because the clock drive is inverted to feed the binary input of a trigger. A larger fall time is obtained by the relatively large resistance of the cathode circuit. Dividing the cathode resistance sets the proper output level. The actual cathode levels are about five volts higher.





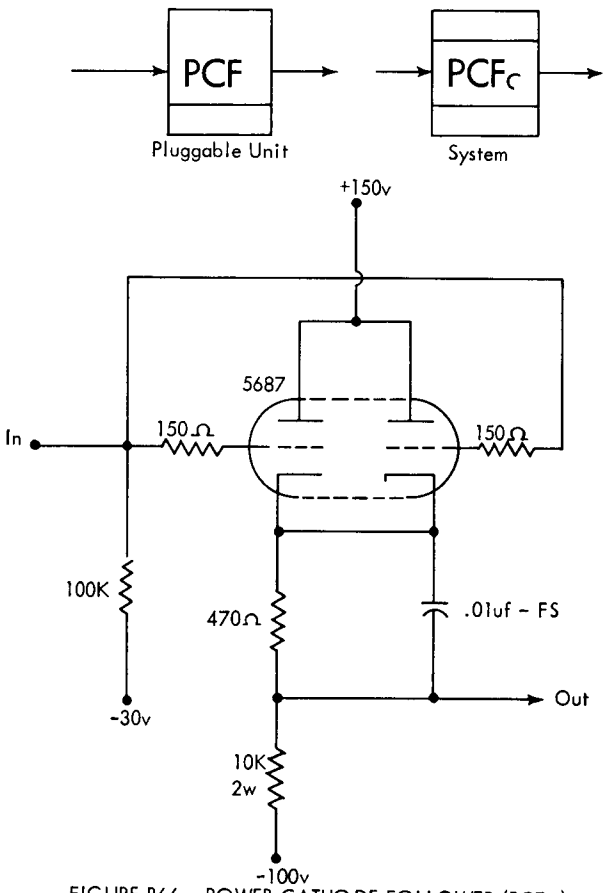


FIGURE B66. POWER CATHODE FOLLOWER (PCF_C)

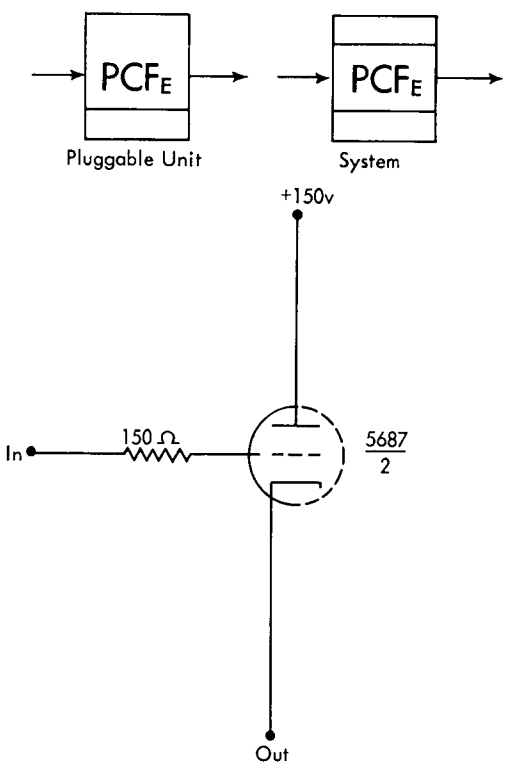


FIGURE B67. POWER CATHODE FOLLOWER (PCF_E)

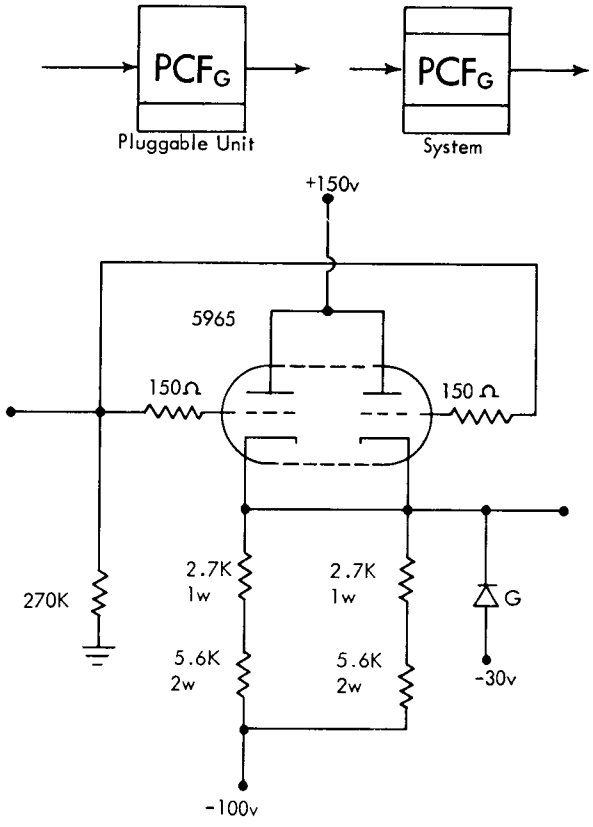


FIGURE B68. POWER CATHODE FOLLOWER (PCF_G)

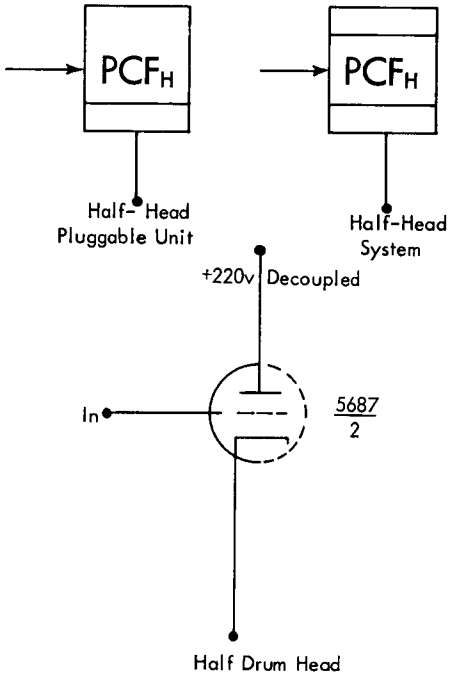


FIGURE B69. POWER CATHODE FOLLOWER (PCF_H)

2.05.15 Power Cathode Follower (PCF_D)

Except for the 470uuf and 220K RC coupling circuit on its input this cathode follower is identical to the power cathode follower PCF_P (Figure B71).

2.05.16 Power Cathode Follower (PCF_E)

The power cathode follower PCF_E (Figure B67) is a delay line driver and can be found driving the delay line on the input to the clock. The load resistor of the $2PCF_E$ is equal to the characteristic inpedence of the delay line and it terminates the input of the line.

2.05.17 Power Cathode Follower (PCF_F)

The PCF_F schematic is identical to the PCF_E (Figure B67) with the possible exception that the plate voltage may be +220 volts. This is indicated by an X in the upper right corner of the pluggable unit block. A decoupling circuit is used consisting of: (1) a 47-ohm resistor between the plate and +220 volts, and (2) a .05 ufd capacitor from the plate to ground.

The circuit is used to drive lines going through cables; the load resistor is at the other end of the cable.

2.05.18 Power Cathode Follower (PCF_G)

The oscillator output must be powered before it is fed into the sync generator. PCF_G (Figure B68) is a special cathode follower used for this purpose. It also serves as a level setter because: (1) its input contains part of a divider attached to the output of the master oscillator unit, and (2) its cathode circuit contains a clamp diode. The circuit is two parallel ordinary cathode followers with no bias resistors. A slight voltage rise through the circuit can be expected.

2.05.19 Power Cathode Follower (PCF_H)

The special circuit used for writing the timing track on the drum is PCF_H (Figure B69). This circuit is used instead of the I_W because a short recovery time is needed to write one pulse every twelve microseconds. Although the output voltage wave form does not have large peaks, the current is such that pulses of flux are written upon the drum. The output of the head when reading the timing track looks like that of an information track when the drum is reading all ones. A large current pulse is obtained by the use of 5687 tubes and 220 volts for a plate voltage supply.

2.05.20 Power Cathode Follower (PCF_M)

This component was assigned to 701 electrostatic memory and is not used now.

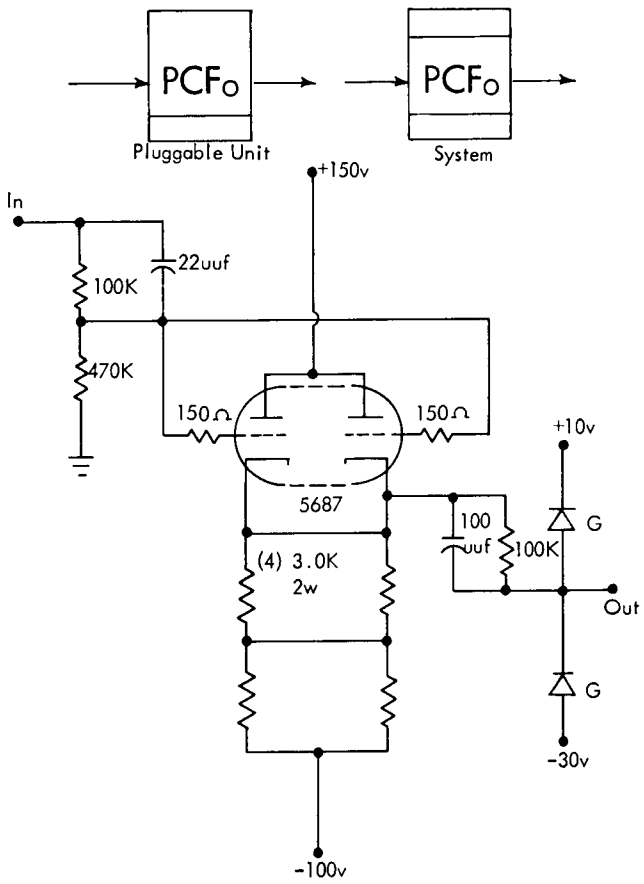


FIGURE B70. POWER CATHODE FOLLOWER (PCF_O)

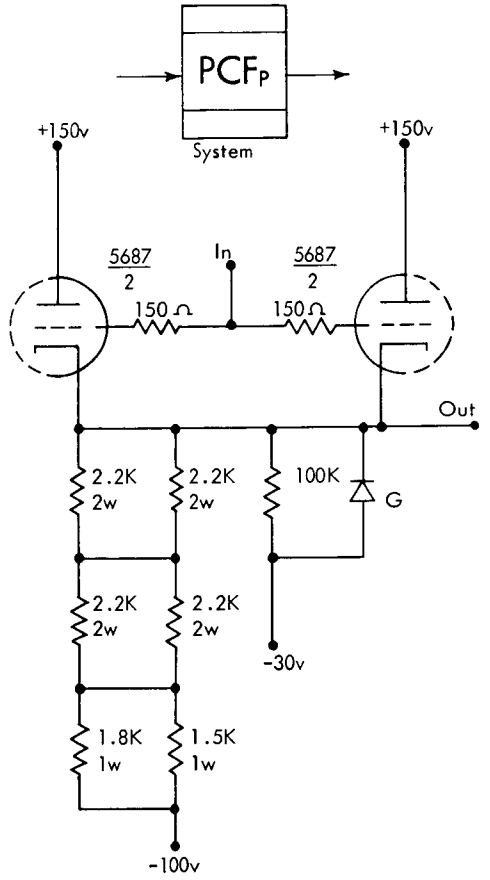


FIGURE B71. POWER CATHODE FOLLOWER (PCF_P)

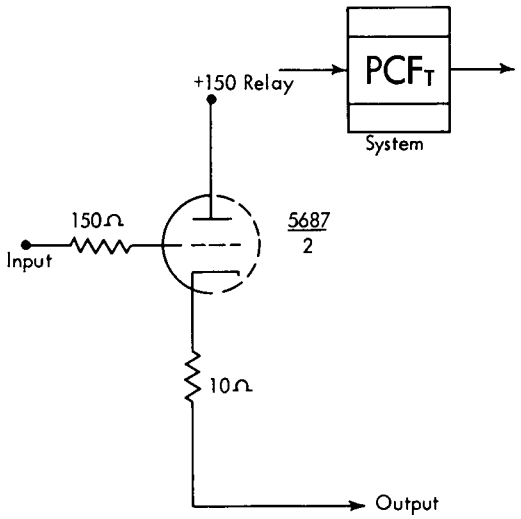


FIGURE B72. POWER CATHODE FOLLOWER (PCF_T)

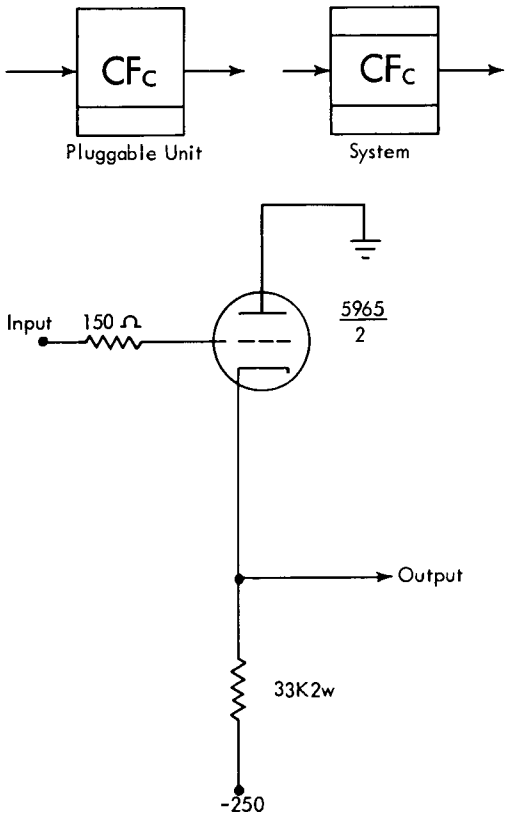


FIGURE B73. CATHODE FOLLOWER (CF_C)

2.05.21 Power Cathode Follower (PCF_O)

The PCF_O (Figure B70) powers the output of the master oscillator into the inverted sync generator.

2.05.22 Power Cathode Follower (PCF_P)

The special cathode follower PCF_P (Figure B71) powers the sync pulse before it enters the sync power amplifier. This cathode follower has an equivalent cathode resistance of 3K, 10 watts. The output of this cathode follower has a greater fall time than the input because of the large input capacitance present in the following stage. The tube can supply much charging current to this capacitance when the pulse is rising, but the cathode resistor cannot supply so much when the pulse is falling.

2.05.23 Power Cathode Follower (PCF_T)

The PCF_T (Figure B72), in conjunction with I_R's, switches current through the moving coil of the 726 tape unit.

The load for $2PCF_T$ is the moving coil and $2I_R$.

2.05.24 Power Cathode Follower OR (PCF_{OR})

This circuit is identical to the PCF except that one load resistor and clamp are used by more than one half tube.

2.05.25 Cathode Follower (CF_A)

This component was assigned to the 701 field tester only (section 2.01.11, Book B).

2.05.26 Cathode Follower (CF_C)

Cathode follower CF_C (Figure B73) is a special circuit found in the deflection circuits of the 740 CRT recorder. It functions similarly to the standard cathode follower, except that the voltage levels are more negative.

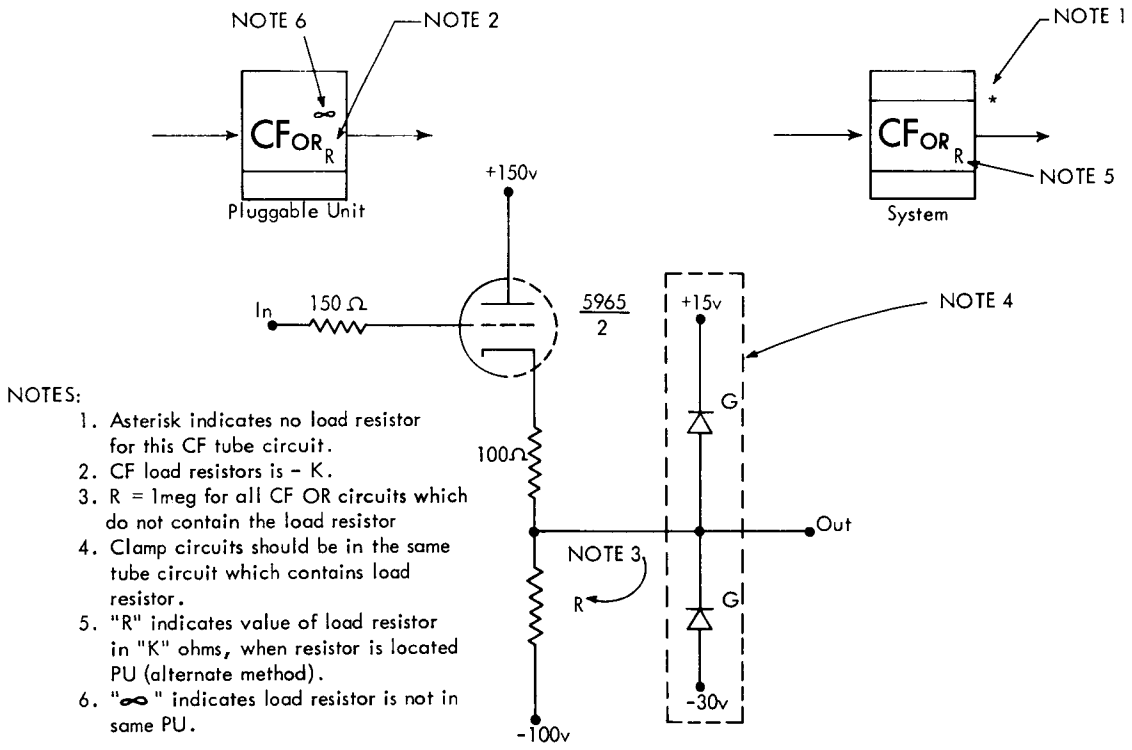


FIGURE B74. CATHODE FOLLOWER OR (CF_{OR})

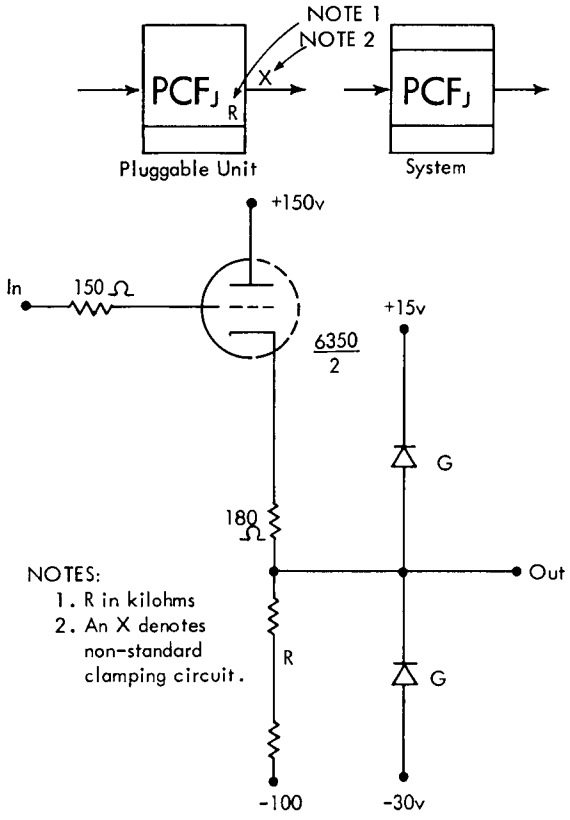


FIGURE B75. POWER CATHODE FOLLOWER (PCF_J)

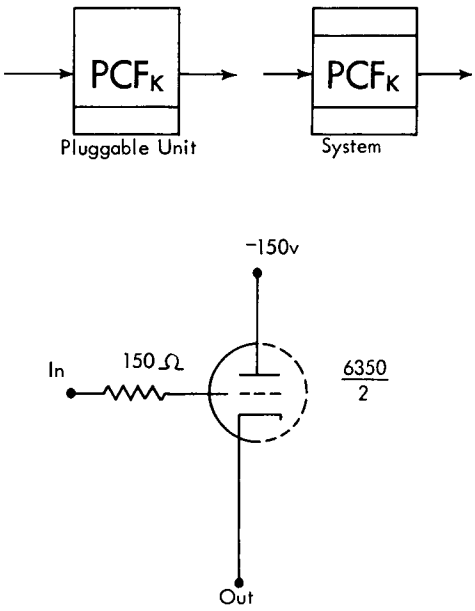


FIGURE B76. POWER CATHODE FOLLOWER (PCF_K)

2.05.27 Cathode Follower (CF_{OR})

Cathode follower CF_{OR} (Figure B74) is an OR circuit. That is, it has more than one input, and the output follows the highest input. This is done by using the same cathode load resistor for more than one half-tube triode cathode follower. Therfore, raising the voltage at any grid input causes an increase in current flow through the load resistor, giving a more positive input.

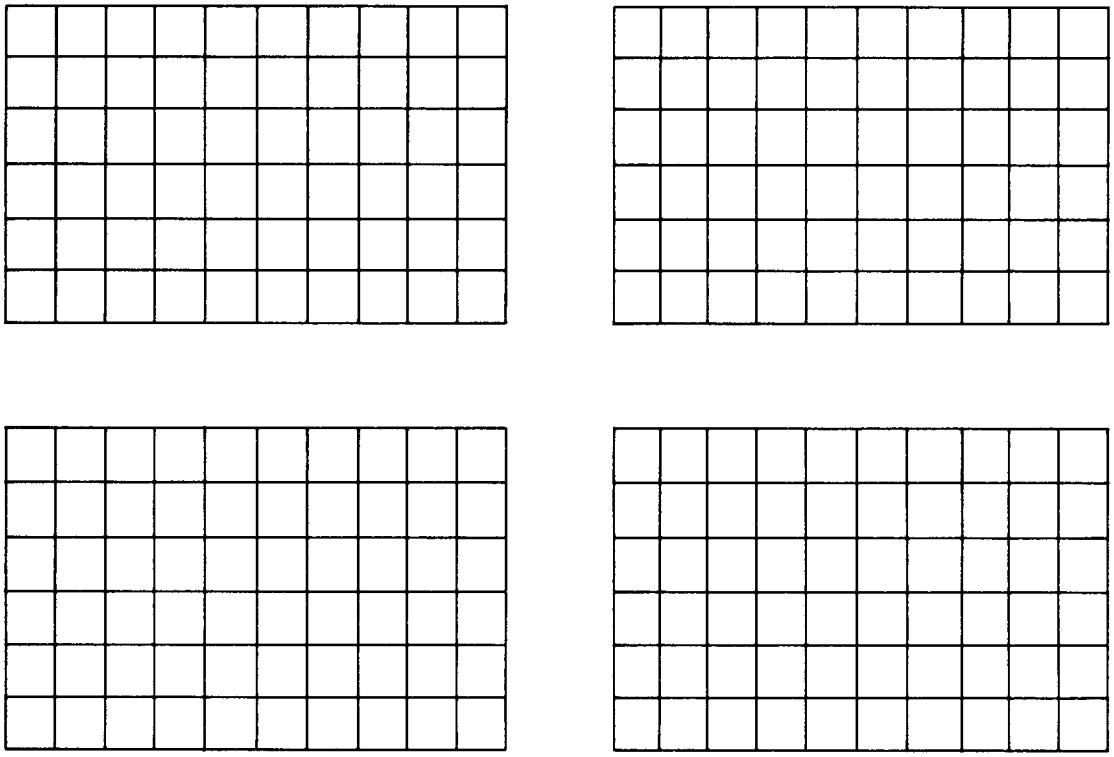
With this exception, CF_{OR} is identical to the standard cathode follower.

2.05.28 Power Cathode Follower (PCF_J)

The PCF_J (Figure B75) is the same as a standard PCF with the components changed to accommodate the 6350 which has an extended tube life.

2.05.29 Power Cathode Follower (PCF_K)

The PCF_K (Figure B76) powers the output of the storage buffer register to the storage buses. The load resistor is located in the CPU. A 6350 tube is used because of its long life.



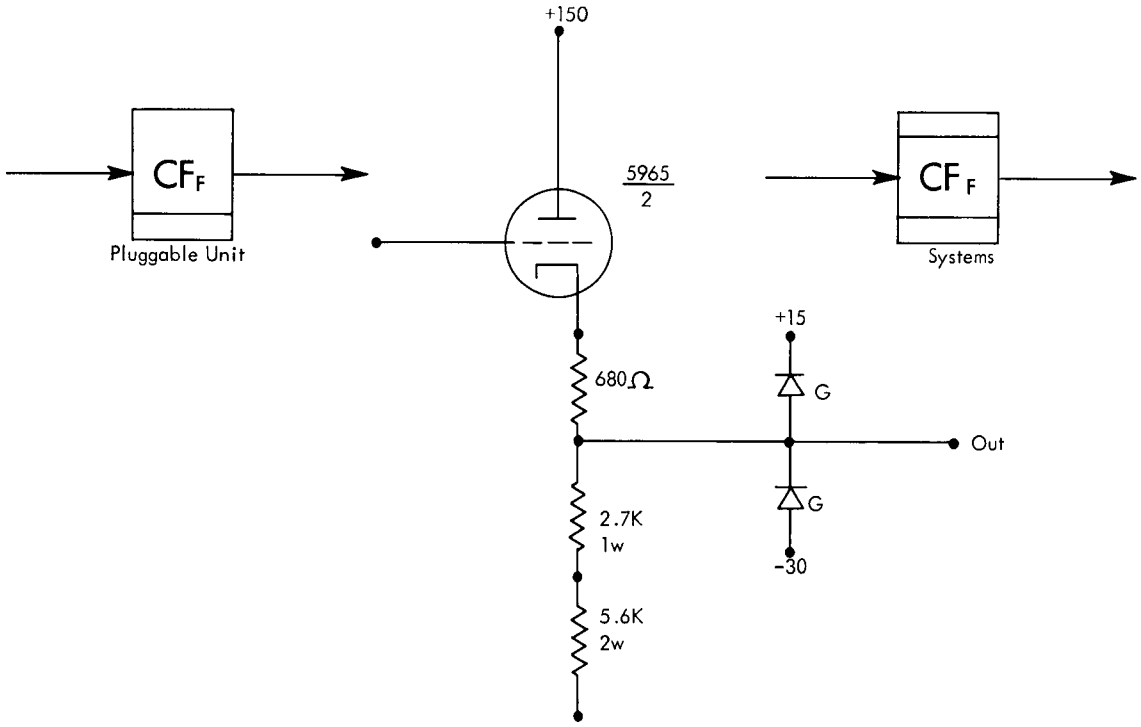


FIGURE B77. CATHODE FOLLOWER (CF_F)

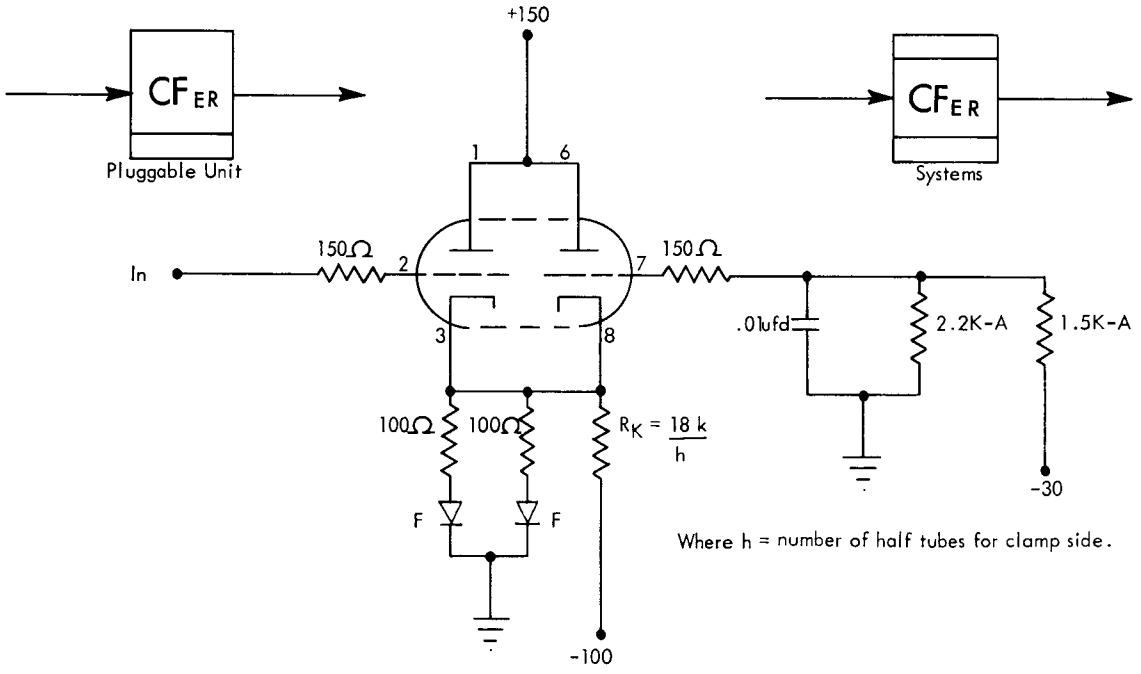


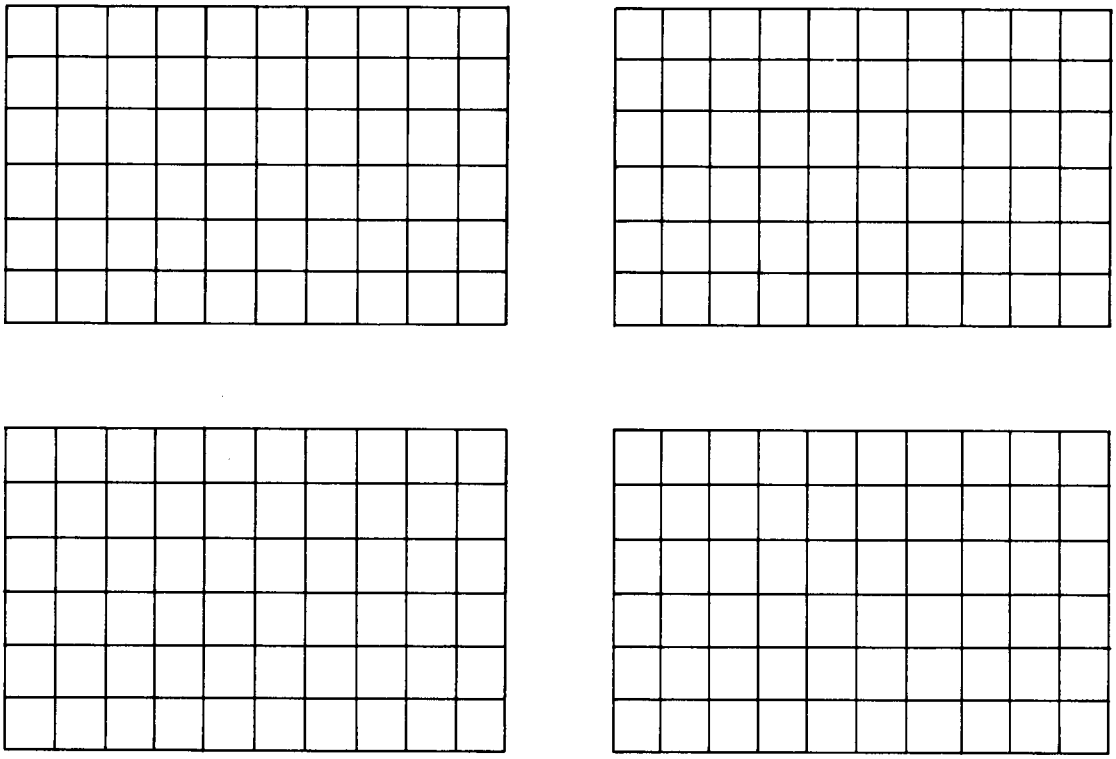
FIGURE B78. CATHODE FOLLOWER (CF_{ER})

2.05.30 Cathode Follower (CF_F)

This component was used to condition the shield grid of a thyratron in applications where this potential appears several milliseconds before firing. THY grid current was limited by the larger bias resistor which holds the up output to +3 volts. This component is being replaced by a CF; the increased grid current aids in firing the THY (Figure B77).

2.05.31 Cathode Follower (CF_{ER})

The CF_{ER} in its steady state provides a -12v clamp to the grid of a trigger, replacing the normal -12v resistor network. The input to the CF_{ER} is normally -30 volts. When the input rises to +10 volts, the output rises to ground and resets the trigger. The 10K resistor limits grid current. One half-tube is used on the clamp side for each 10 triggers and one half-tube on the reset side feeds 20 triggers. When half-tubes are paralleled, 100-ohm resistors are inserted in each paralleled cathode for current equalization (Figure B78).



2.06.00 DIODE CIRCUITS

2.06.01 Plus AND (Minus OR) Circuit

The operation of the AND (-OR) circuit is discussed in section 2.01.00, Book A.

Cascaded AND/OR circuits are discussed in section 2.04.00, Book A.

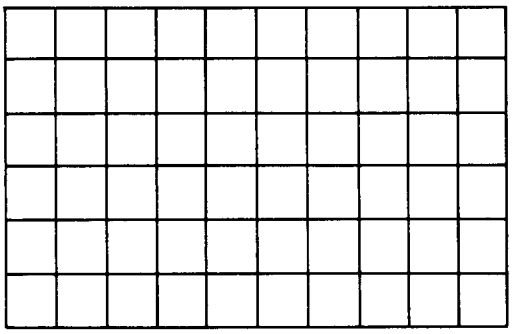
2.06.02 Plus OR (Minus AND) Circuit

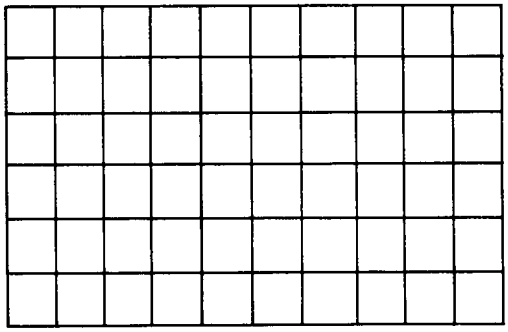
The operation of the OR (-AND) circuit is discussed in section 2.02.00, Book A.

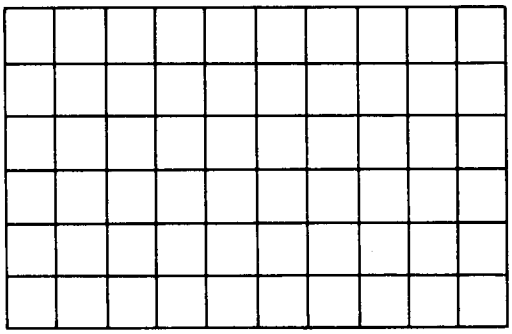
Cascaded AND/OR circuits are discussed in section 2.04.00, Book A.

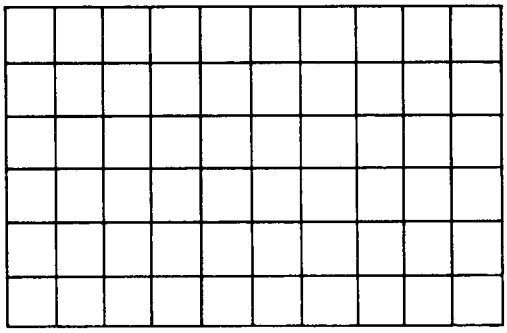
2.06.03 Tube Diode (DT)

This component was assigned to 701 electrostatic memory and is not used now.









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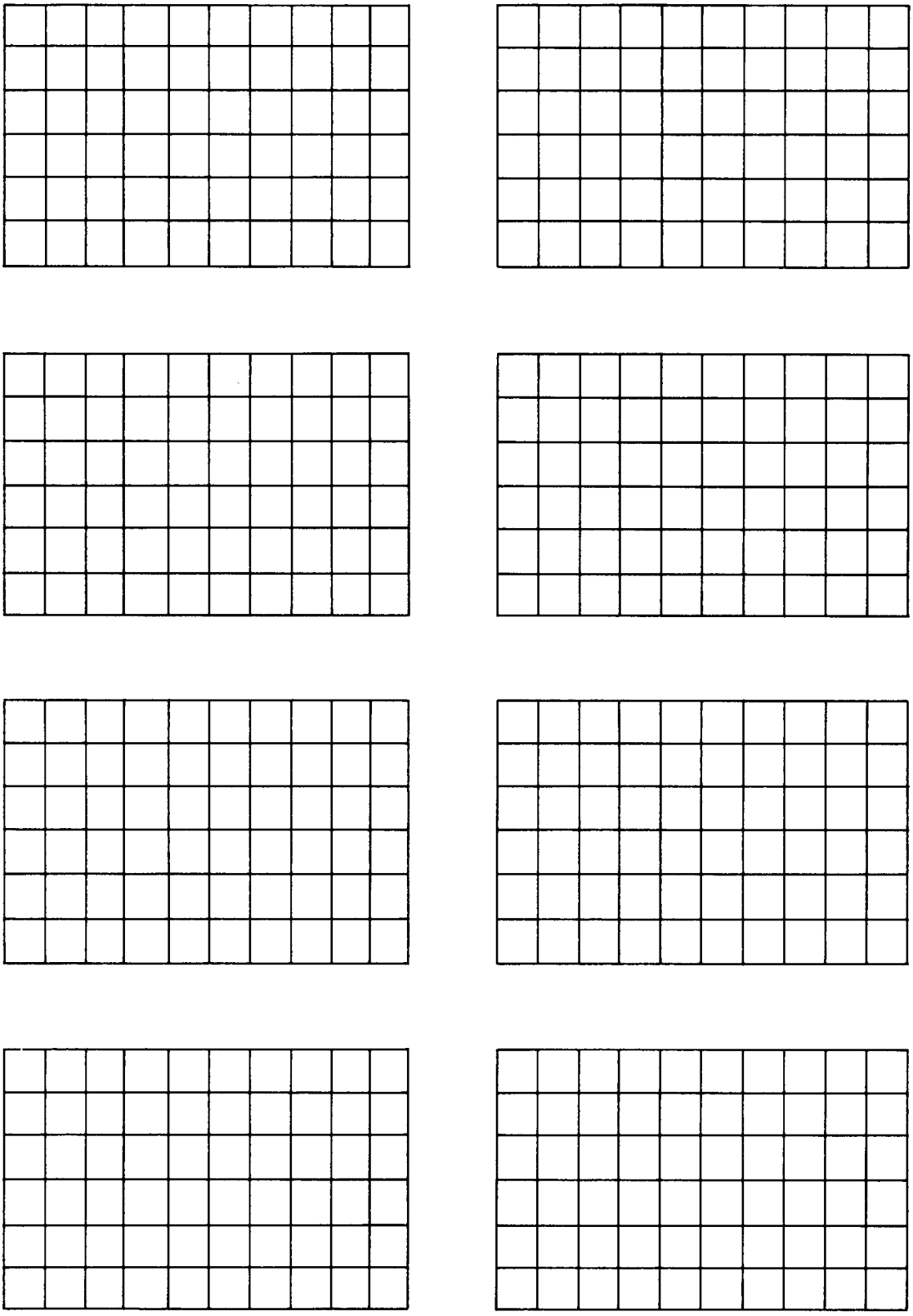
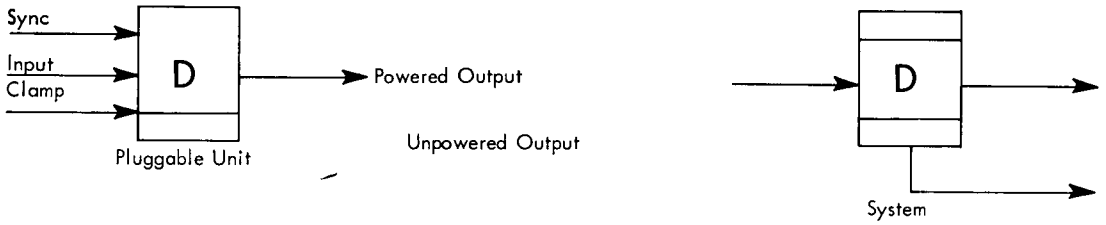




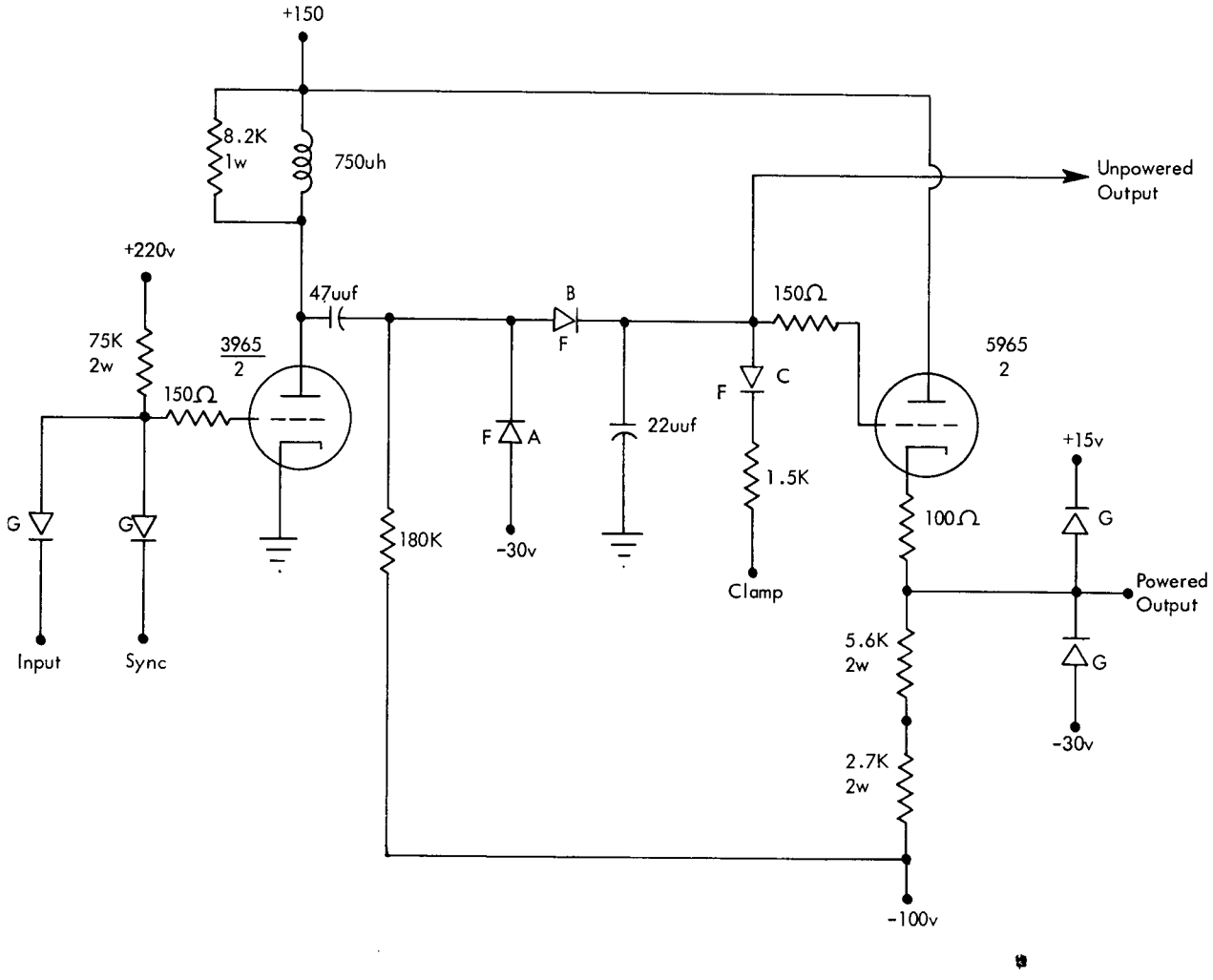


FIGURE B79. MICROSECOND DELAY UNIT

2.07.00 DELAY CIRCUITS

2.07.01 Microsecond Delay Unit (D)

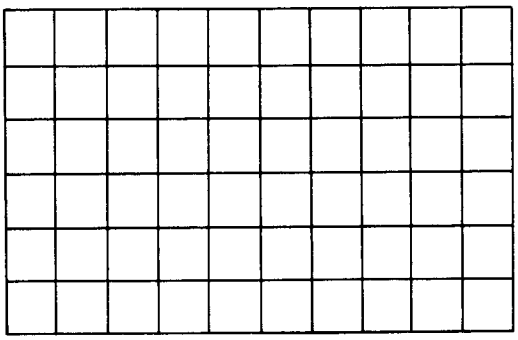
The microsecond delay unit, D (Figure B79), is a device for storing information. It has two operating states; one state represents a zero and the other a one. A useful property of this circuit is that new information may be applied to its input at the same time that old information is being taken from its output. This property makes the delay unit useful in shifting registers or other applications requiring simultaneous read-in or read-out.

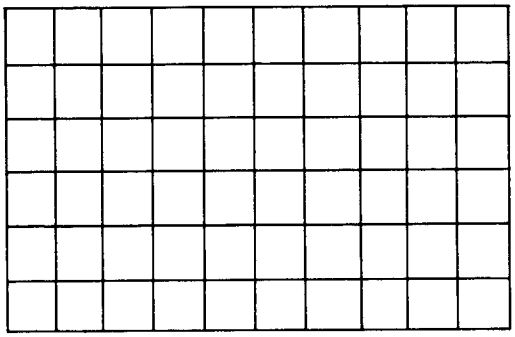
Operation of the delay unit requires the use of two special signals, sync and clamp. The sync pulse is a positive pulse having a duration of about 0.3 microsecond, and the clamp pulse is a negative pulse having a duration of 0.2 microsecond. Both pulses have a repetition rate of one megacycle and have nominal upper and lower voltage levels of +10 to -30 volts. These pulses are pictured in Figures B80a and B80b. The negative shift of the clamp pulse and the negative shift of the sync pulse are coincident in time. This relationship is important to the correct operation of the delay units. Another important feature is that the fall of the sync pulse is fast.

Circuit Description--Reading in a One

Input to the Delay Unit. The input circuit to a delay unit is identical to a standard 75K, two-way AND circuit. An information bit is fed to the delay unit through the input diode, and the sync pulses are fed through the sync diode. The information input line is shown on a logical diagram. A binary one is represented by 10 volts; and if a one is contained on the information input, it gates the sync pulse through the AND circuit to the grid of the input tube. Figures B80c and B80d show sample input and grid wave forms. The pulses on the grid of the input tube do not rise to +10 volts because the heavy grid current is being drawn by the tube.

Peaking Circuit. The input tube to the delay unit is part of a shunt-peaking circuit, similar in operation to the high-speed inverter. The peaking tube is normally cut off, but a positive pulse on the grid causes the plate voltage to fall to about +85 volts. The tube conducts heavily because no current-limiting resistors are present in either the grid or the plate circuits. When the sync pulse falls sharply, the tube is cut off and a large peaked positive pulse is produced at the plate. This pulse rises to about +205 volts and is shown in Figure B80e. The resistor in parallel with the coil serves to damp the peaked pulses and also serves as a bobbin for the coil. Therefore, whenever a delay unit is reading in a binary one, the sync pulse produces at the plate of the peaking tube a 65v negative pulse followed by a 55v positive pulse.





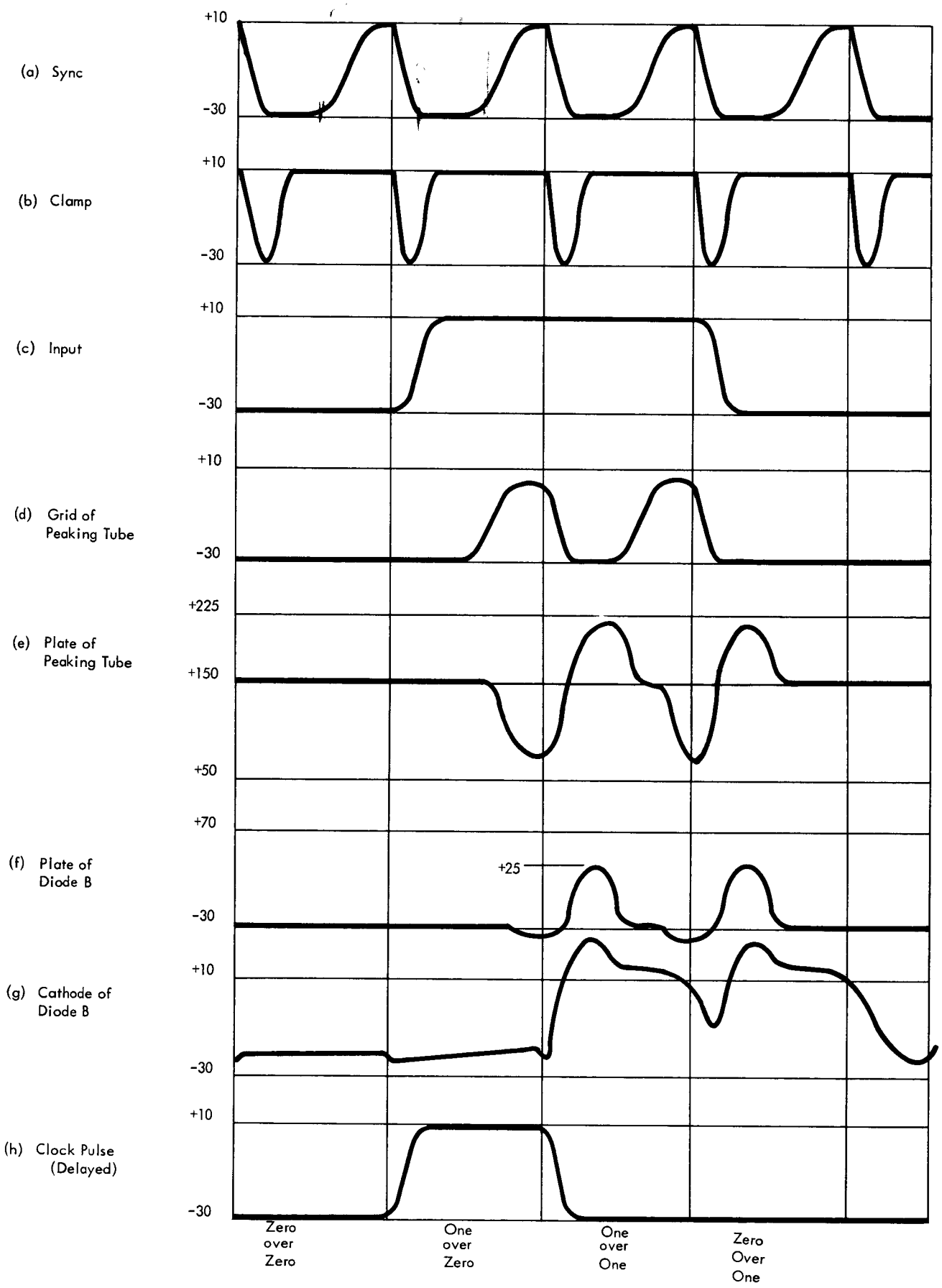


FIGURE B80. MICROSECOND-DELAY-UNIT WAVE FORMS

Timing of the Delay Unit

The microsecond delay unit does not delay a pulse in the sense that a delay line does; when given the proper input, the delay unit produces an artificial pulse timed accurately with the clock pulses of the machine. To understand timing, it is helpful to consider the time intervals of one microsecond each (shown in Figure B80) as being divided into tenths of microseconds, the beginning of each tenth being designated as 0.0 time, 0.1 time, and so on.

For correct operation, all an input pulse is required to do is to gate the sync pulse so that the last fall of the sync pulse can cut off the peaking tube to obtain the peaking action. To fulful these qualifications, the input pulse should be present both before and while the sync pulse falls; therefore, the input pulse may be poorly shaped or entirely absent during the first 0.6 of a microsecond and still be sufficient.

On the other hand, the delay unit produces a uniform output pulse of up to +10 volts by 0.2 time. If an input pulse should arrive at 0.8 time, the delay is then only 0.4 microsecond. The only time that a delay unit produces a delay of one microsecond is when it is fed a pulse that comes up at 0.2 time. Such a pulse may be from another or even from the same delay unit. The nominal delay of the unit is proportional to the period of the sync and clamp pulse.

The Delay Unit as a Storage Device

The circuits required to read an information bit into a delay unit and store it are shown in Figure B81. When information is to be read in, "read-in control" becomes positive, gating information through AND circuit A and OR circuit C to the unit. At the same time, it prevents (through "hold") any information from the delay unit itself from entering the input. When "read-in control" goes negative, "hold" goes positive, allowing the output of the delay unit to feed into itself through AND circuit B and OR circuit C. If the unit contains a 1, the sync pulse is gated in to produce another 1 that appears during the next microsecond to gate through the following sync pulse. This the the process of storing a bit. It is actually a process of substituting the output of the unit for the information input. The storing of a zero is merely the suppression of the sync pulses by the -25v output of the unit. The process of storage continues until "hold" is dropped to a negative voltage, at which time new information is read in. Note that, at the time new information is being read in, it has no effect on the information appearing at the output. This property makes the unit extremely valuable in shifting registers. "Read-in control" is a clock pulse that has been delayed by mixing and amplifying circuits; the timing of this line, therefore, is shown with respect to a sync pulse in Figure B80h.

Note here that a 1 could be read into a delay unit without dropping "hold," but a zero cannot be read in over a 1. Therefore, "hold" is dropped (for simplicity of control) whenever reading in occurs. This process amounts to simultaneous resetting and reading in.

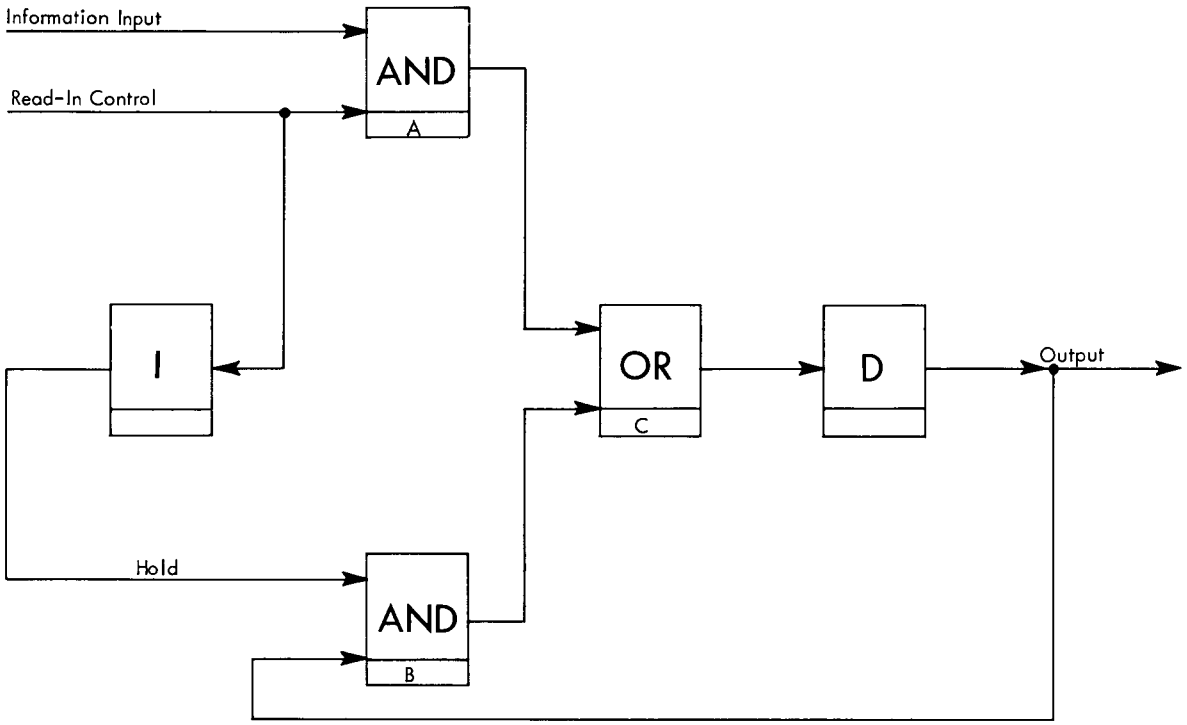


FIGURE B81. MICROSECOND DELAY UNIT AS A STORAGE DEVICE

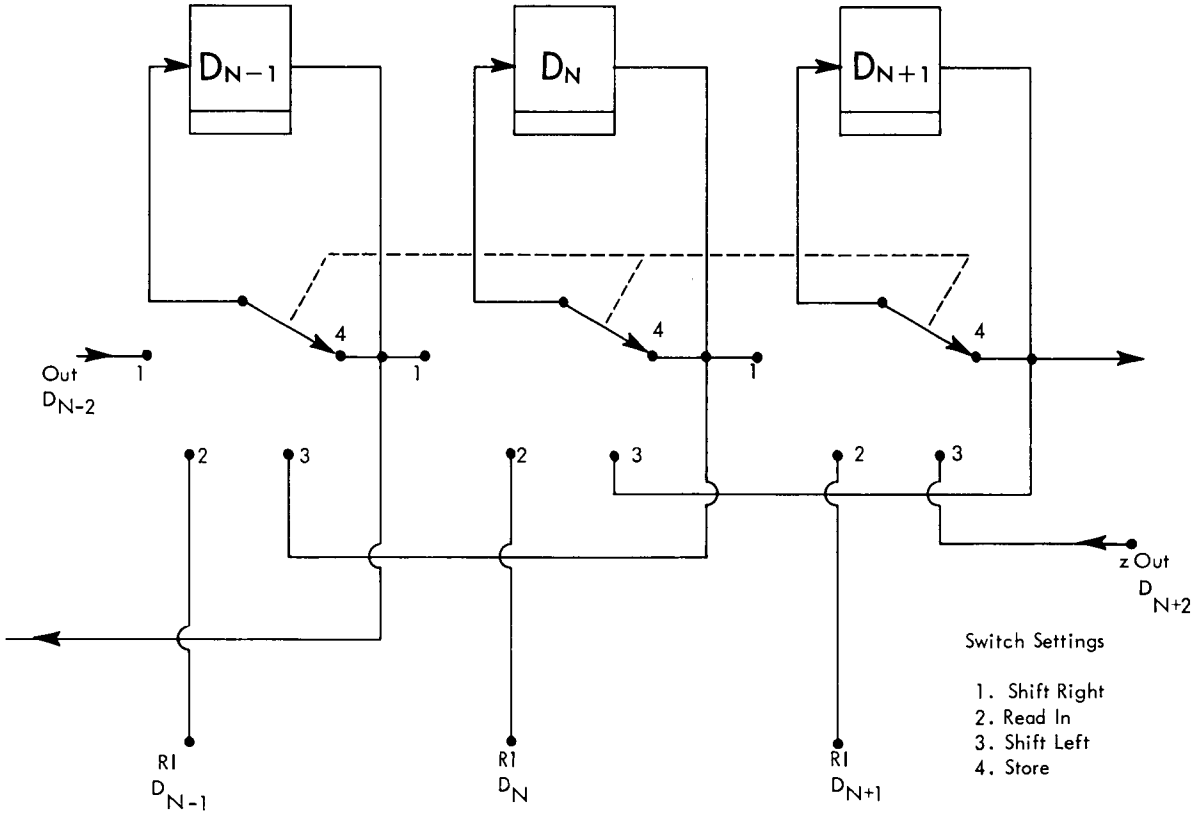


FIGURE B82. SHIFTING REGISTER

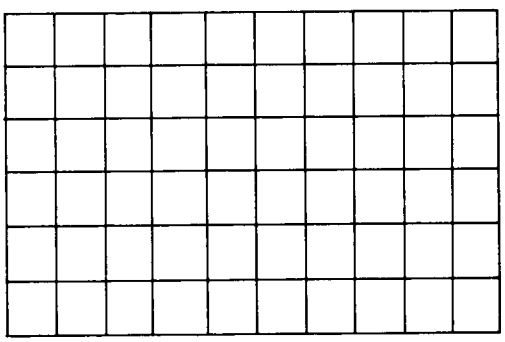
Charging the Storage Capacitor, the Clamp Pulse. The 22-uuf capacitor shown connected to the grid of the output tube in Figure B79 is called a storage capacitor; the voltage produced at this grid by the charge upon this capacitor determines the voltage output of the delay unit. In describing the action of this capacitor, the terms, charge or discharge, mean making the voltage upon the grid more positive or making it more negative, respectively. Two pulses have an effect upon the charge left on the capacitor; a positive pulse from the peaking circuit tends to charge the capacitor, and the clamp pulse tends to discharge it. The plate of diode B normally is at -30 volts; therefore, the 47-uuf capacitor and 180K resistor pass the positive pulse to the plate of diode B, but diode A clips off the negative pulse from the peaking circuit. The wave form at the plate of diode B is shown in Figure B80f. If the grid of the output tube is at -30 volts when the positive pulse arrives at the plate of diode B, this diode passes the pulse and allows it to charge the capacitor. Coincident with the beginning of the positive pulse, the clamp pulse arrives to discharge the capacitor. Because the positive pulse has greater amplitude and lasts longer than the clamp pulse, the capacitor becomes charged after the clamp pulse returns to +10 volts. If the capacitor were already charged to +10 volts, only the peak of the positive pulse would be conducted through diode B. Because the clamp pulse arrives before the peak of the positive pulse, the capacitor is discharged somewhat. This discharging before the arrival of the peak is shown as a negative 10v dip (called glitch) in the grid wave form in Figure B80g. This figure also shows the peaked effect from the positive pulse.

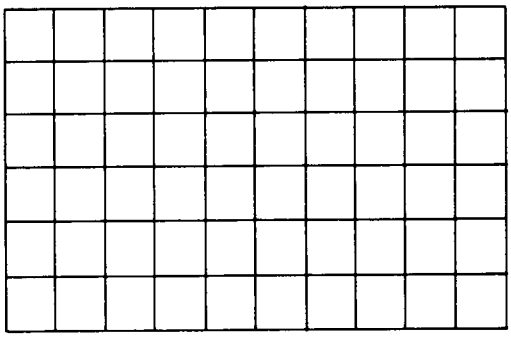
Output of Delay Unit

The output circuit of the delay unit is identical to a standard cathode follower. An alternate output is provided directly from the grid of the output tube; it is shown out of the bottom of the blocks (Figure B79). When this alternate output is used, it is powered externally to the delay unit by a cathode follower.

Circuit Description--Reading In a Zero

The process of reading a zero into the delay unit is much simpler than reading in a one. Since the information line is at -30 volts for a binary zero, no sync pulse can be gated through to produce any pulses at the plate of the peaking tube. Therefore, when the clamp pulse tends to discharge the storage capacitor, no opposing pulse will be present to interfere with the discharging action. The discharge path has so large a time constant that the clamp pulse can discharge the capacitor to only -25 volts before it disappears. The amplitude of the clamp pulse and the value of the 1.5K resistor were chosen to allow a quick discharge of the capacitor when the unit is reading in a zero over a one without giving excessively large glitches.





Action of Components

Each of the diodes in the delay unit has a special purpose. Diode A helps to set the voltage level at its cathode. Diode B allows passing of the positive pulse, but prevents the -100v supply from discharging the storage capacitor through the 180K resistor. Diode C prevents the clamp pulse from charging the capacitor while allowing the same pulse to discharge it.

If turns in the coil should become shorted or if the coil should become open, the unit is not able to read in 1's. In general, if a unit cannot read in the number, it cannot store it. The three diodes labeled A, B, and C in Figure B79 must be class F diodes, but the input diodes may be class G. The effects upon the operation of the delay unit when the diodes are faulty are varied and are listed briefly as follows:

Open Input Diode. The unit will always contain a 1.

Open Sync Diode. The unit will have difficulty in reading in a 1.

Shorted Sync or Input Diodes. Operation is likely to be erratic, and the input or sync wave forms are likely to be distorted. Distortion of the sync pulse may adversely affect operation of the other delay units in a column unit.

Open Diode A. The unit will not read in a 1 reliably.

Shorted Diode A. The unit will not read in a 1.

Open Diode B. The unit will not read in a 1; output falls to lowest clamp pulse level.

Shorted Diode B. Output will come up when a 1 is read in, but it will fall quickly and fail to hold the 1.

Low Back Resistance Diode B. Upper level of output will not hold constant, but will fall quickly toward -30 volts. Unit may operate intermittently.

Open Diode C. The unit will hold a 0 until a 1 is read in. The 1 then has a positive level and will not allow reading in of a 0.

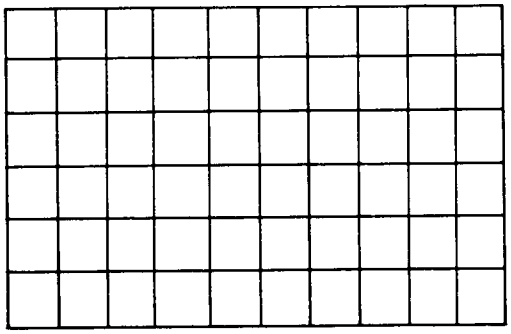
Shorted Diode C. Output follows clamp voltage.

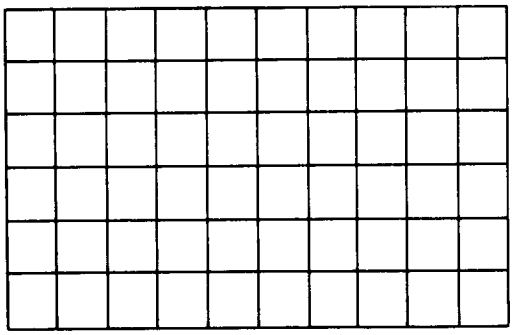
The above are general statements and may be modified under various marginal or boundary conditions.

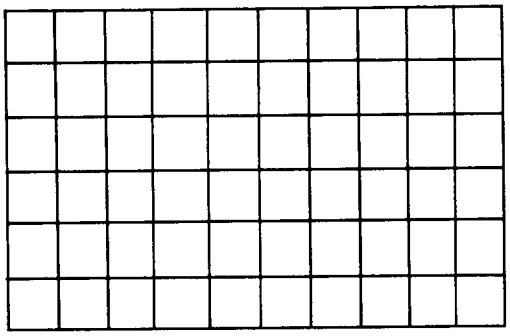
Summary of Characteristics

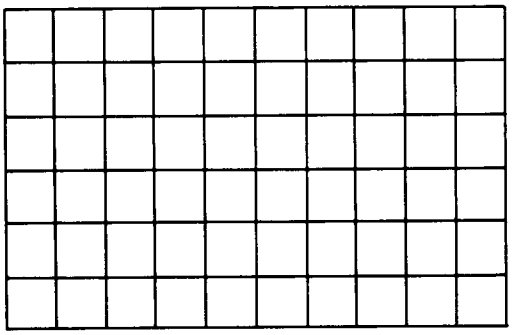
The delay unit has particular advantage over certain forms of storage because of its property of simultaneous read-in and read-out. This property allows higher speed and more economy for use in shifting registers.

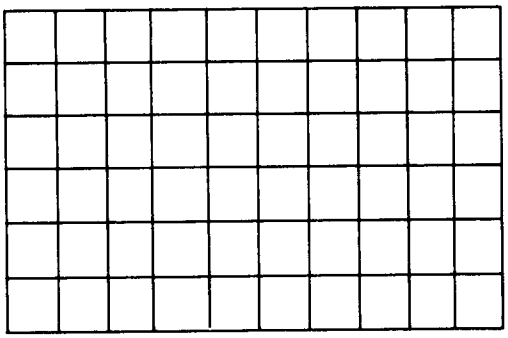
NOTES

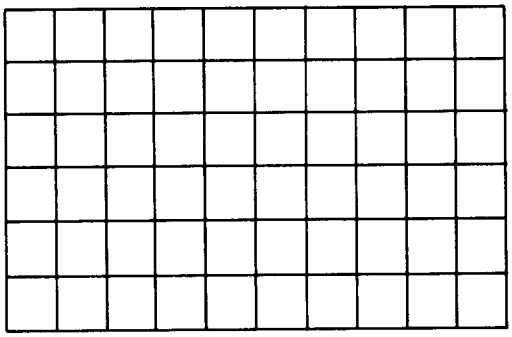


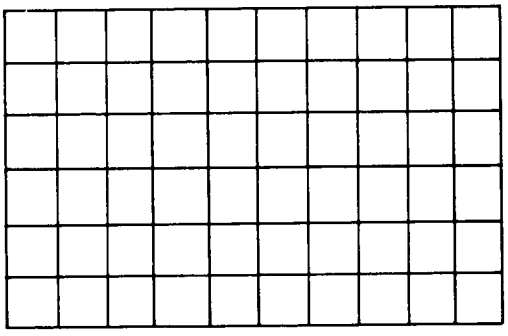


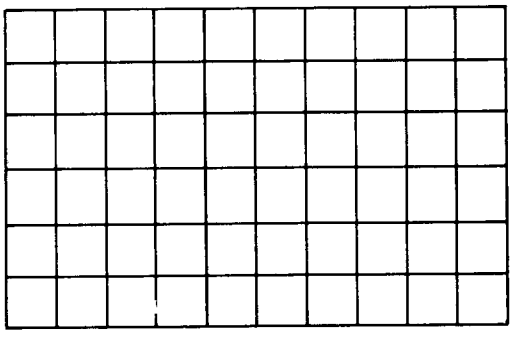












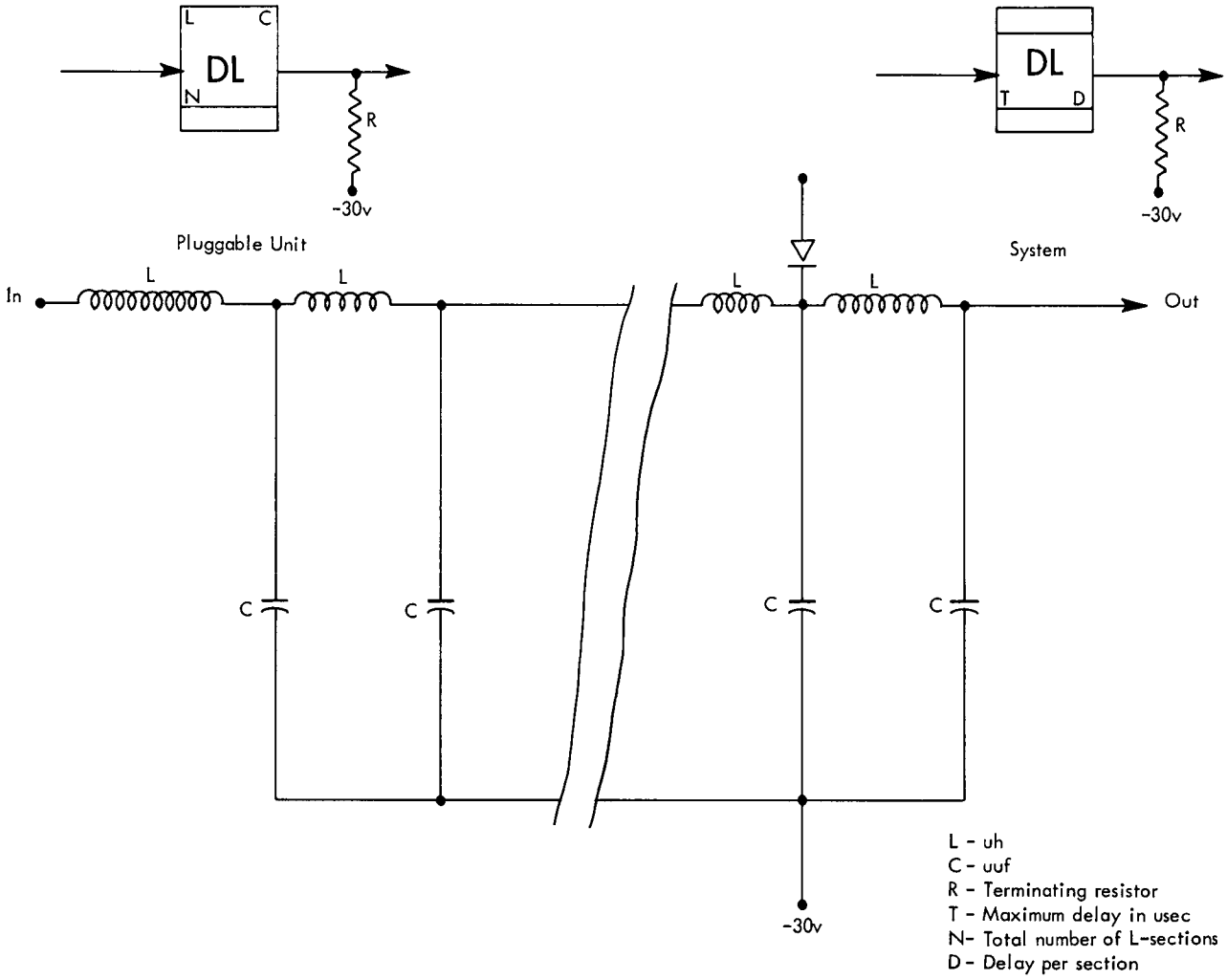


FIGURE B83. DELAY LINE (DL)

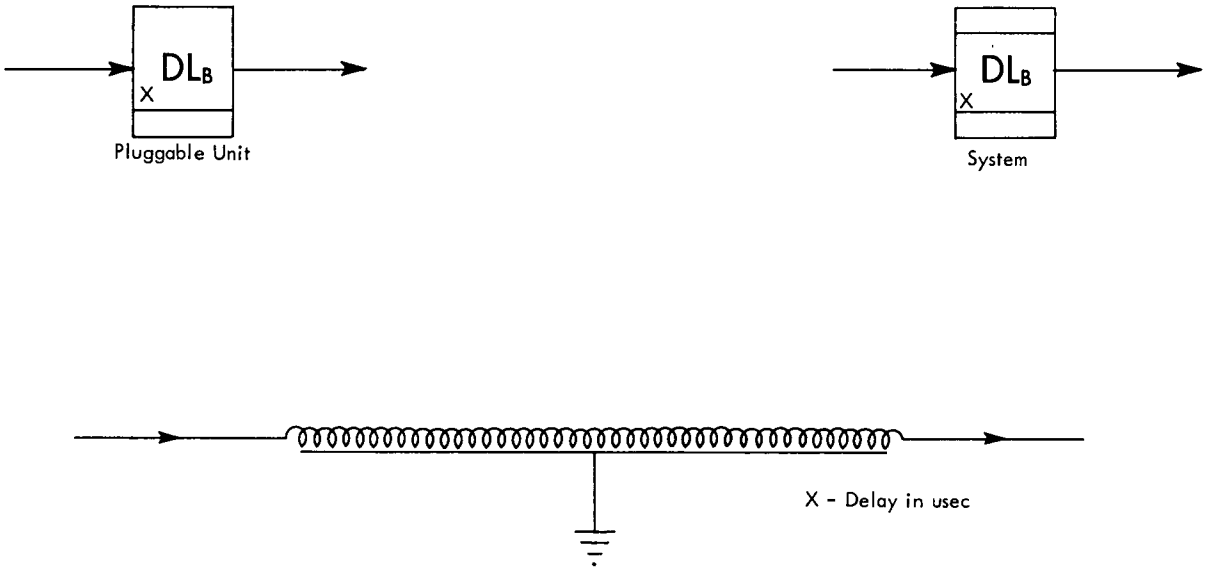


FIGURE B84. DELAY LINE (DL_B)

The delay unit is economical in that it uses only one full dual triode, and in addition gives a powered output. Its output pulses are accurately timed, and delays through a group of units are not accumulated. Poorly shaped pulses may be used as information inputs without causing poor operation. Also the unit is stable with variations in supply voltages. Two characteristics of the unit are not desirable--need for dynamic pulses for storage, and glitches in the output. But the advantages of such a circuit far outweigh these disadvantages, in the applications for which they are used in the calculator.

2.07.02 Delay Line (DL)

The delay line circuit, DL, (Figure B83) is used in the clock drive. This circuit is a lumped-constant type delay line. A lumped-constant delay line consists of a series of L-sections, each containing a series inductor and a shunt capacitor. If a voltage shift is applied to the input terminals of this type of line, current flows through the inductor of the first section to charge the capacitor of that section. As that capacitor becomes charged, its voltage then causes current to flow through the next inductor to charge its corresponding capacitor. This process continues successively from one section to the next along the line. Because it takes a finite time to charge the capacitor of each section through the impedance of its corresponding inductor, the pulse is delayed in its propagation along the line. The delay time in microseconds per section is the square root of the product LC, where L is the inductance per section in henries, and C is the capacitance per section in uuf. A lumped-constant delay line is found in the input to the clock.

The diagram blocks show the total number of sections and maximum delay of the circuit, but this circuit may be tapped at any section for obtaining a delay of less than the maximum. The tapped position is not indicated on the diagram blocks. Although a terminating resistor may be drawn from the output line on the block diagram, it is actually connected to the last section of the delay line.

2.07.03 Delay Line (DL_B)

DL_B is the symbol for a distributed-constant delay line (Figure B84). A distributed-constant delay line resembles coaxial transmission line, except that it is specially constructed so that its inductance and capacitance are relatively large per unit length. This is necessary so that the desired delay may be obtained in shorter lengths of line. This type of line differs from the lumped-constant type in that the line itself, instead of discrete components, forms the inductance and capacitance. Electrically it acts as a lumped-constant line with a large number of components of small value. That is, the capacitance and inductance are distributed continuously along the line. The delay per unit length in microseconds equals the square root of LC, where L is the inductance in henries per unit length, and C is the capacitance in uuf per unit length. Distributed-constant lines may be found in the drum-read-sample circuit, and in the pulse forming circuits for core storage.

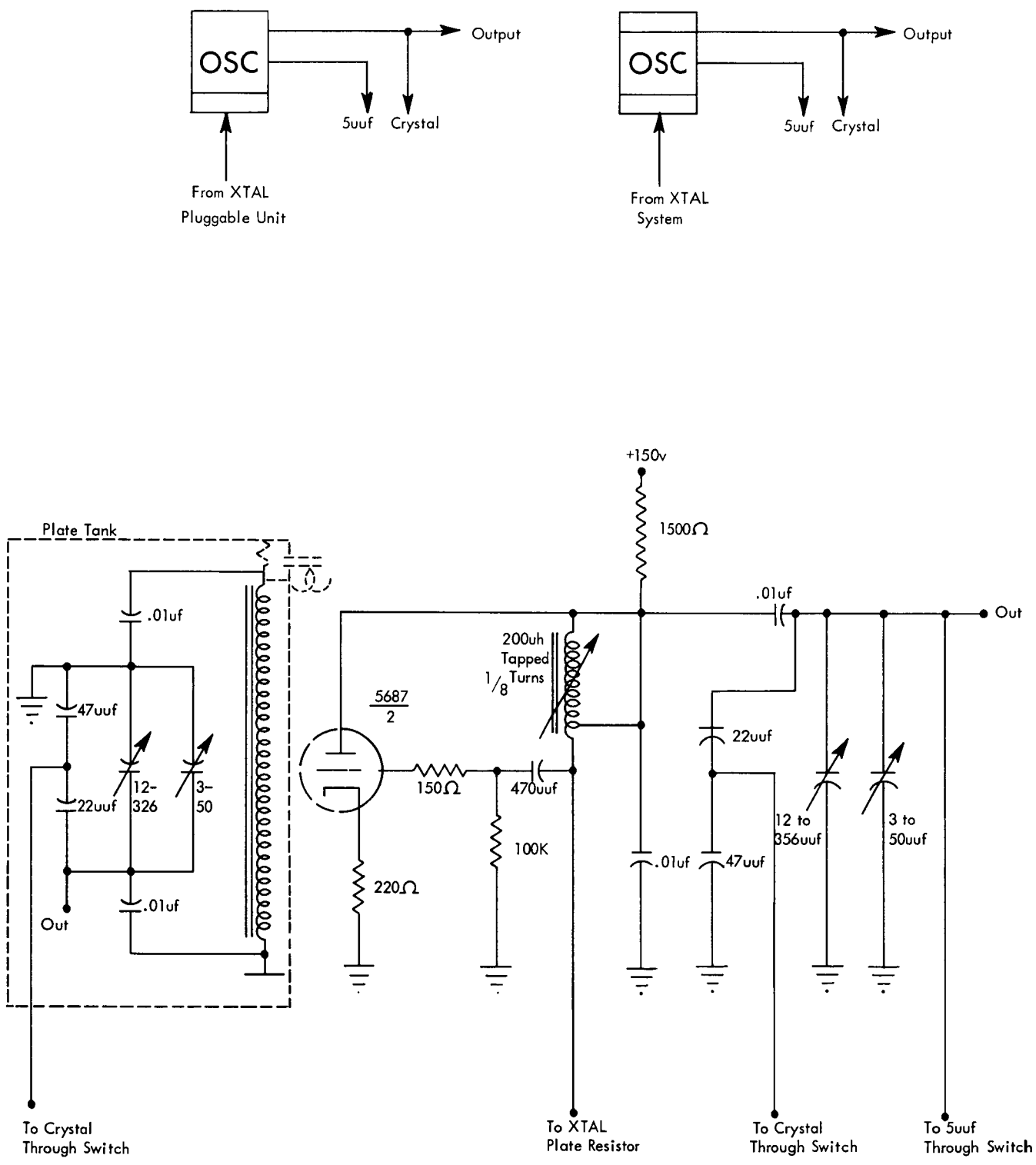


FIGURE B85. MASTER OSCILLATOR (OSC)

2.08.00 PULSE GENERATORS

2.08.01 Clamp Generator (CG)

The clamp generator, CG, (Figure B87) is similar to the sync generator both in operation and in circuit configuration. The chief difference is in the use of a shorter delay line to obtain the narrow pulse required here. RC coupling is used on the input for the same reason. Refer to Figure B80 for wave forms.

2.08.02 Master Oscillator (OSC)

The master oscillator circuit, OSC (Figure B85), is the basic timer for the entire system. It produces a one-megacycle, slightly distorted, sine wave.

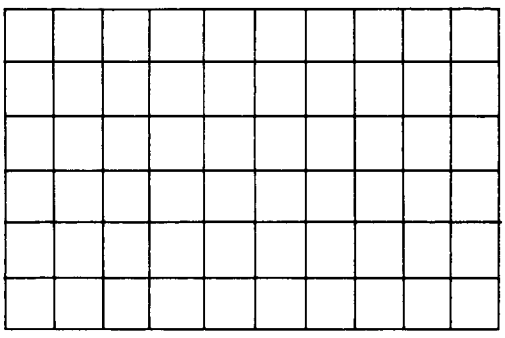
The OSC is a complete, independent, tuned-plate oscillator, free to oscillate without the crystal control discussed below. The tuned-plate circuit consists of the upper portion of the 200-uh plate coil, paralleled by the network of capacitors. The plate tank is illustrated in the inset of Figure B85. Voltage across the tank circuit is fed through auto-transformer action to the lower portion of the 200-uh coil. This lower portion feeds the grid circuit of the tube 180^{o} out of phase from the plate voltage. This feedback sustains oscillations in the tank.

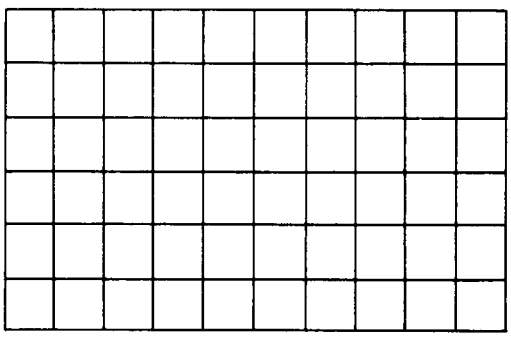
The variable capacitor labeled 12 to 356 uuf is in the form of a large vernier adjustment knob on the front of the oscillator box. It is intended to vary the frequency over a wide range when the crystal is not in the circuit. The dial on the front is notched so that the capacitor can be locked in approximately mid-position when using the crystal control.

The variable capacitor labeled 3 to 50 uuf is a screwdriver adjustment on the front of the oscillator box. It is intended to be adjusted to stabilize the oscillator when under crystal control.

2.08.03 Multivibrator (MV)

MV is the symbol of the multivibrator used for writing the timing and index tracks on the drum (Figure B86). This circuit includes a symmetrical, free-running multivibrator, a cathode follower, and a peaker circuit for shaping the output of the multivibrator. A switch is provided on a drum panel to turn on the circuit only when required, and a neon on this panel indicates the MV is on.





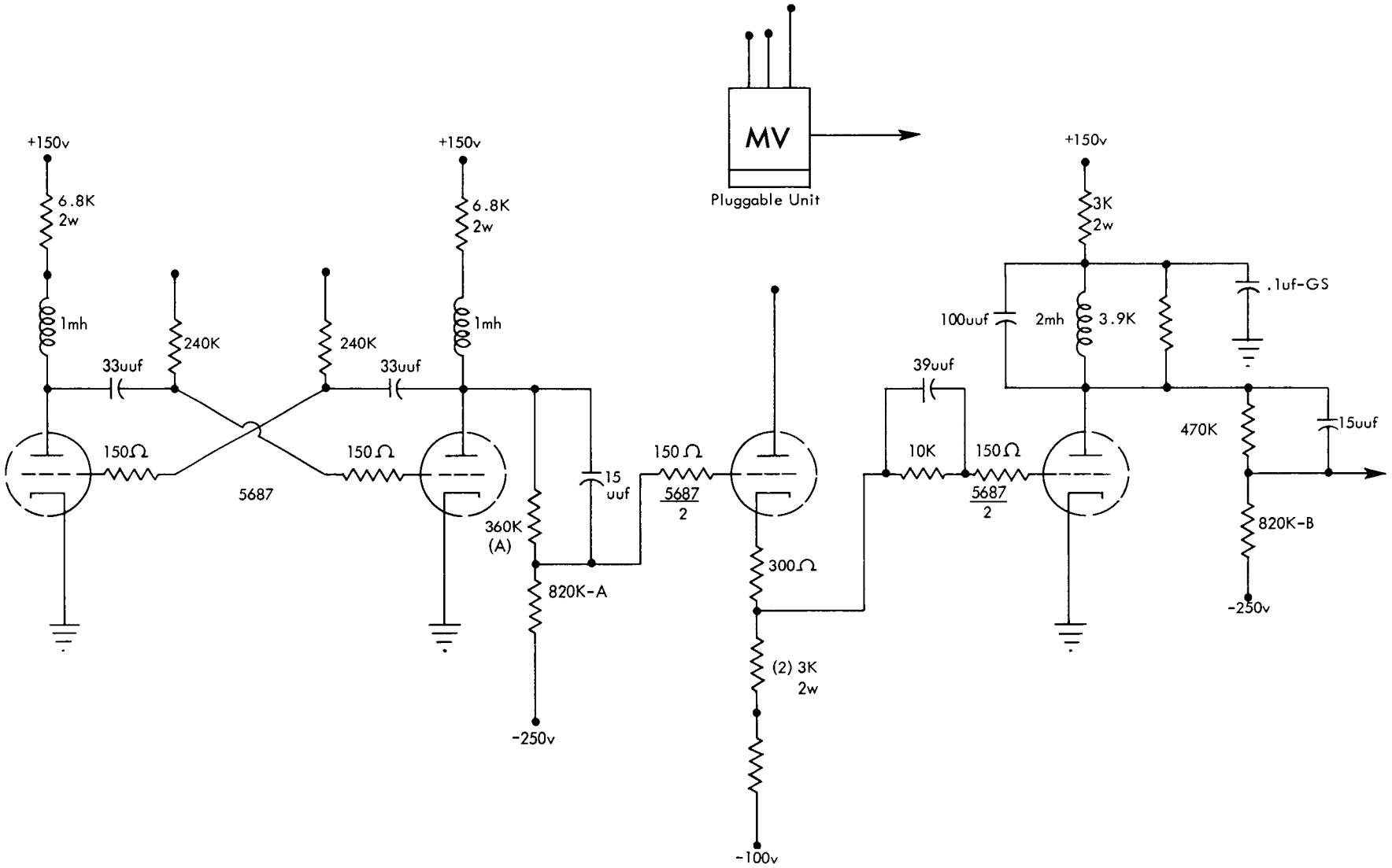


FIGURE B86. MULTIVIBRATOR (MV)

Multivibrator Stage

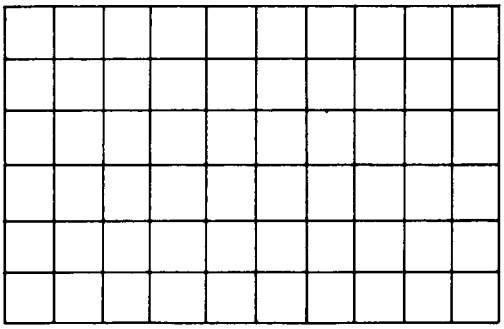
The operation of the plate-to-grid-coupled, free-running multivibrator is discussed first. This circuit resembles a basic trigger circuit, except that there is no resistance coupling from one plate to the opposite grid. The connections to the 240K resistors are through 250K potentiometers to +150 volts when the circuit is on and to -100 volts when the circuit is off. The series resistance from the grid to +150 volts is the timing resistance. When the circuit is first turned on, unbalance in the components causes one tube to conduct more than the other. The fall of its plate causes the opposite grid to fall and start to cut off the other tube. The plate of the other tube, in rising, causes the first tube to draw more current. This triggering action continues until the first tube is conducting heavily, and the other is fully cut off. Because (1) there is no resistance coupling to the down-grid from the up-plate, but (2) there is resistance coupling to the +150v supply through the timing resistance, the down-grid rises exponentially as the coupling capacitor is discharged through the timing resistor and the conducting tube. When this grid reaches such a value that the off-tube begins to conduct, the circuit flips to the opposite conditions because of the regenerative action mentioned above. Because this circuit is symmetrical, this action repeats continually at a rate determined by the magnitude of the negative shift on the grids and the value of timing resistance and capacitance. The potentiometers in the timing circuit of this multivibrator allows a frequency variation of about 80 to 120 kilocycles. They are ganged to keep the circuit symmetrical.

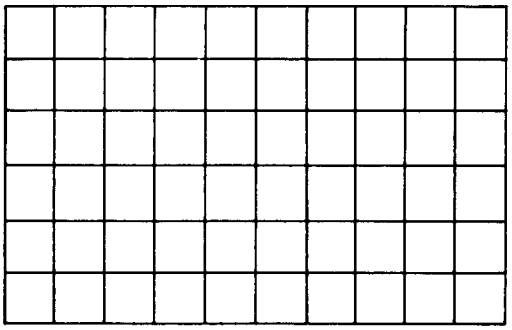
Cathode Follower Stage

The output of the multivibrator portion is fed into a standard power cathode follower without clamp doides. The plate return of this cathode follower is returned to the same point as the potentiometers, so that when the circuit is off, the output of the cathode follower is -100 volts. This is done so that the following peaker portion does not remain conducting during the relatively long periods when it is not in operation.

Output Stage

The last stage is a peaker circuit designed to give an output pulse about 1.5 microseconds wide. See section 2.15.00, Book A, for general peaker circuit operation. The output of the MV comes up to +10 volts. Since the peaker puts out a pulse more positive than +150 volts, and the output divider of the peaker is calculated to give out a pulse that comes to +10 volts, the DC level of the divider output is about +5 volts when the MV is off. The output of the cathode follower which follows this circuit is connected to +15 volts when the MV switch is off. Since its grid then is only +5 volts, no damage results to the tube.





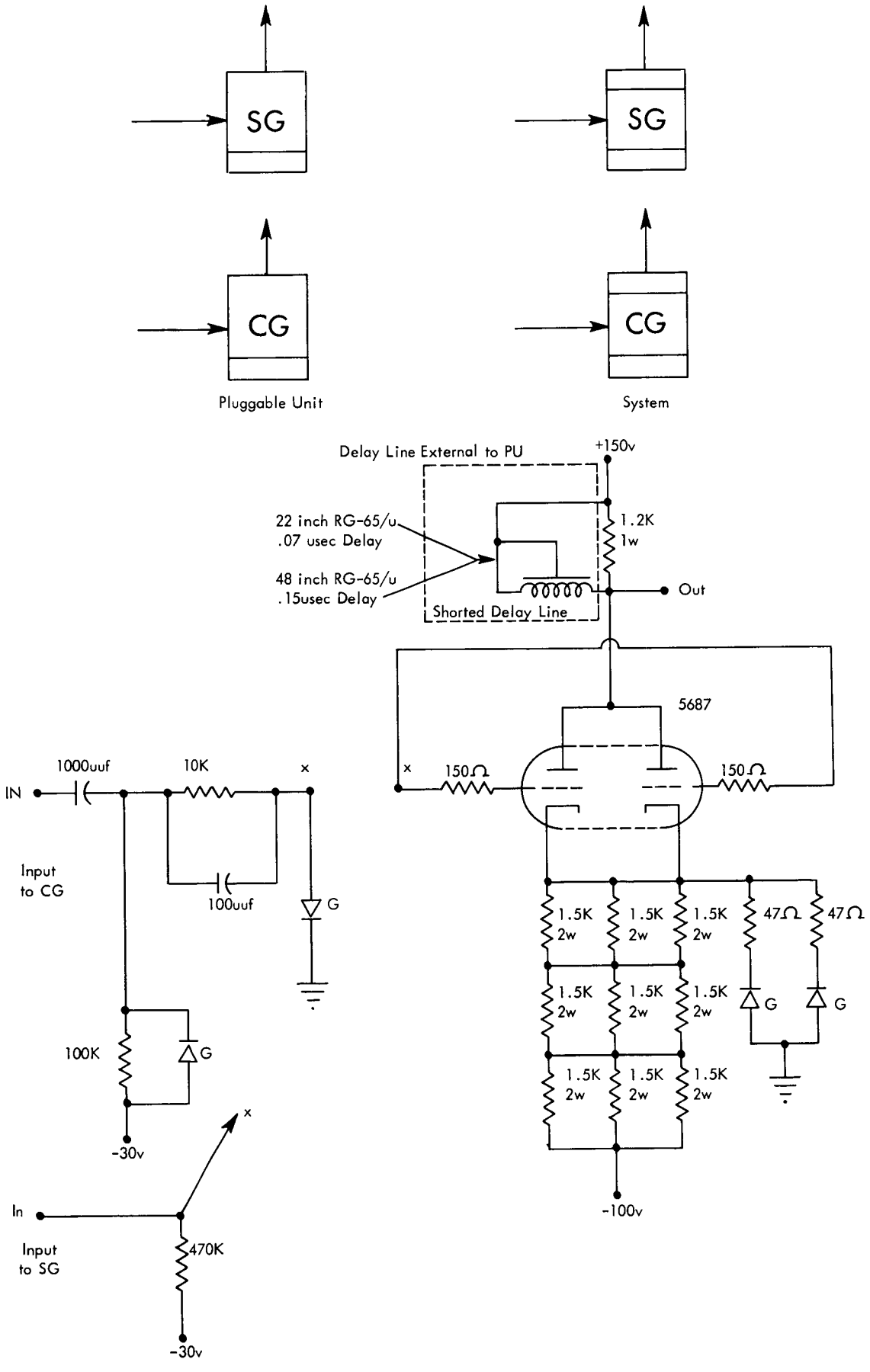


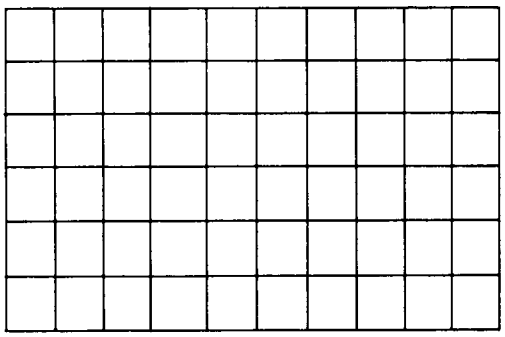
FIGURE B87. CLAMP AND SYNC GENERATORS (CG, SG)

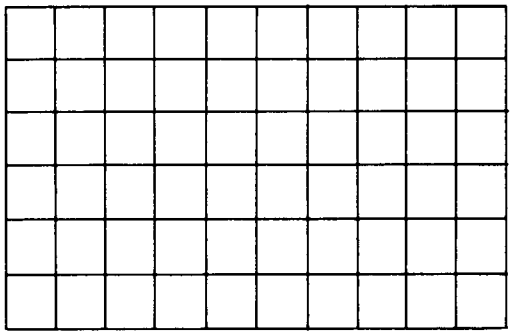
2.08.04 Sync Generator (SG)

The sync generator circuit (Figure B87) uses a shorted delay line for forming pulses of accurately determined widths. This line resembles a distributed-constant line (Figure B84) except that its delay is small. Its output terminals are shorted together. If a negative shift is applied to the input terminals, a negative wave front propagates down the line, but when it reaches the shorted end, the voltage shift cannot appear across a short circuit. To keep the voltage across the shorted end zero, the capacitance at that end must be discharged as fast as it is charged. This process originates a positive shift which propagates from the shorted end to the input end of the line, discharging the line capacitance as it progresses. When the reflected shift of opposite polarity from the initial shift reaches the input terminals, the capacitance is all discharged, and the voltage across the input terminals is the same as it was initially. But assume that the initial voltage drop across the input terminals is the result of current flowing through a resistor in parallel with the input terminals and assume that this current is still flowing; notice that after the reflected pulse reaches the input terminals, the current now flows through the series inductance of the line, through the short circuit at the shorted end, and back to an input terminal. Except for series resistance of the inductors and return line (not the characteristic resistance) the line appears as a short circuit across the input terminals after the reflected pulse has returned. The duration of the negative pulse at the input terminal is twice the delay of the line.

Assume that the current flow through the line is now stopped by some external source; a positive shift is produced at the input terminal. This shift results because the current ceases to flow through the inpedance (inductance and series resistance) of the line. The positive shift travels down the line, is reflected at the shorted end, and appears at the input end as a negative shift, thus ending a positive pulse of width equal to twice the delay of the line. At this time, the voltage at the input terminals should again be as it was before any pulses were applied, and the current through the line should be zero.

The delay line used in the sync generator is 48 inches long and has a delay of 0.042 microseconds per foot, giving a delay of 0.17 microseconds. The width of either the positive or the negative pulses at the plate is twice this delay or 0.34 microseconds, nominally. Because the sum of these two pulse widths is not one microsecond there is some time when the plate of the tube is approximately +150 volts, its quiescent level. Therefore, the output of this circuit is a series of alternate positive and negative pulses. It is the positive pulse of accurately determined width that eventually becomes the sync pulse, after it is shaped by the sync clipper (Figure B91). Refer to Figure B80 for wave forms.





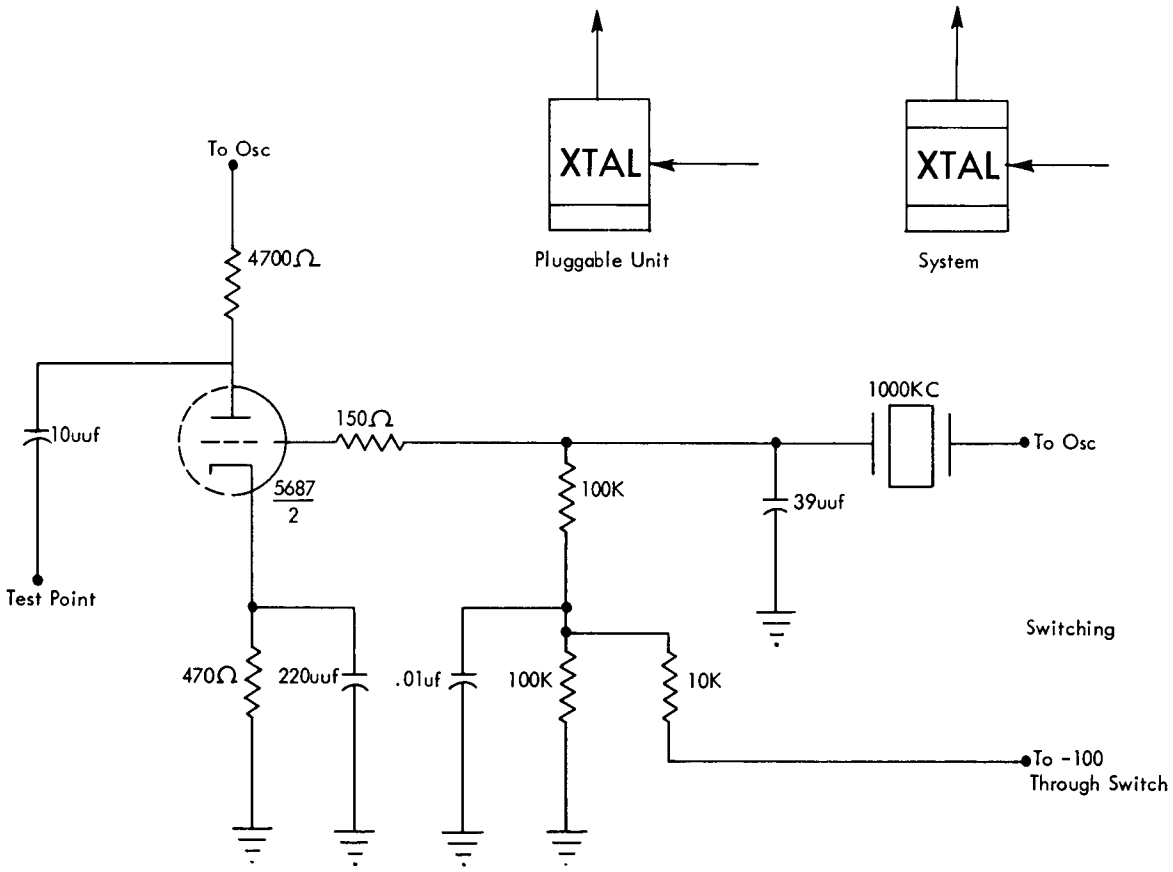


FIGURE B88. CRYSTAL (XTAL)

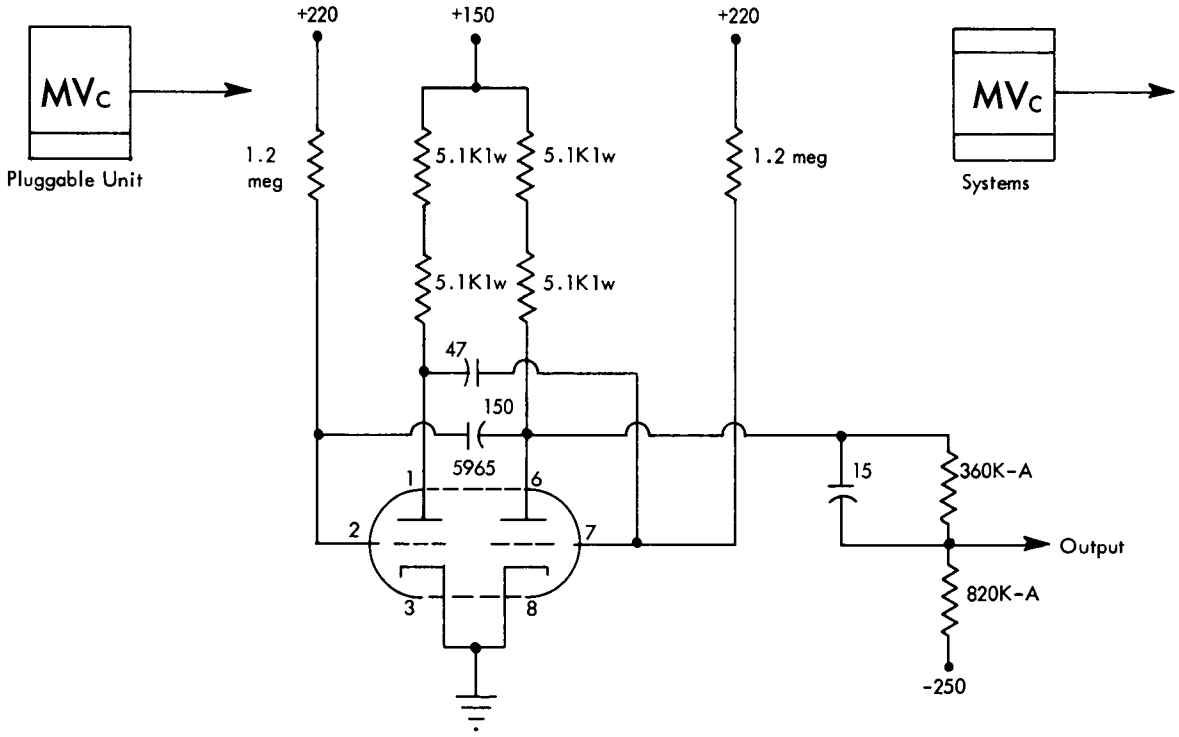


FIGURE B89. MULTIVIBRATOR (MV_C)

2.08.05 Crystal (XTAL)

The one-megacycle crystal, XTAL (Figure B88) is provided as a frequency standard for the machine. That is, it causes the master oscillator to operate at an exact and constant frequency.

When the crystal is switched in, energy is supplied to the crystal from the capacitor divider in the tank circuit. This causes the crystal to oscillate at its own mechanical resonant frequency. These oscillations are then sustained by a slight amount of energy from the tank circuit. The output of the crystal is applied to the other half of the oscillator tube which amplifies the signal, phase-shifts it 180^{o}, and applies it back to the grid of the oscillator tube.

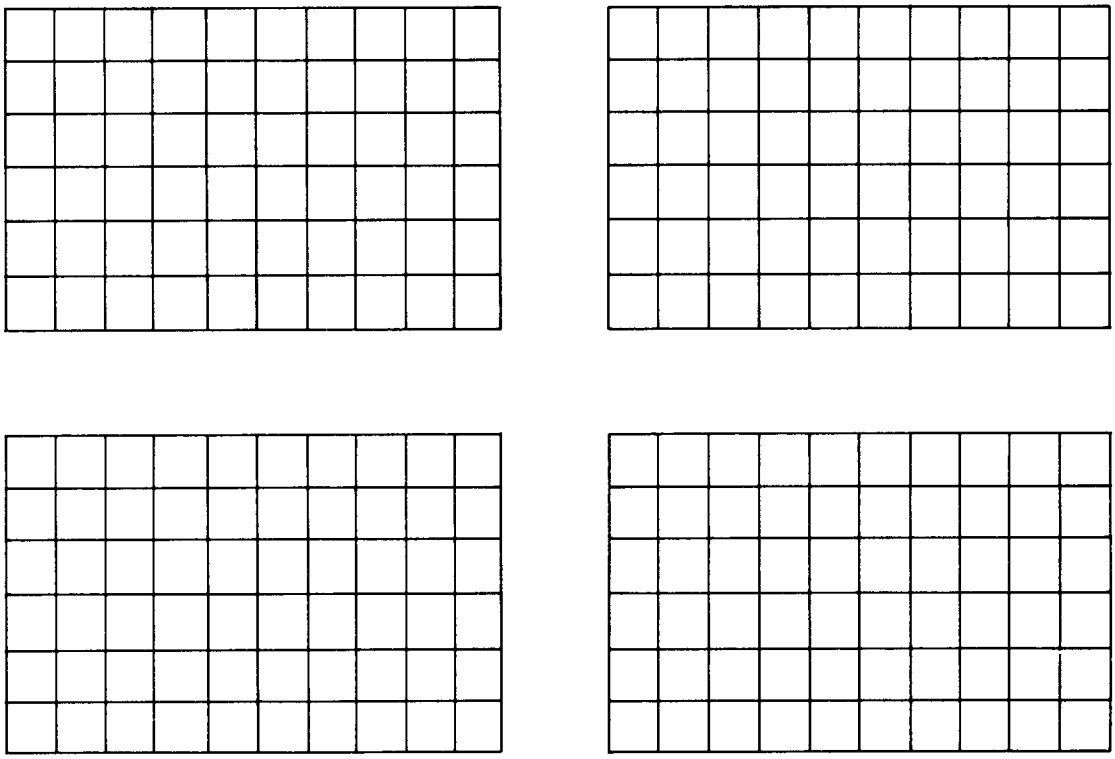
Therefore, as long as the oscillator tank is reasonably close to the crystal frequency, the crystal controls the oscillator. The 3 to 50 uuf capacitor in the oscillator is adjusted to the center of the range of crystal control.

A discussion of a crystal controlled oscillator is presented in section 2.13.00, Book A.

2.08.06 Unassigned

2.08.07 Multivibrator (MV_C)

The multivibrator, MV_C (Figure B89), is a special purpose circuit used in the CRT display unit. It is used to control the unblanking of the CRT when in a testing operation. Note from the RC coupling values that the output is about three to one. That is, the output is up three times as long as it is down.



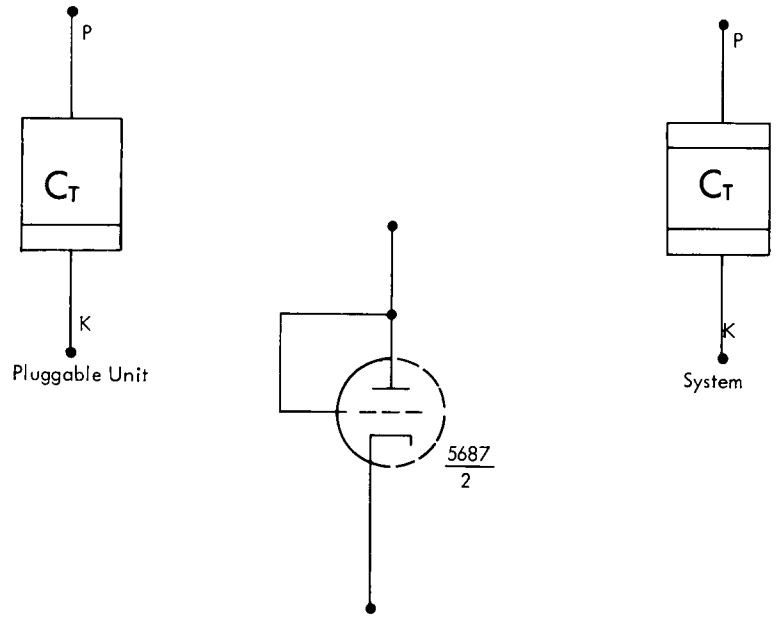


FIGURE B90. CLIPPER (C_T)

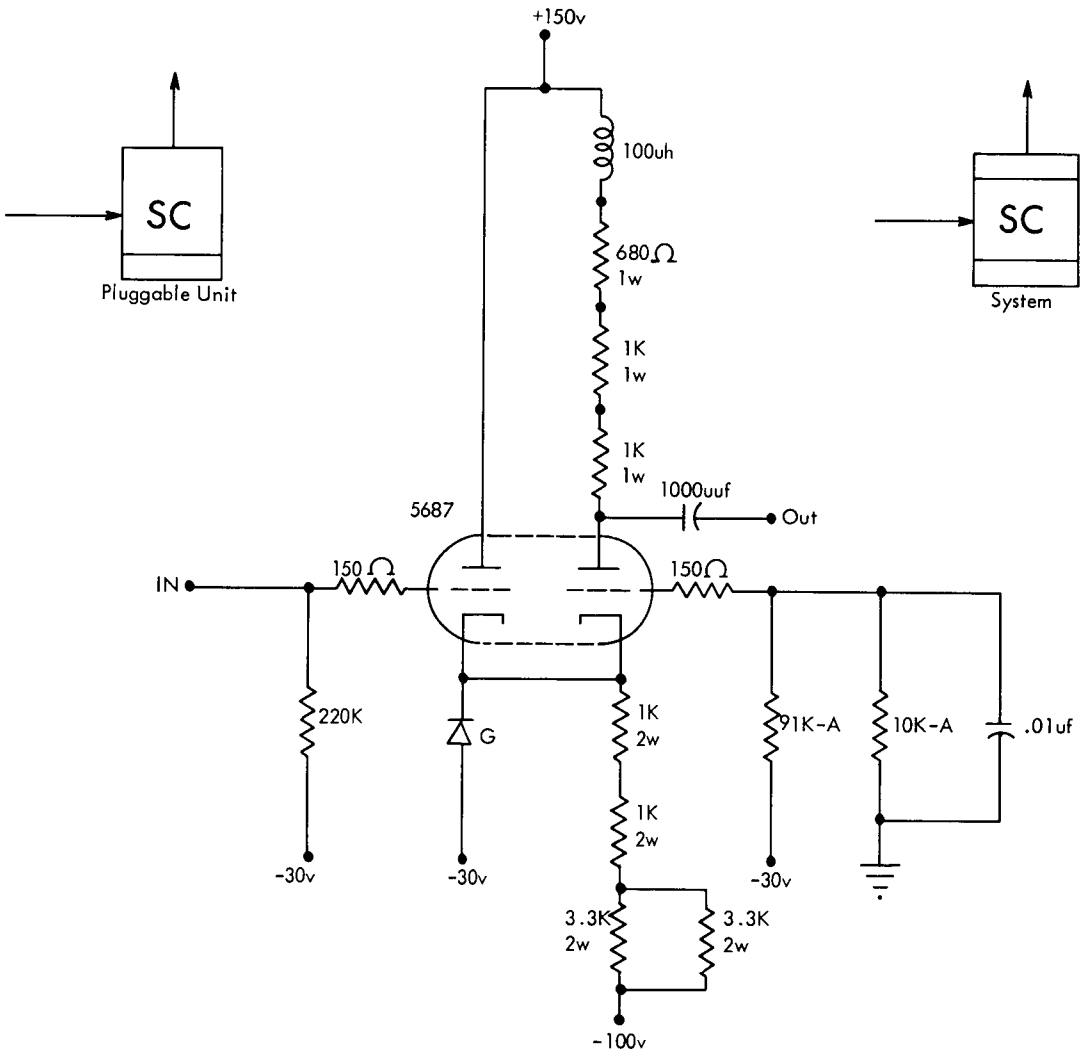


FIGURE B91. SYNC CLIPPER (SC)

2.09.00 PULSE-SHAPING CIRCUITS

2.09.01 Unassigned

2.09.02 Clipper (C_T)

This is a heavy-current diode clamp used in the 726 moving coil circuit (Figure 90).

2.09.03 Clipper (C_L)

This component was assigned to 701 electrostatic memory and is not used now.

2.09.04 Sync Clipper (SC)

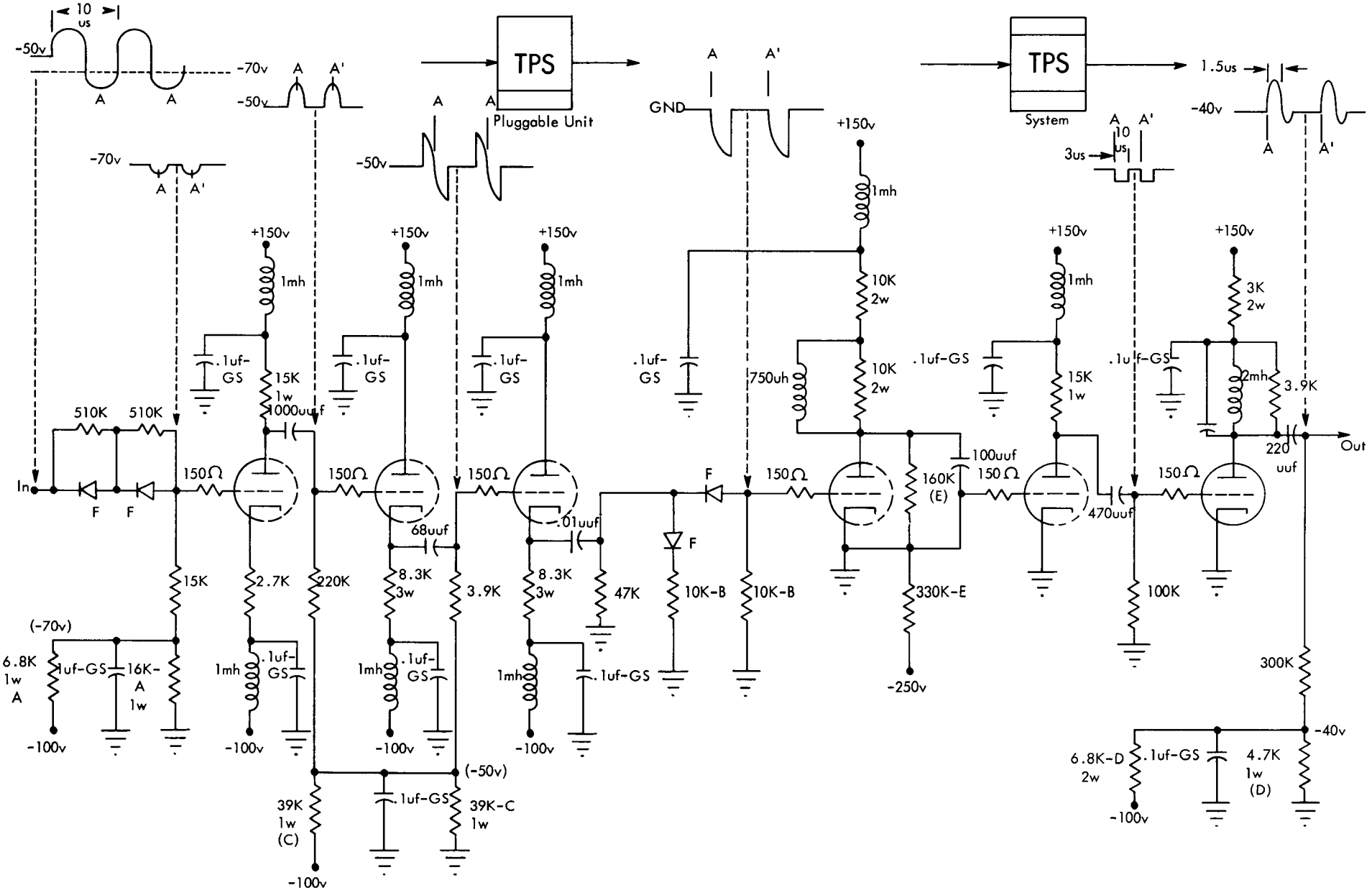
The sync clipper, SC (Figure B91), retains and amplifies the positive peaks of the sync generator output. This circuit is a grounded-grid amplifier, whose grounded grid is about -3 volts. The cathode also operates at about -3 volts. The resistor connected to -30 volts on the grid is part of the RC coupling between this circuit and the sync generator. Low plate and cathode resistances help provide fast pulses; the coil in the plate provides peaking action for a fast positive shift, and the capacitor on the grounded grid helps speed the negative shift.

2.09.05 Timing Pulse Shaper (TPS)

The timing pulse shaper (Figure B92) is designed to produce an output pulse of practically constant amplitude and constant width with a leading edge which is in synchronism with the drum. Its input is from the timing track main amplifier and may vary widely in amplitude. This input is conductively coupled to the shaper, and is biased around -50 volts.

Input to First Stage

The input to the first tube is a diode selector circuit that clips off all of the input pulse more positive than -70 volts. This is accomplished with the diodes, the 15K resistor, and the divider circuit on the grid. The 0.1-microfarad capacitor is used in the divider circuit to hold the output of the divider at about -70 volts for a short length of time. Two diodes are in series so that the back voltage developed across each does not exceed rated value, and the shunt resistors around the diodes are used to equalize the back voltages across the diodes. Although any input signal greater than 40 volts, peak, to peak, produces an output from the selector circuit,



5687 08 A | 5687 08 B | 5965 02 B | 5965 02 A | 5965 03 A | 5687 04 A

FIGURE B92. TIMING PULSE SHAPER (TPS)

a signal of at least 60 volts is required to operate the following circuits. Any signal fed to the selector circuit greater than 150 volts is likely to be distorted because of overdriving of the amplifiers. Therefore, to obtain greatest reliability of operation of the shaper circuit, the output should be between these two values, that is, about 100 volts, peak to peak.

First Stage

The first stage is an amplifier with a gain of approximately three. The gain is small because of the 2.7K degeneration resistor in the cathode circuit. The degeneration is used so that input signals on the grid of the tube may swing at least 50 volts and still allow the circuit to operate class A. As in most of the other circuits in the shaper, some of the supply voltages are decoupled so as to keep transients off the DC power supply lines and to prevent interaction between stages when pulses are transmitted through this circuit.

Second Stage

The second stage is a cathode follower with a capacitively-coupled input, which is biased at -50 volts. The cathode follower is needed to provide a low-impedance source for feeding the differentiating circuit which follows. Variations in amplitude are caused by variations in input pulse amplitudes. The pulse is differentiated so that the portion before the peak appears as a positive pulse on the grid of the third tube, and the portion after the peak appears as a negative pulse on the grid.

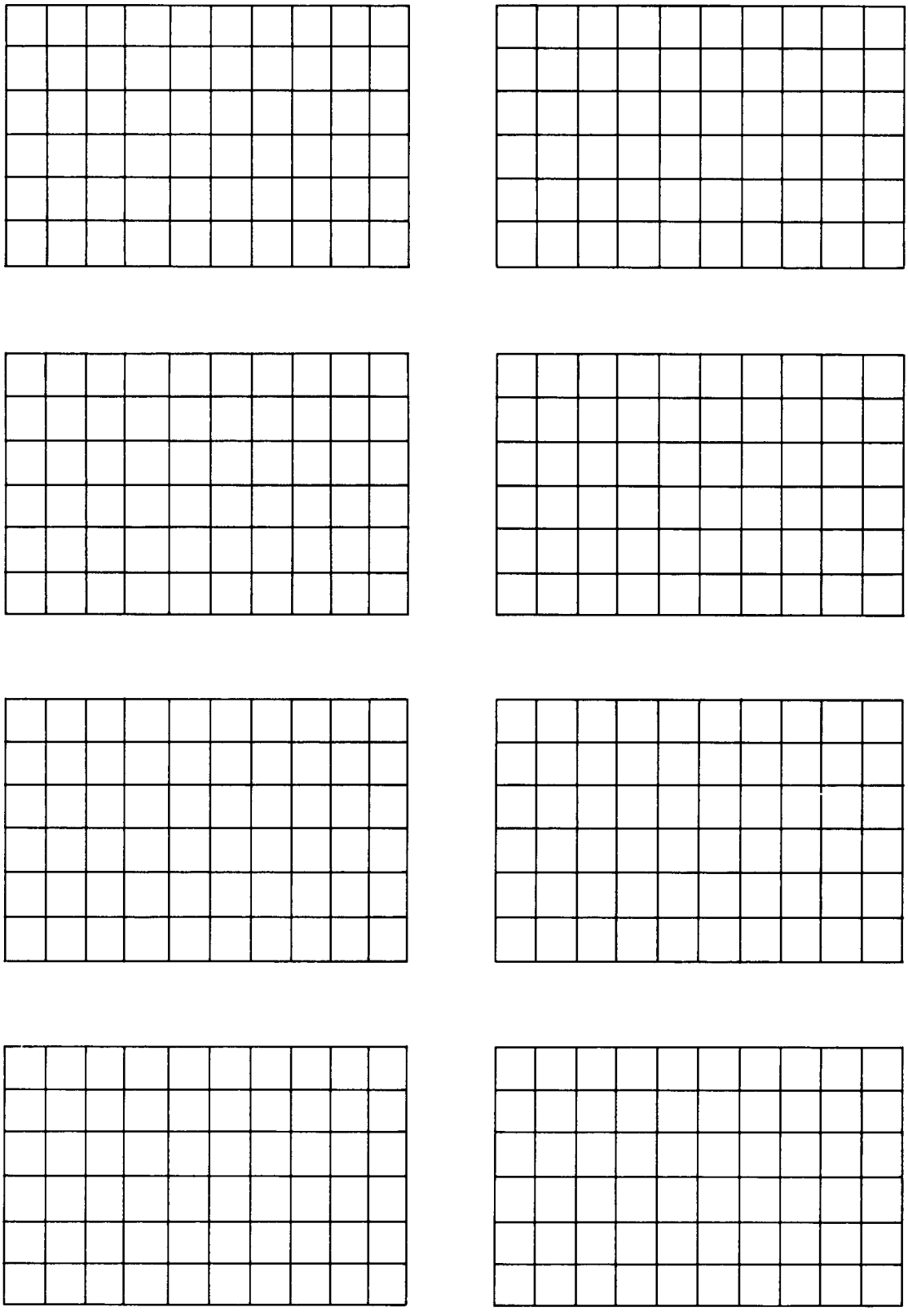
Third Stage

The third stage is also a cathode follower, thus, it does not load the output of the differentiating circuit. Its output is capacitively-coupled into a symmetrical diode circuit. On either the positive or negative shift of the voltage fed to the capacitor, the charging path for the current to the capacitor is the parallel combinations of the 47K resistor and a 10K resistor (the forward resistance of either diode being neglected). This symmetry is necessary to prevent bias buildup that: (1) would cause clipping at some other value than ground and (2) would prevent proper operation of the following stage. The series diode clips off the positive part of the pulse, leaving the negative part intact. It should be noted here that the beginning of the negative transition of this pulse corresponds with the negative peak of the input to the shaper. This is the feature that allows the shaped pulse to be synchronized with the drum. These points are marked A and A' on the theoretical wave forms drawn above each circuit in Figure B92.

Fourth and Fifth Stages

The next two stages are inverters, which are used for squaring the pulses by grid-circuit clipping and plate-current-cut-off clipping. The outputs of the plates of the fourth and fifth stages are square waves.

NOTES



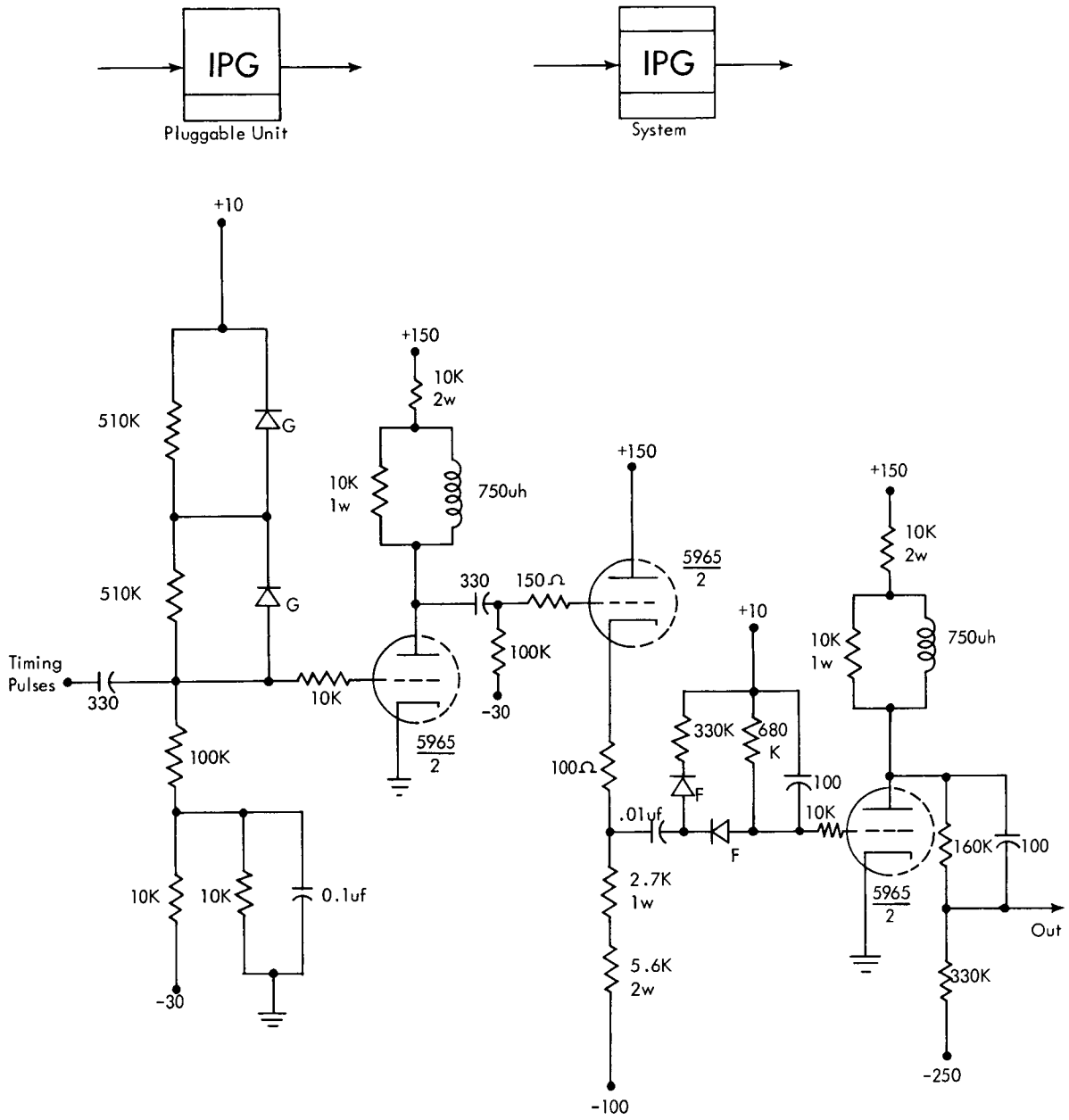


FIGURE B93. INDEX PULSE GENERATOR (IPG)

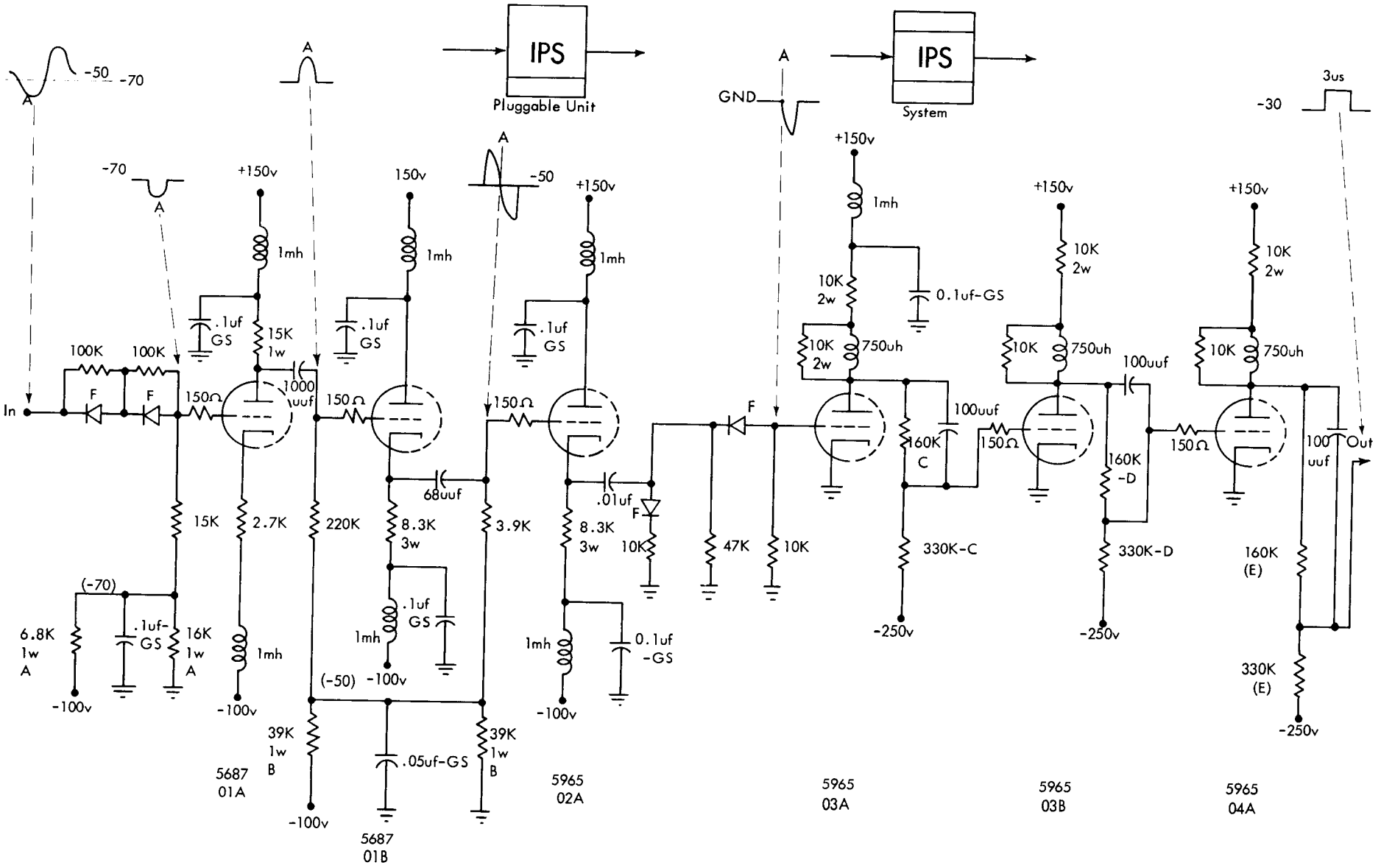


FIGURE B94. INDEX PULSE SHAPER (IPS)

Final Stage

The final stage is a peaker circuit producing an output of practically constant amplitude and width. Since the resonant frequency of the RLC circuit on the plate is about 333 kilocycles, the output pulse, being one half of a cycle, is about 1.5 microseconds in width. The slight negative excursion in the pulse is caused by peaking action when the tube is again caused to conduct, but this portion is clipped off in a succeeding cathode follower, and therefore, does not cause trouble.

2.09.06 Index Pulse Shaper (IPS)

The index pulse shaper (Figure B94) is designed to produce an output pulse of practically constant amplitude, which is in synchronism with the drum. Its input is from the main amplifier for the index tracks and may vary widely in amplitude. As in the timing pulse shaper, the input is biased at -50 volts and is conductively coupled to the index pulse shaper.

The first four stages are identical in construction and operation to the first four stages of the timing pulse shaper (Figure B92), and the signal amplitude required is also identical. The last two stages are standard inverters with increased compensation in the output dividers. This increase is necessary because of the high-input Miller capacitance in the succeeding stages. As in the timing pulse shaper, these inverters shape the pulse by grid-circuit clipping and plate-current-cut-off clipping. The output is practically a square pulse of constant amplitude, but its width is proportional to the amplitude of the input to the shaper.

2.09.07 Index Pulse Generator (IPG)

The index pulse generator (Figure B93) is used on the drum to indicate the beginning of the timing track. The amplified timing pulses are fed into the input stage of the index pulse generator through the 330-uuf capacitor. The signal is large in amplitude and must be clamped to +10 volts at the input to prevent overdrive. The timing pulses could be fed in through a divider network but then the effect of a steep wave front would be lost. The first timing pulse after the 150-usec gap causes generation of the index pulse. This pulse must be detected early, because of the arrangement of the index and timing pulse circuits in section 7 of Systems. The timing pulses on the drum surface are 12 usec apart. When the timing pulse causes the input of the index pulse generator to go positive, the plate of the first tube goes in a negative direction. This negative signal is fed through a capacitor to the grid of the next stage. This cathode follower output also goes negative. The 100-uuf capacitor in parallel with the 690K resistor is charged with the negative pulse. When the timing pulse causes the input to the first stage to go negative, the resulting positive pulse from the output for the cathode follower has no effect on the 100-uuf capacitor. The grid of the output tube is controlled by the voltage that appears across the capacitor; as it is negative, the tube is cut off. The time constant of this RC network is larger than 12 usec; therefore, as long as the timing pulses appear every 12 usec, the output voltage does not change. When the 150-usec gap arrives, the capacitor in the grid circuit of the output stage has time to discharge. This allows the output tube to conduct; its plate is held down. Then the first timing pulse appears at the input stage, the capacitor is charged again and a positive pulse appears at the output. This pulse is used to generate the index pulse.

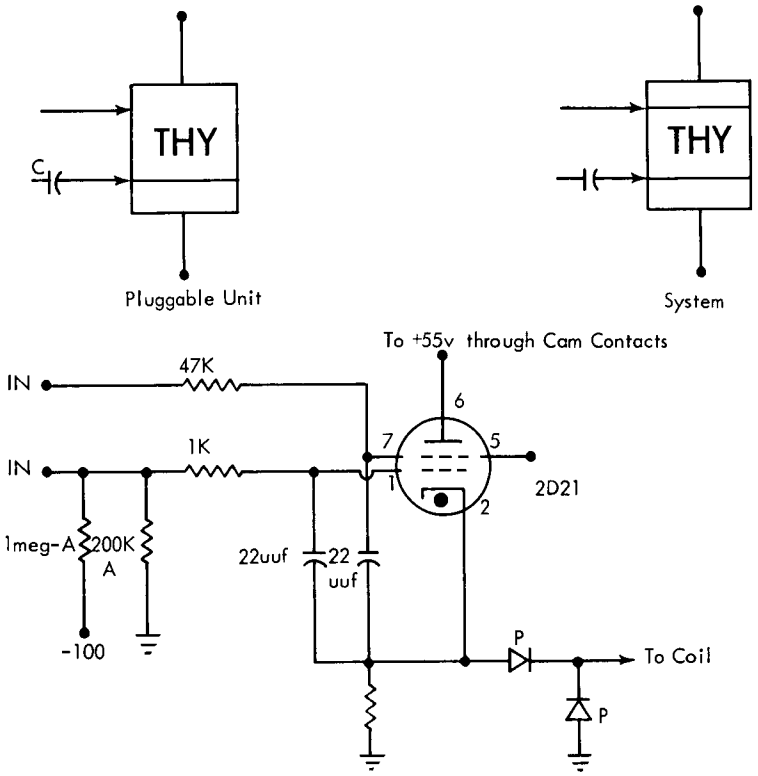


FIGURE B95. THYRATRON (THY)

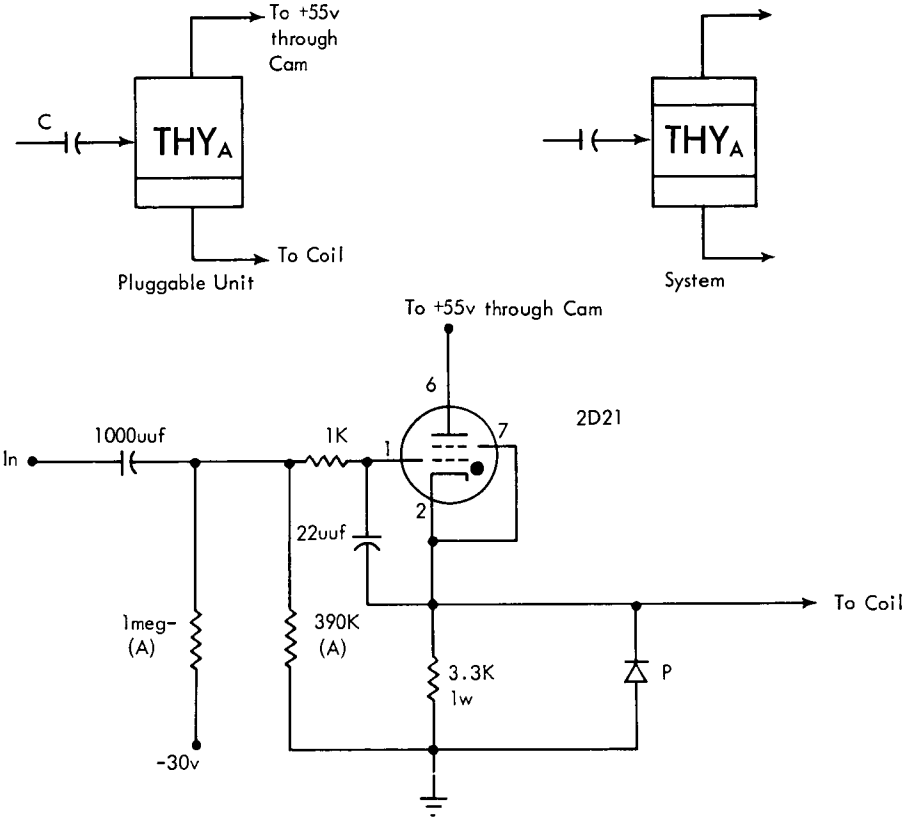


FIGURE B96. THYRATRON (THY$_A$)

2.10.00 SPECIAL CIRCUITS

2.10.01 Current Adder (CA)

This component was assigned to 701 electrostatic memory and is not used now.

2.10.02 Current Switch (CS)

This component was assigned to 701 electrostatic memory and is not used now.

2.10.03 Cathode Ray Tube (CRT)

This component was assigned to 701 electrostatic memory and is not used now.

2.10.04 Level Shifter (LS)

This component was assigned to 701 electrostatic memory and is not used now.

2.10.05 Sampling Amplifier (SA)

This component was assigned to 701 electrostatic memory and is not used now.

2.10.06 Thyratron (THY)

The thyratron circuit THY (Figure B95) is used to pick relays in all the card machines. This circuit is also used to fire the print magnets and punch magnets. It is necessary to have an up line at each of the two inputs in order to fire the tube. When fired, the gas in a thyratron ionizes and remains in conduction until the plate voltage falls to a low level or the circuit is broken. In practice, the plate voltage to all the thyratrons is fed through CB's. Therefore, the thyratron is de-ionized by the break of the CB.

The coil or magnet to be operated upon is found in the cathode circuit of the thyratron where it is shunted by a resistor and a diode. The resistor provides a smooth current through the tube while overcoming the reactance of the inductive load. The diode swamps any attempt of the inductive load to oscillate when power is removed. In doing so, it also prevents generation of harmful voltages caused by inductive kick.

2.10.07 Thyratron (THY_A)

The thyratron circuit THY_A (Figure B96) is identical in operation to the THY (Figure B95). It is used to pick relays in the card machines. The main difference is that this circuit is operated by one AC input. The fact that the input is AC determines that the input may be a long one without interfering with operation. The single input circuit is used for logic reasons. The double input above was used to save an AND circuit.

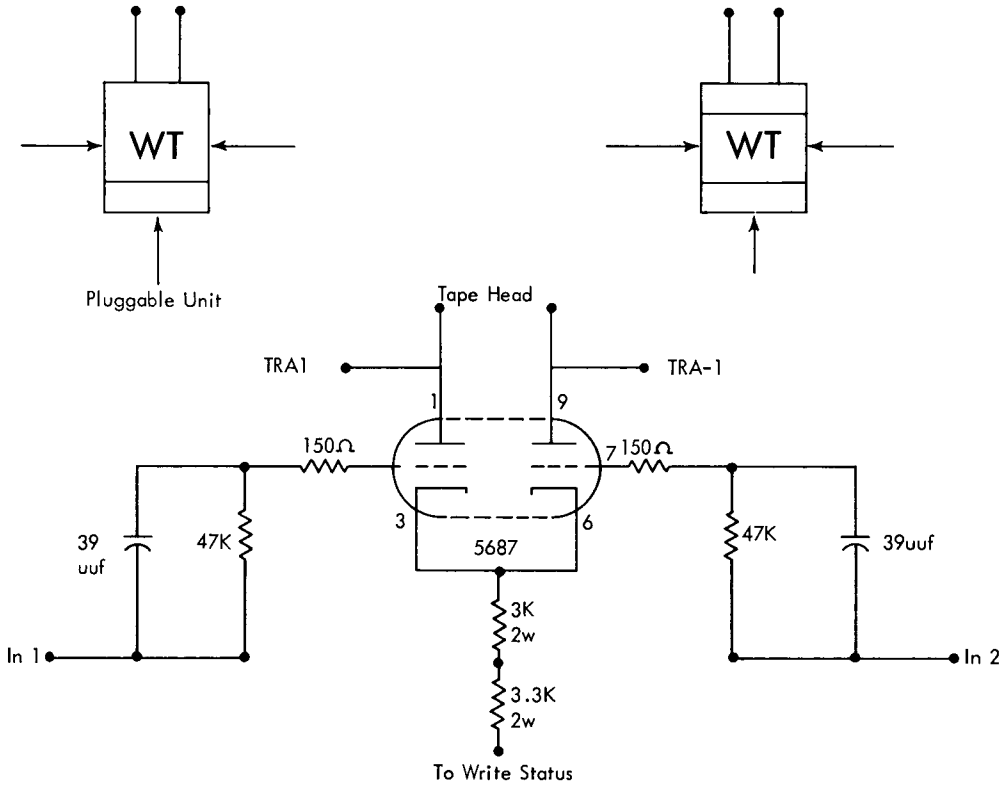


FIGURE B97. WRITE TUBE (WT)

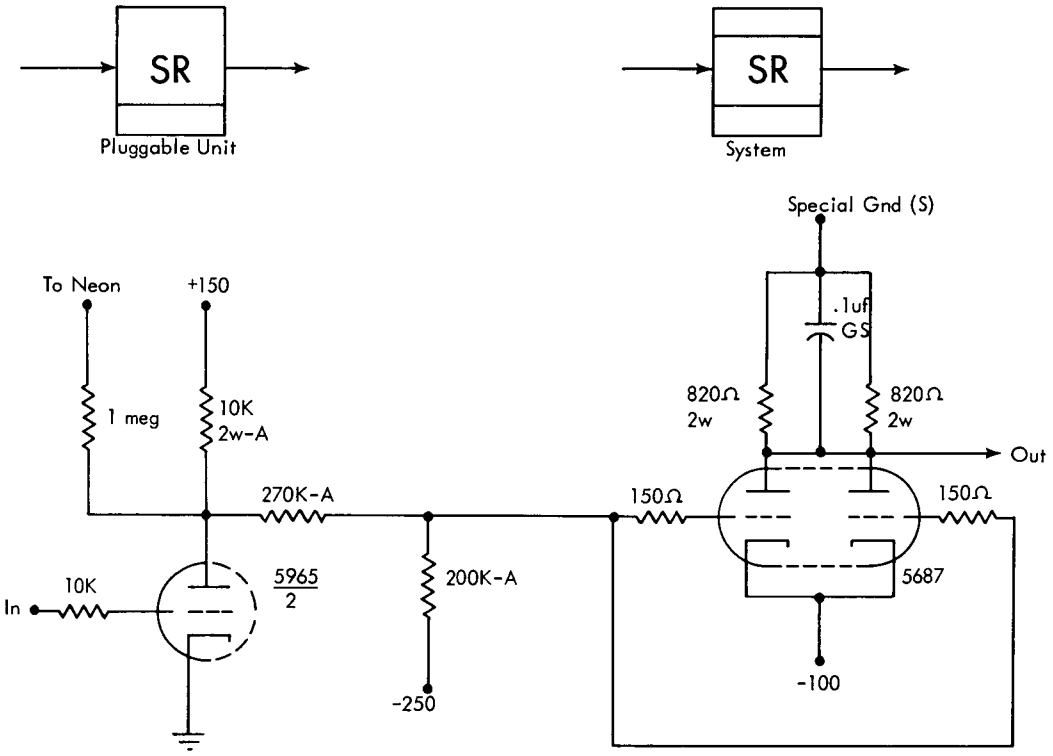


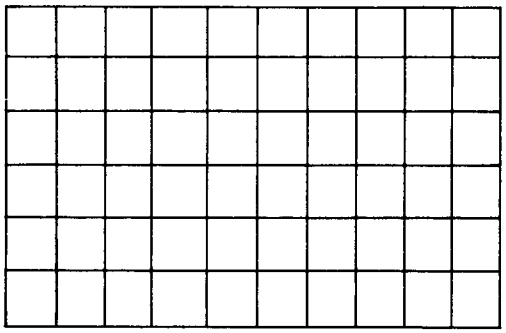
FIGURE B98. SWITCH READ (SR)

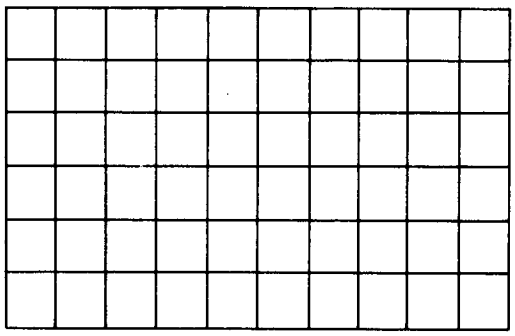
2.10.08 Write Tube (WT)

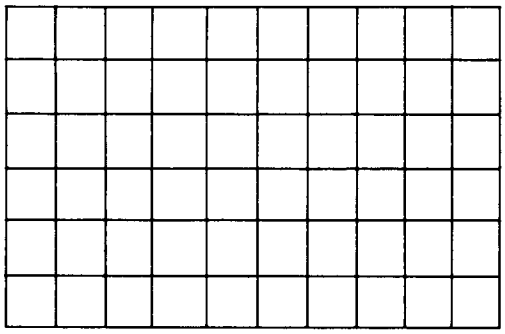
WT is the symbol of the tape write tube circuit used to supply current to the write heads (Figure B97). It is fed a push-pull input from the tape write trigger, T_T with levels of -15 volts and -68 volts. These levels appear upon the grid of the WR as approximately -30 volts and -70 volts. This circuit is actually a cathode follower OR circuit with one tube always cut off in the DC state. The inputs are protected from excessive grid current by the 47K resistors. The cathode return is connected through a relay to -100 volts when the circuit is turned on, and to ground when the circuit is turned off. The peaks in voltage are caused by the inductance of the head. If the grid goes positive, the corresponding plate shows a negative peak at that time. The DC current in a head is about 11 milliamperes. This component is used with the 701 only.

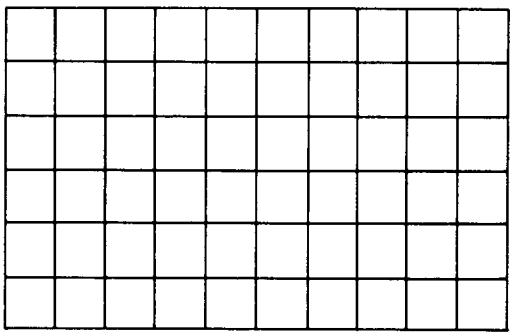
2.10.09 Switch Read (SR)

The switch read, SR, (Figure B98) is used to switch the reading of the drum from one logical drum to the other. There are four heads and four pre-amps for each drum amplifier. Only one of these can be activated at any one time. To activate any one read head and its pre-amp, the lower end of the read winding is grounded. The other end feeds the grid of the pre-amp. This ground is made through the two 820-ohm resistors in the plate circuit of the SR. When this SR tube conducts, the current through the 820-ohm resistors causes the voltage at its output to be about -20 volts. This is enough to cause the associated pre-amp to be cut off. A positive signal on the grid of the input stage of the SR activates the read winding and the pre-amp by cutting off the output tube of the SR, thereby grounding the end of the read winding.









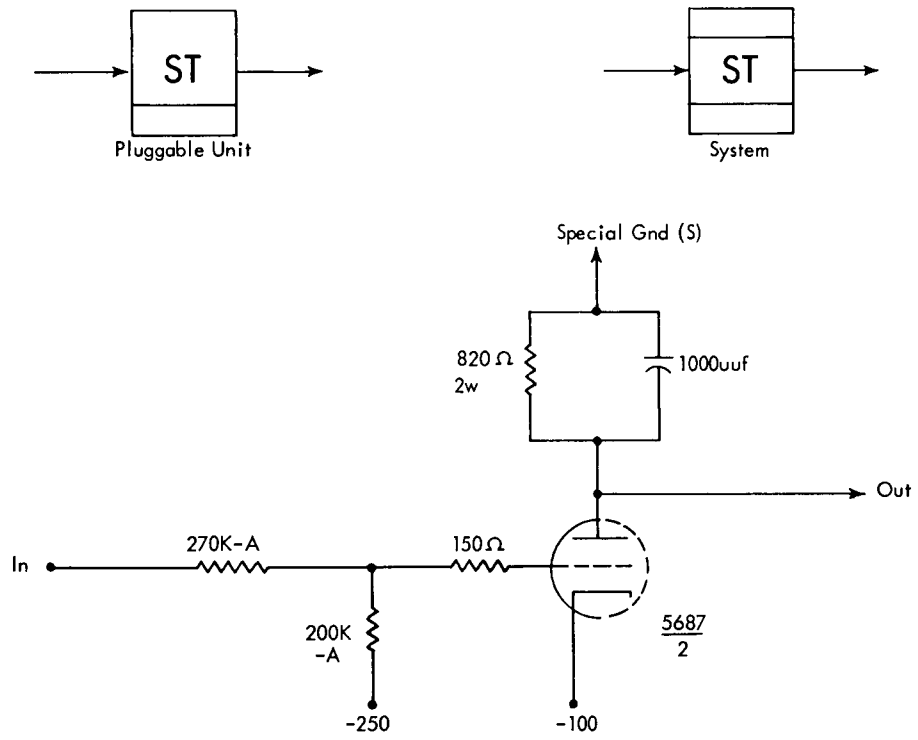


FIGURE B99. SWITCH TIMER (ST)

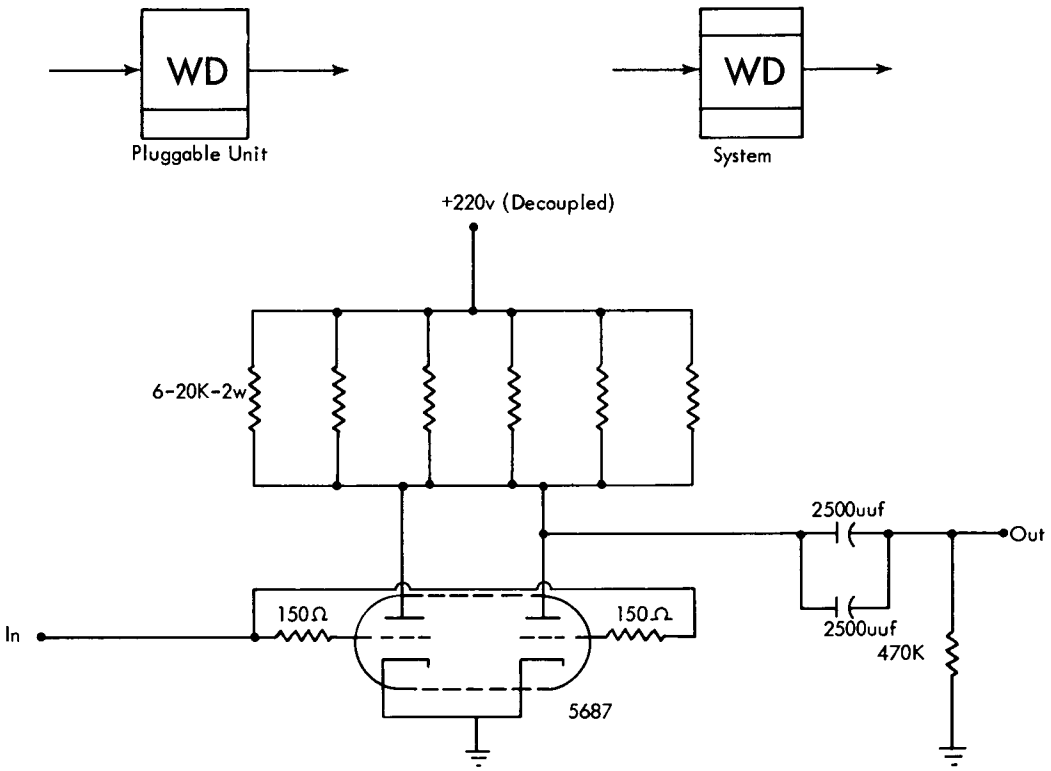


FIGURE B100. WRITE DRIVER (WD)

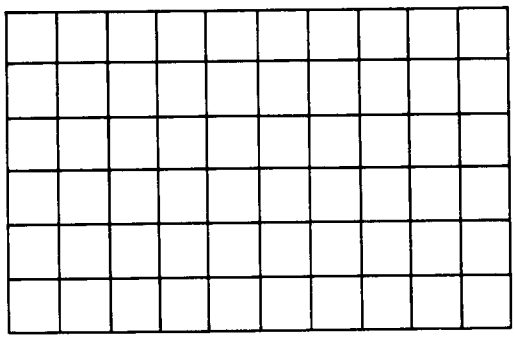
2.10.10 Switch Timer (ST)

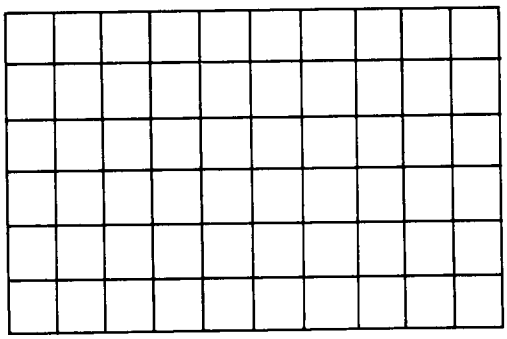
The switch timer, ST, (Figure B99) is used to activate a pre-amp for a timing track. Two read heads read the timing tracks on the drum, one for each physical drum. The read windings on these two heads are grounded through 820-ohm resistors in the plate circuits of the ST. There are two ST's or one for each timing track. To activate a timing pre-amp, the ST must have a negative signal at its grid. To de-activate a timing pre-amp, a positive level is applied to the grid of the ST. The resulting voltage drop across the 820-ohm resistor biases the associated pre-amp below cut off. Only one timing track can be read at one time.

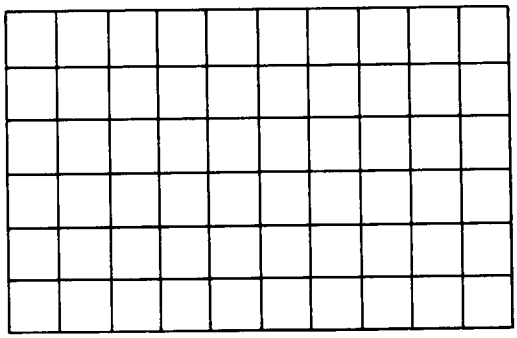
2.10.11 Write Driver (WD)

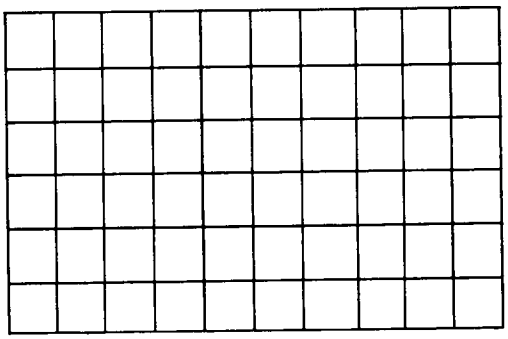
The write driver, WD, (Figure B100) is used in the write circuits in the drum. The output shown on Figure B100 is connected, when in use, through a relay point, through half of a drum write head to ground. The WD is normally cut off. During this period, the two parallel 2500-uuf capacitors charge to the supply voltage. Also, during this period, the charging current (flowing through the write head) is limited by the plate load resistance of the WD. This limited current is small enough so that nothing is written on the drum.

A gated delayed timing pulse is applied to the grid of the tube lowering the plate voltage and providing a low impedance discharge path for the capacitors through the tube. The 470K resistor across the head damps any attempt at oscillating. This circuit is discussed in detail in the drum section of Electronic Operations Customer Engineering Manual of Instruction, Volume II.









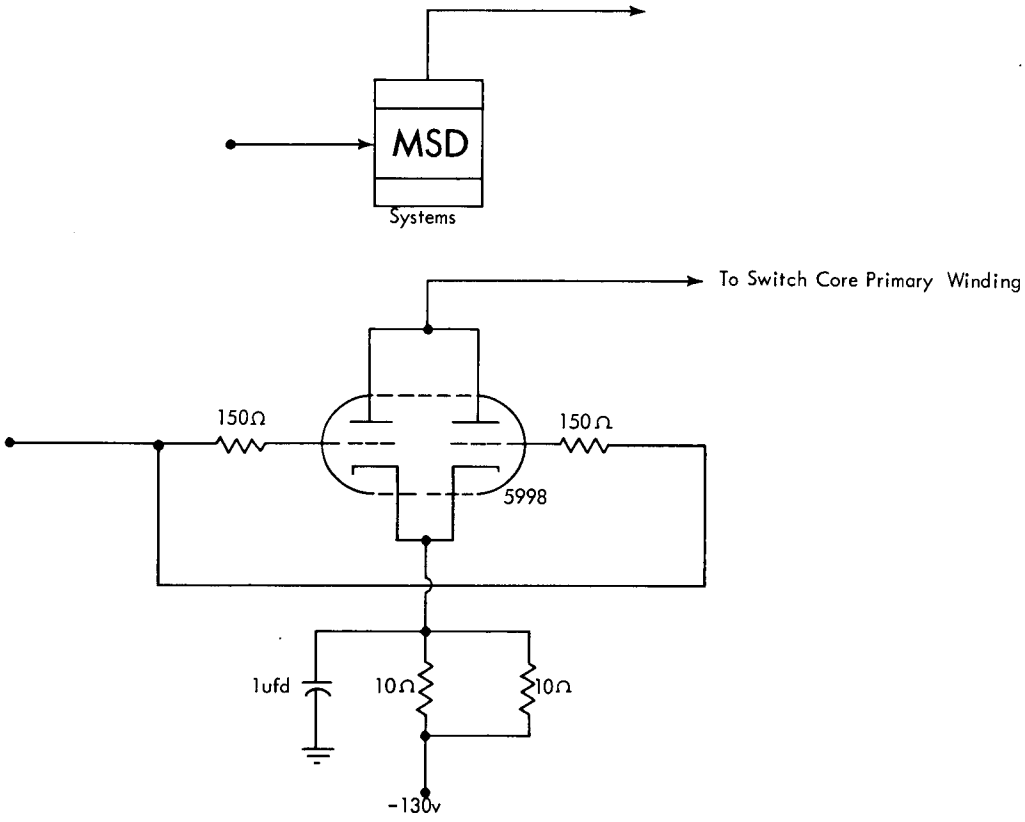


FIGURE B101. MATRIX SWITCH DRIVER (MSD)

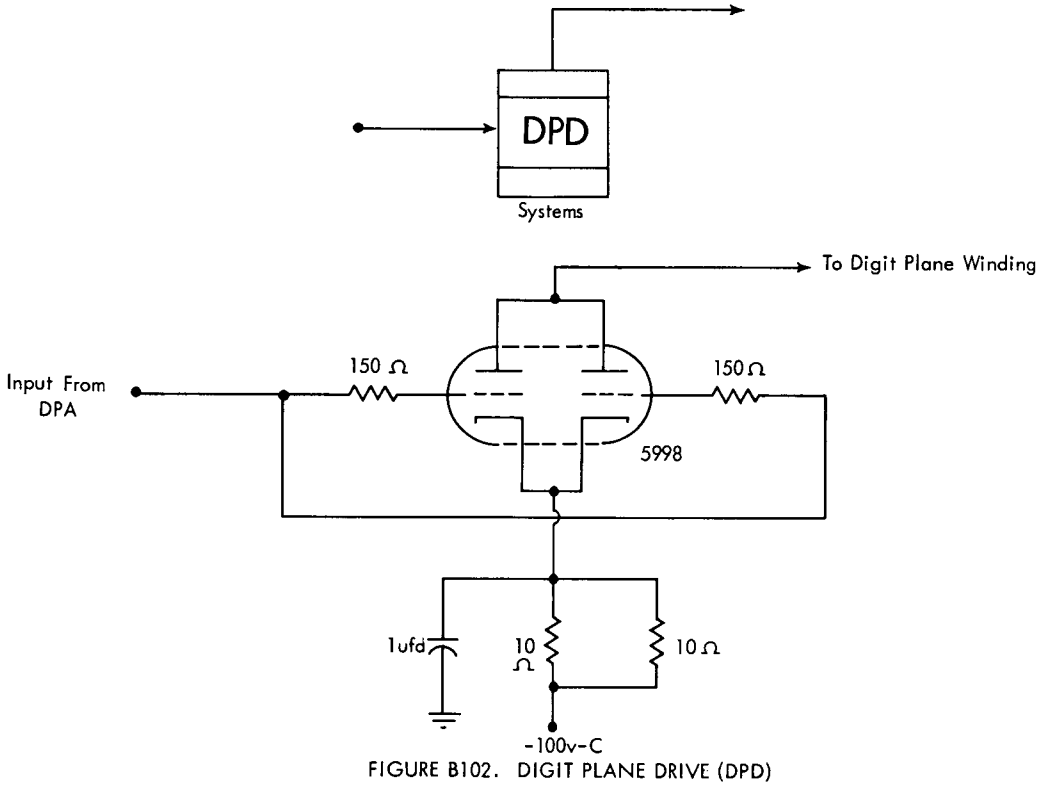


FIGURE B102. DIGIT PLANE DRIVE (DPD)

2.10.12 Matrix Switch Driver (MSD)

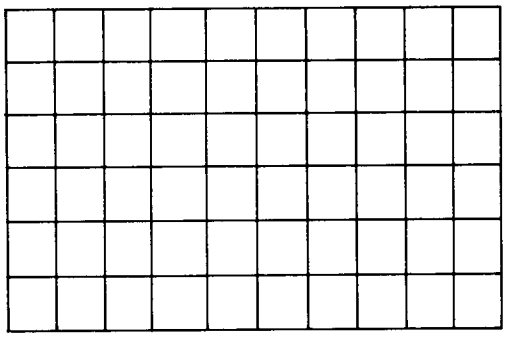
The MSD (Figure B101) is similar in operation to the DPD (Figure B102). It is fed by a MSA (Figure B57 or B58) and its plate load is a primary winding drive line in the switch core plane plus a precision feedback resistor.

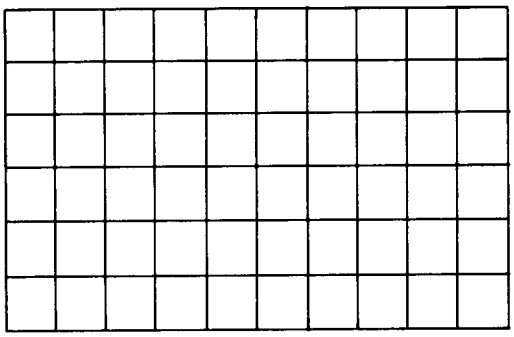
2.10.13 Digit Plane Driver (DPD)

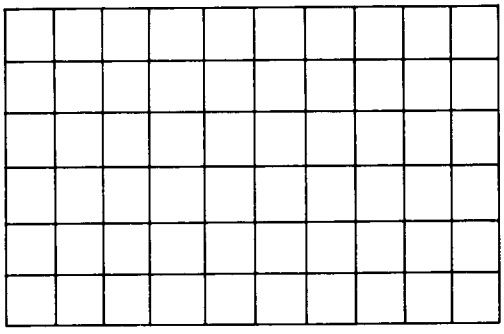
The DPD (Figure B102) is a power amplifier, supplying surge currents of about half an ampere to the digit plane (inhibit) windings in the core plane. The signal from the digit plane amplifier (Figure B59) is fed to the input of the DPD. The plate load of the tube is the inhibit winding itself plus a precision resistor from which the feedback is sent to the DPA.

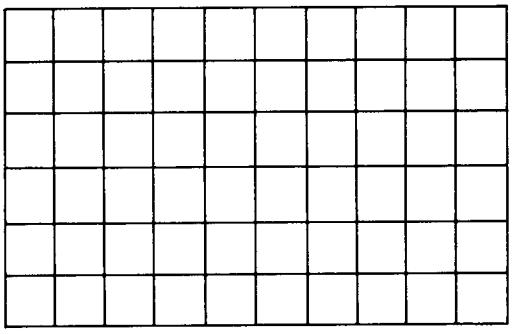
2.10.14 Matrix Switch Driver or Digit Plane Driver (MSD or DPD)

These components used with the 738 differ from Figures B101 and B102 by the addition of a 1-megohm resistor between the input and -250 volts to cut off the driver in case of an open input circuit. The cathode supply is -160 volts.









Component Circuits

Book C. 702-705 Components

CONTENTS

CONTENTS (continued)

CONTENTS (continued)

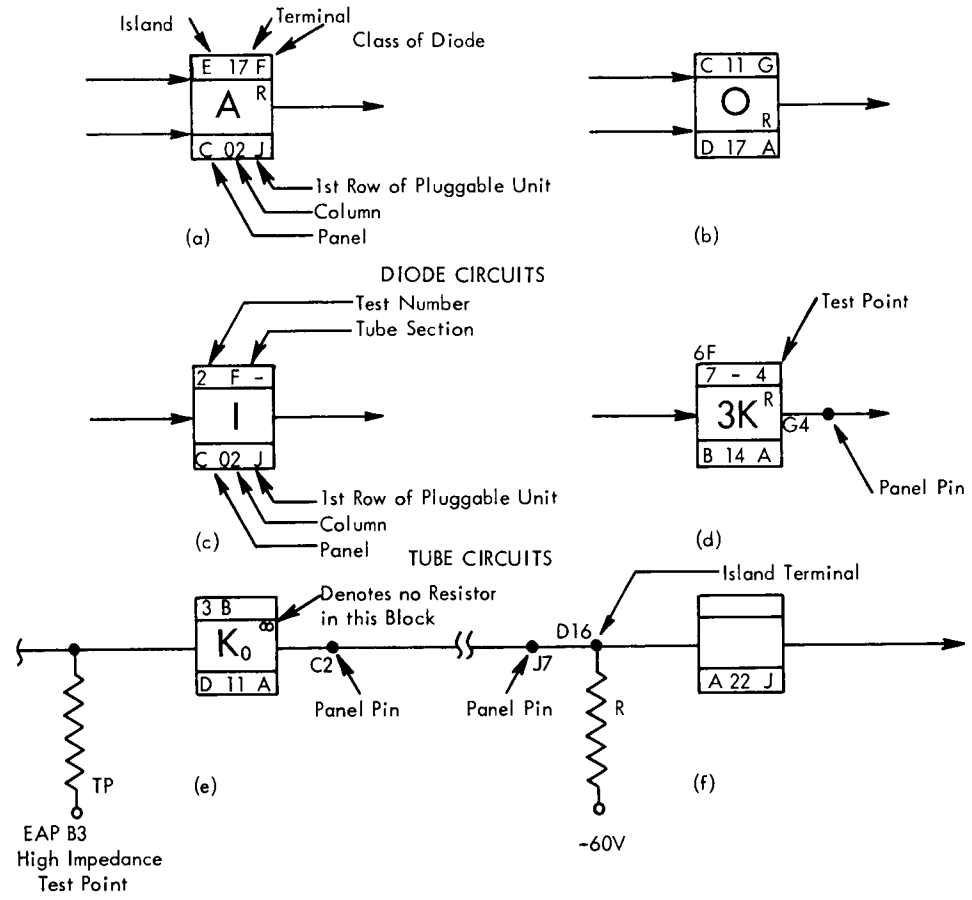


FIGURE C1. LOGIC BLOCK NOTATIONS

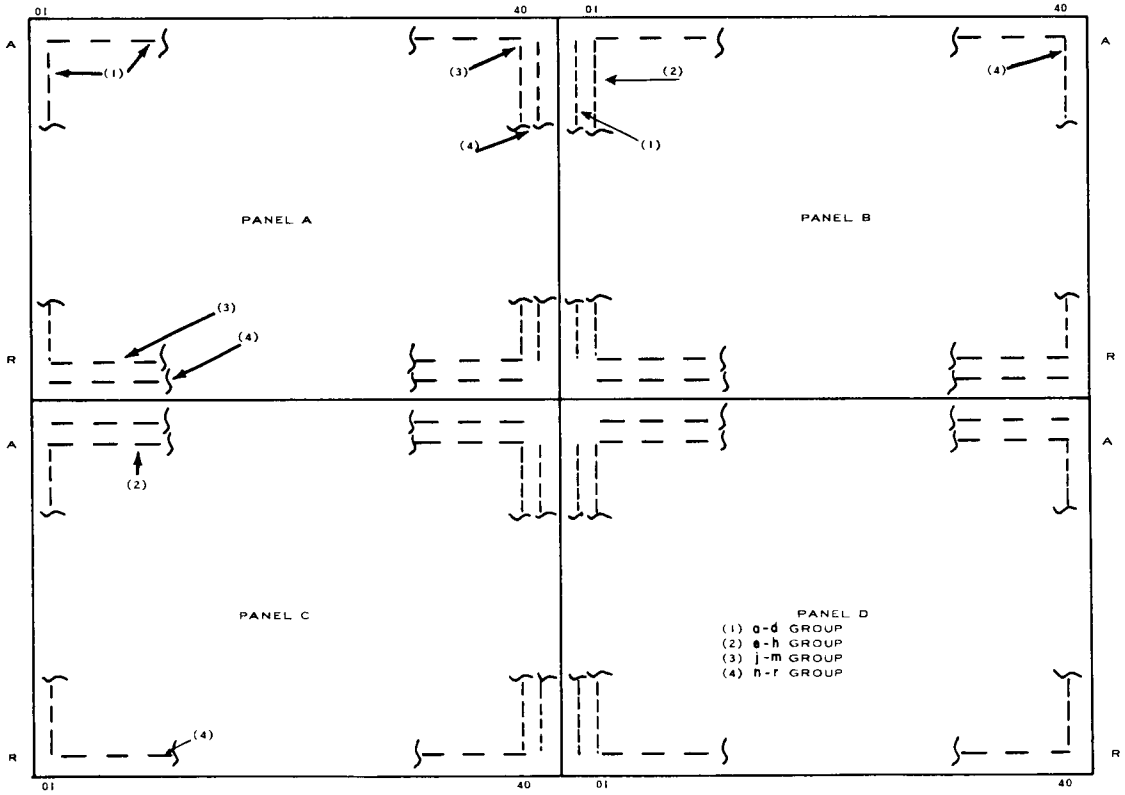


FIGURE C2. EDGE CONNECTOR LAYOUT

1.00.00 GENERAL INFORMATION

1.01.00 CIRCUIT LOCATION

For location purposes, logic blocks fall into two major classifications: tube circuits and diode circuits. In both cases, the procedure for locating the pluggable unit containing the circuit is the same.

Figure C1 shows typical representations of both diode and tube circuit logic blocks. Note that the lower section of each block is similar. The first symbol in the lower section indicates the panel, the second symbol indicates the column of that panel and the third symbol indicates the row which the first tube of the pluggable unit occupies. Example: C02J indicates panel C, column 02, and the first tube of the pluggable unit, J. This holds true for both types of circuits.

The diode circuit block contains, in the upper section, notations to further locate the circuit within the pluggable unit. The first symbol indicates the "island" of the unit, the second symbol indicates a "terminal" on the island and the third symbol indicates the "class of diode" or diodes used in the circuit. The identified island terminal is a "junction" point where the diodes meet a resistor. In the center section of each block is the circuit name. Diode blocks also contain the value of resistor R that is used in the circuit.

Tube circuit logic blocks contain notations to identify what tube or tubes in the pluggable unit are used. The first symbol in the upper section indicates the tube number of that unit (1-8) while the second symbol indicates front or back portion of the tube used. If the complete tube is used, a hyphen denotes intentional omission of F or B. When more than one tube is used in a block, all tube sections are noted (Figure C1d). The 3K block uses both halves of tube 7 and the front half of tube 6. The upper right section is used (mostly in I or K blocks) to denote an output test point. The 4 denotes a panel pin number and is identical to the G4 on the output line. The G notation means that the pin is directly beneath the seventh tube of pluggable unit A.

Special notations that appear in various logical blocks are explained with their circuits. The upper section of T blocks is described under Triggers (Book A, Section 2.06.00).

1.02.00 TEST POINTS

Wherever possible, inputs and outputs to a logical block are brought out to a panel pin as an aid to servicing. The panel pin is identified from the tube directly above it or as close to it as possible. In diode blocks, the nearest available panel pin is used.

High impedance test points are used wherever a direct wire affects circuit loading. A one-megohm resistor is placed in series with the panel pin and is noted on the Systems page (Figure C1e).

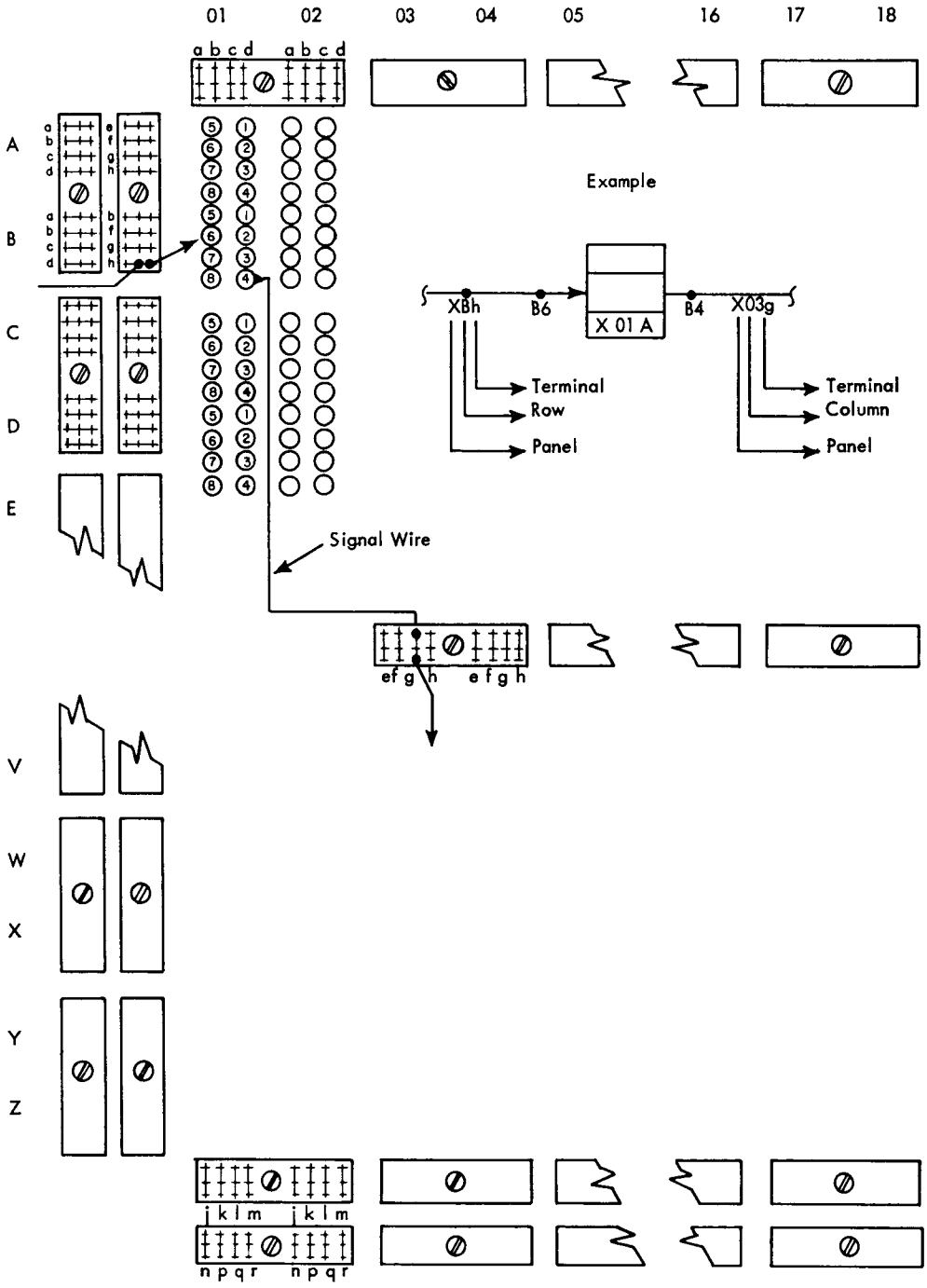


FIGURE C3. EDGE CONNECTOR LAYOUT

1.03.00 MISCELLANEOUS NOTATIONS

Frequently circuits that normally contain a resistor value in their logic block contain an infinity sign (∞). This symbol means that the return resistor is in another circuit (Figure C1e).

Figure C1f shows an input returned to -60 volts outside the logic block. This resistor keeps the line from floating when a cable connector or relay point is opened. A floating input can produce an unwanted up level in certain circuits. D16 is the island terminal in the pluggable unit associated with the nearest logic block.

1.04.00 EDGE CONNECTORS

When signal or service wiring enters or leaves a panel, it is routed through an edge connector (EC), as shown in Figures C2 and C3. Because connectors are pluggable, circuit isolation is convenient.

The connectors are arranged in two groups of four on each mounting block. Because of the layout arrangement, each group is located by the alphabetic or numerical panel index system (Figure C3). Terminals in each individual row or set are shorted to provide continuity.

EC's are laid out around the perimeter of the panels in the central processing unit (CPU), while control units have EC's on the sides of the panels where the cabling enters the panel. Where excess wiring enters a panel (hinge side of the control unit or where panels butt together in CPU) two rows of EC's are provided. Units other than CPU may have a horizontal row of EC's in the middle of the panel.

The EC's laid out horizontally on the top, middle, or bottom row are located by the numerical indexing on each panel (01, 02, and so on) as in Figure C2. The alphabetic indexing (A-Z) locates the vertical columns on the left or right side of the panel. The alphabetic index is A-R or A-Z, depending on the number of pluggable units (two or three) mounted on the panel. Individual terminals are labeled a-r (omitting i and o) left to right and top to bottom. Therefore, EC's in the extreme left column are the a-d group; the adjacent column is the e-h group; the two columns on the right are the j-m group and the n-r group. The same procedure follows for the horizontal rows (top to bottom). If only one column is used on the left, it is the a-d group. If only one column is used on the right it is the n-r group. Therefore, if a row or column of EC's is omitted, the indicated grouping is not used.

An example of EC labeling and location is shown in Figure C3. The labeling on the lines entering and leaving the logical block is an example of labeling as found in the Systems pages. Typical wiring is shown entering the panel, through EC (XBh), to pluggable unit terminal (B6), into the component circuit and out on terminal B4, to EC (X03g), then on to further components (not shown).

1.05.00 PANEL DESIGNATION

Each panel of the machine has its own designation. The following is a list of the symbols used:

A-D	CPU
E-H	Drum
J	Printer Control Unit
K, L	Printer
M, V, W, Z	Memory
N	Punch Control Unit
P	Punch
Q	Reader Control Unit
R	Reader
S	Tape Control Unit
T	Tape
Y	Typewriter

1.06.00 LINE NOMENCLATURE

To enable customer engineers to locate circuits and better understand them, various labels are attached to the lines between blocks and pages. The labeling on the lines gives a point-to-point description of a wire going from one component circuit to another. A line may contain pluggable-unit island terminals, panel pins, edge connectors and cable connectors. Lines contain routing information (where the line came from and where it goes). A line is also named in order to simplify cross referencing pages. This name is descriptive to aid in the understanding of the circuit.

2.00.00 COMPONENT CIRCUIT DESCRIPTIONS

This section contains a description of each component circuit represented by a logic block. The circuit descriptions are arranged in the same order as the circuit schematics that are found in the systems for each machine. Thus, 2.1.1 (Inverter) is the same circuit as found on C.01.01. Numbers unassigned as of this writing are so noted.

Each circuit description is designated by a three-part decimal number. The first part of the number is a 2, which represents this section. The second part of this number represents the functional classification of the circuit. These functional classification numbers are as follows: (1) inverters, (2) triggers, (3) single shot multivibrators, (4) amplifiers, (5) cathode followers, (6) diode circuits, (7) delay circuits, (8) pulse generators, and (9) thyratron circuits. These classifications are rather loose, and some circuits may fall into either of two categories. The third part of the number is the number of the circuit within its classification. The circuits are usually arranged alphabetically within one category.

Many of the component circuits are not complete in themselves; that is, components in the circuits that feed them or are fed by them are just as important to the circuit operation as the components shown in the corresponding block.

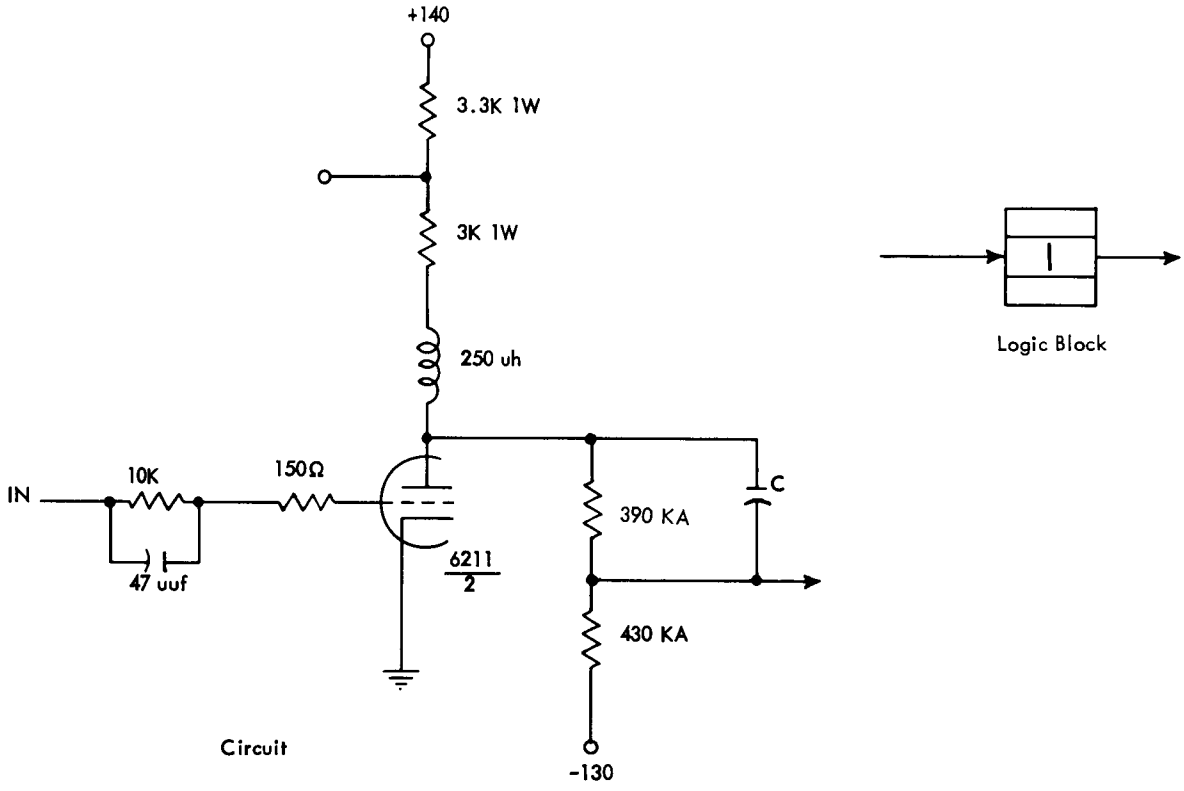


FIGURE C4. STANDARD INVERTER -- I

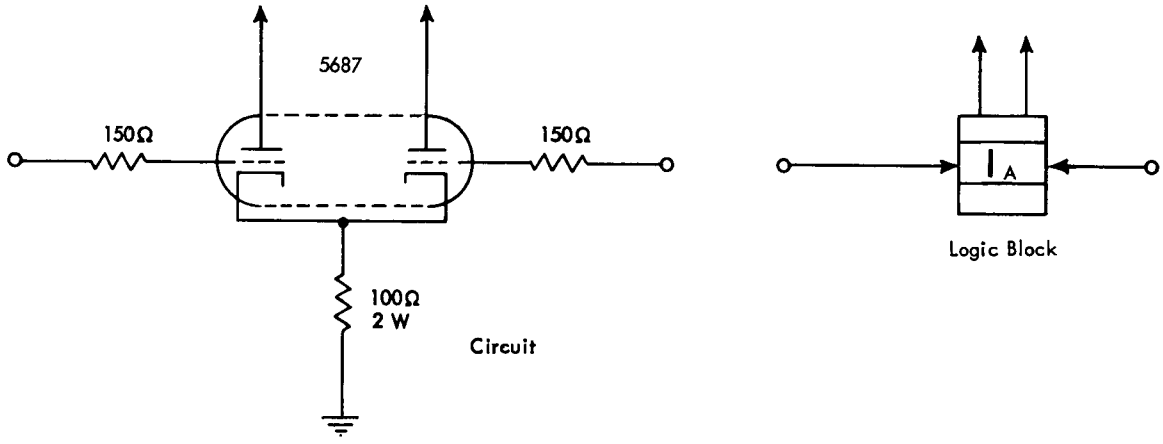


FIGURE C5. INVERTER (WRITE AMPLIFIER -- DRUM) -- I_A

2.01.00 INVERTERS

2.01.01 Standard Inverter (I) (I_K)

The standard inverter I and I_K (Figure C4) is described in "Standard Circuits," section 2.05.00, Book A.

2.01.02 Inverter (Write Amplifier--Drum) (I_A)

The inverter (write amplifier--drum) I_A in Figure C5 is used in the drum write circuits to write the ones and zeros on the drum through the drum write coils. The I_A is made up of two half-tubes with a common 100-ohm cathode resistor returned to ground. Each I_A has two inputs. One of these inputs is "write 0." The other input is "write 1." The two plates return, through opposite ends of the write coil, to the cathode follower K_H. See section 2.5.9, Book C, for the operation of the cathode follower K_H.

Since both the inputs to the I_A and the output of the K_H are peaked pulses, the I_A is operative only when these peaks occur in coincidence. Because the I_A draws its plate current through the K_H, the tube currents are rather heavy (250 ma). This, however, is not detrimental because the duty cycle is short (1.2 usec). As a service aid, the cathode is brought out to a panel pin and the test point is noted on the Systems page.

2.01.03 Moving Coil and Forward Reverse Driver (Tape)

The inverters I_E, I_F, and I_M together with cathode follower K_A (Figures C6 and C7) comprise the circuits necessary to operate the moving coil mechanism in the tape drive unit. Figure C6 shows the logic block circuit and C7 shows the circuit schematic.

Circuit Description. All inputs are nominal +10v to -30v signal levels. When "start" comes up, "stop" is brought down. This causes the inverter I_F in the upper left-hand corner of Figure C7 to cut off. As the plate voltage rises, it brings up the left end of the moving coil through the parallel cathode followers K_A. At this same time, the inverter I_E at the middle left of the page is cut off as was the I_F, because "stop" is down. As the inverter I_E cuts off, its output (+ 100v shift) causes the inverters I_M located at the left center of the page, to conduct. One inverter, I_M, is AC coupled while the other is DC coupled. Both inverters I_M complete the path for the current through the I_F, K_A and the moving coil The current causes the coil to move the mechanical linkage in such a way as to cause the tape to move. Whether the tape runs forward or backward depends upon whether "reverse" is up. The cathode followers K_A are used to isolate the start and stop circuits from each other because they share the same load.

The circuits used to stop the tape are similar to those used to start the tape. The difference is that the start-line-down condition operates the circuits on the right side of the page in the manner explained above. This causes the current to flow in the opposite direction through the moving coil and operates the linkage in such a way as to stop the tape. It was mentioned above that one I_M was AC coupled and one DC coupled on both the start and the stop circuit. This means that the AC-coupled I_M, with a -130v returned cathode, provides a heavy current for the moving coil only for a

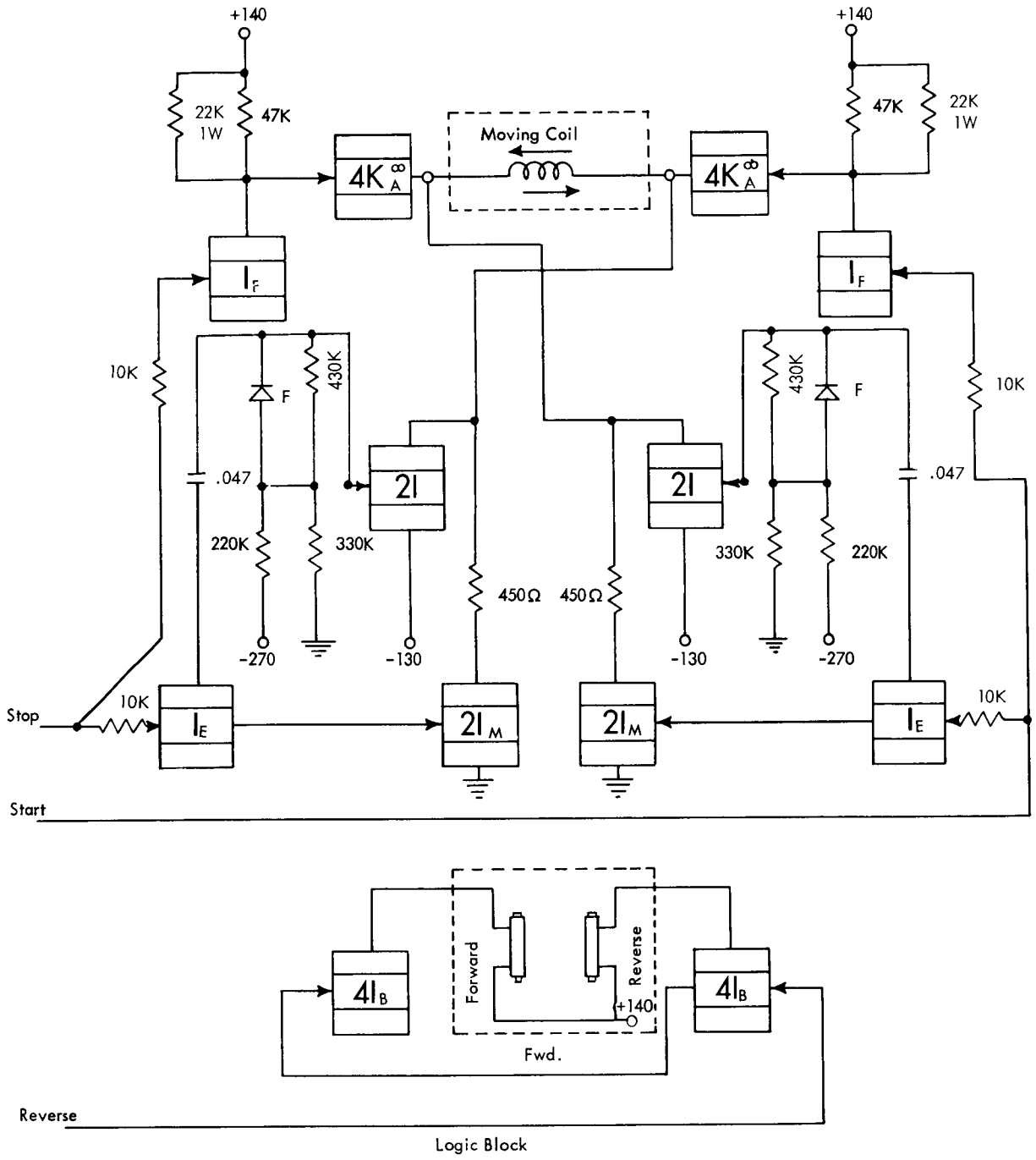


FIGURE C6. MOVING COIL AND FORWARD-REVERSE DRIVERS -- I_M, I_E, I_F, I_B, K_A

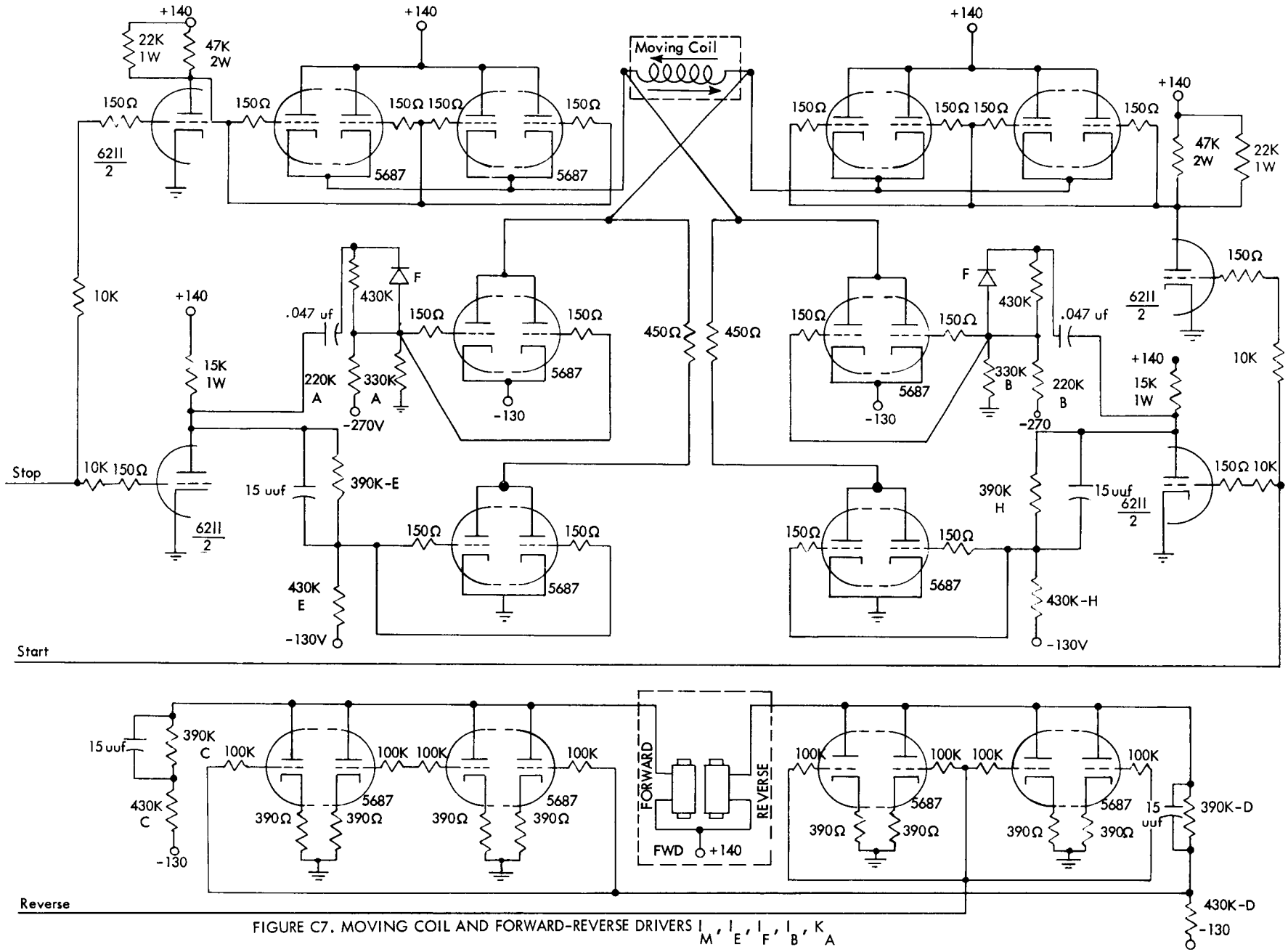


FIGURE C7. MOVING COIL AND FORWARD-REVERSE DRIVERS I_M, I_E, I_F, I_B, K_A

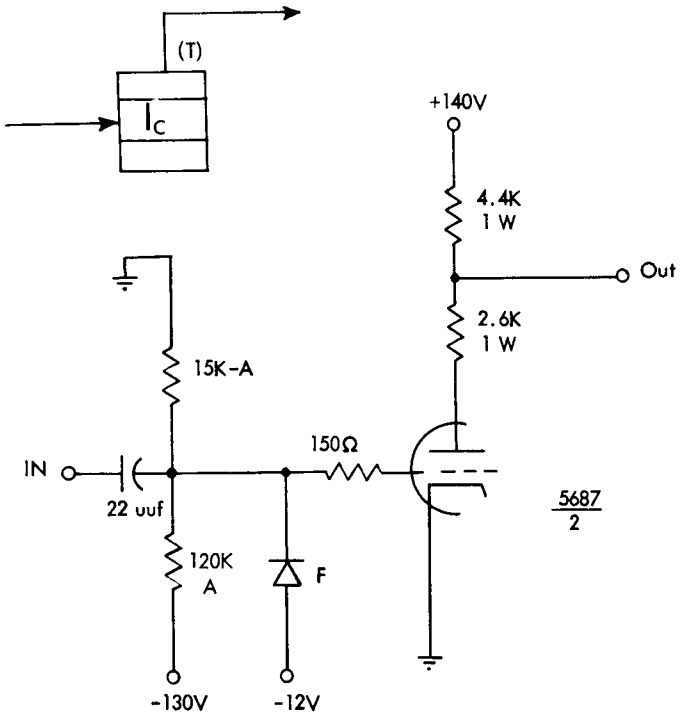


FIGURE C8. CLOCK DRIVE PULSE INVERTER -- I_C

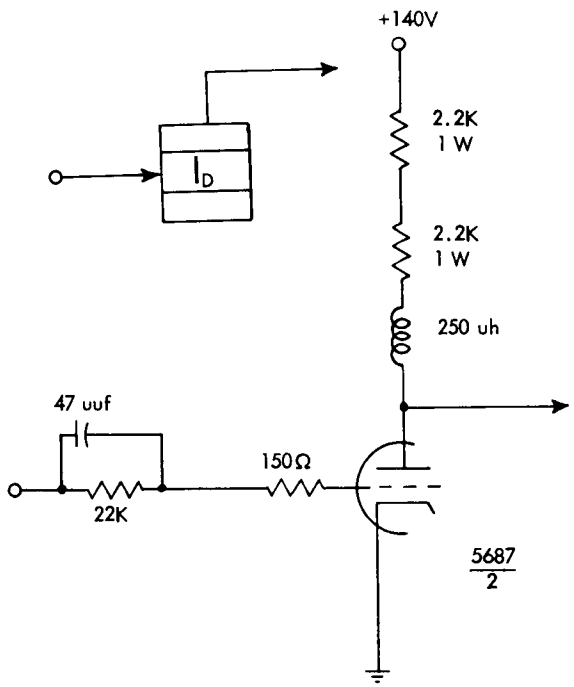


FIGURE C9. INVERTER (DRUM) -- I_D

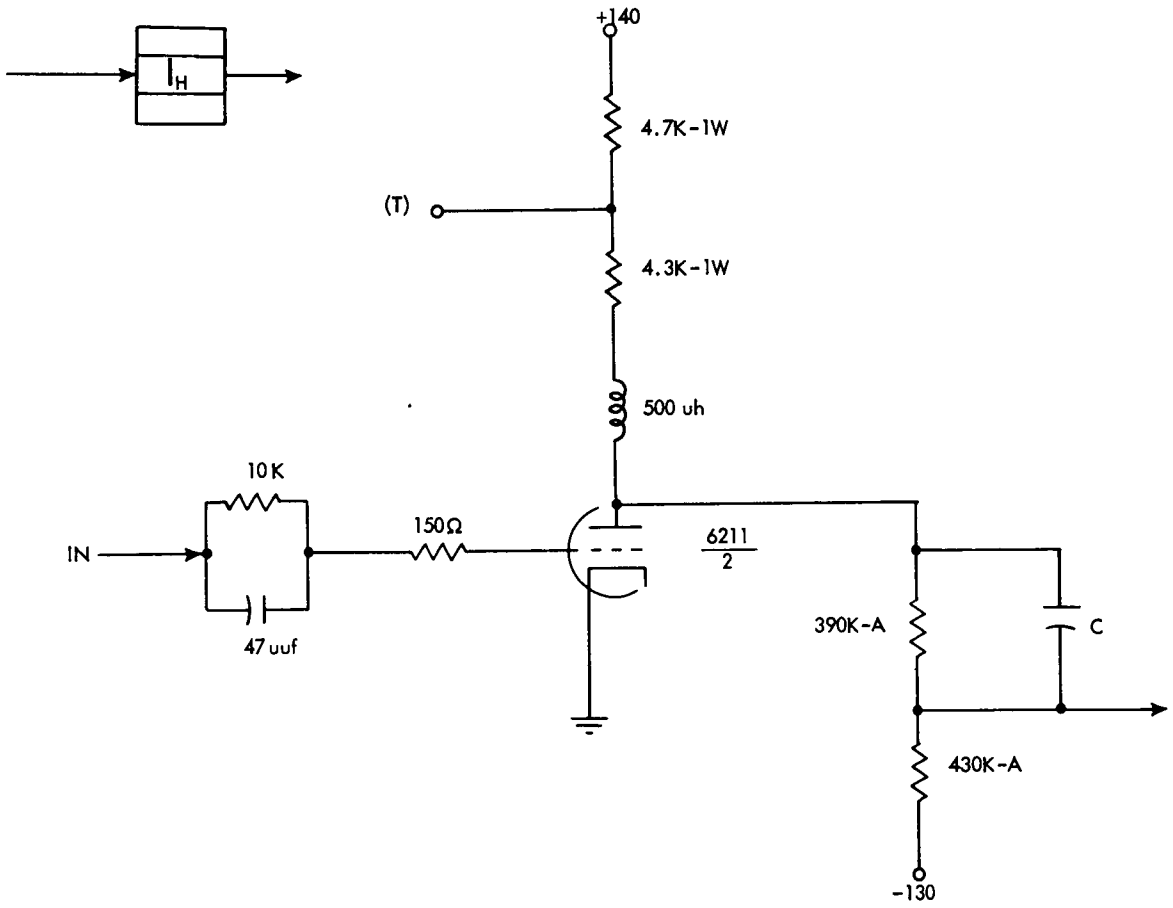


FIGURE C10. INVERTER -- I_H

short time after the input pulse. This AC-coupled inverter I_M then ceases to conduct because the grid is held at -162v. On the other hand, the DC-coupled I_M provides a path for the moving coil current as long as the driving I_E remains cut-off. This system provides the necessary amount of current to move the coil rapidly at the start (200 ma for 12 ms) and then only the amount necessary to hold it in place thereafter (60 ma).

The backward-forward mechanism consists of a magnet assembly that causes the moving coil linkage to force the tape against either the forward or reverse drive capstan. The status of the reverse line selects the group of I_B's that will conduct. With the reverse line down (-30 volts), the right group of inverters is cut off and the divider that feeds the left inverter grids is at +10 volts. The left inverters are in full conduction (20 ma each) and the forward coil is energized.

The reverse line, up at +10v, causes the right group of inverters to conduct. The divider feeding the left group is at -30v and only the reverse coil is energized.

2.01.04 Clock Drive Pulse Inverter (I_C)

The clock drive pulse inverter I_C (Figure C8) is used to invert and set the level of the clock drive pulses. The input to the I_C has a time constant comparable to that of the period of the incoming signal, and thus serves merely to set the level of the grid in the quiescent state and to couple the incoming signal. The input is a positive-going, 70v spike, while the output is a negative-going, 45v spike. The input repetition rate is one megacycle.

In the quiescent state, the tube would be cut off with minus 12 volts on the grid and the cathode grounded. When the input pulses arrive, they drive the grid up to ground and the tube conducts, with a plate current of approximately 14 ma. The plate voltage drops from +140 volts to +95 volts. An I_{C1} uses a 6350 tube.

2.01.05 Inverter (Drum) (I_D)

The inverter I_D (Figure C9) appears in the drum where it drives the peaker PKR_V (section 2.01.27, Book C) that generates the write voltages. The I_D is used rather then the standard inverter I to make use of available half tubes (5687's). In operation, the I_D is the same as the standard inverter I. The output used is full plate without a divider. The output voltage is a negative 100v shift as the plate drops from +140 to +40v.

2.01.06 Inverter (I_H)

The inverter I_H (Figure C10) is a standard inverter with an increased plate load to produce a larger voltage swing at the plate. The larger voltage swing produces a nominal divider output swing of +10 volts to -34 volts with a rise time of 0.3 usec.

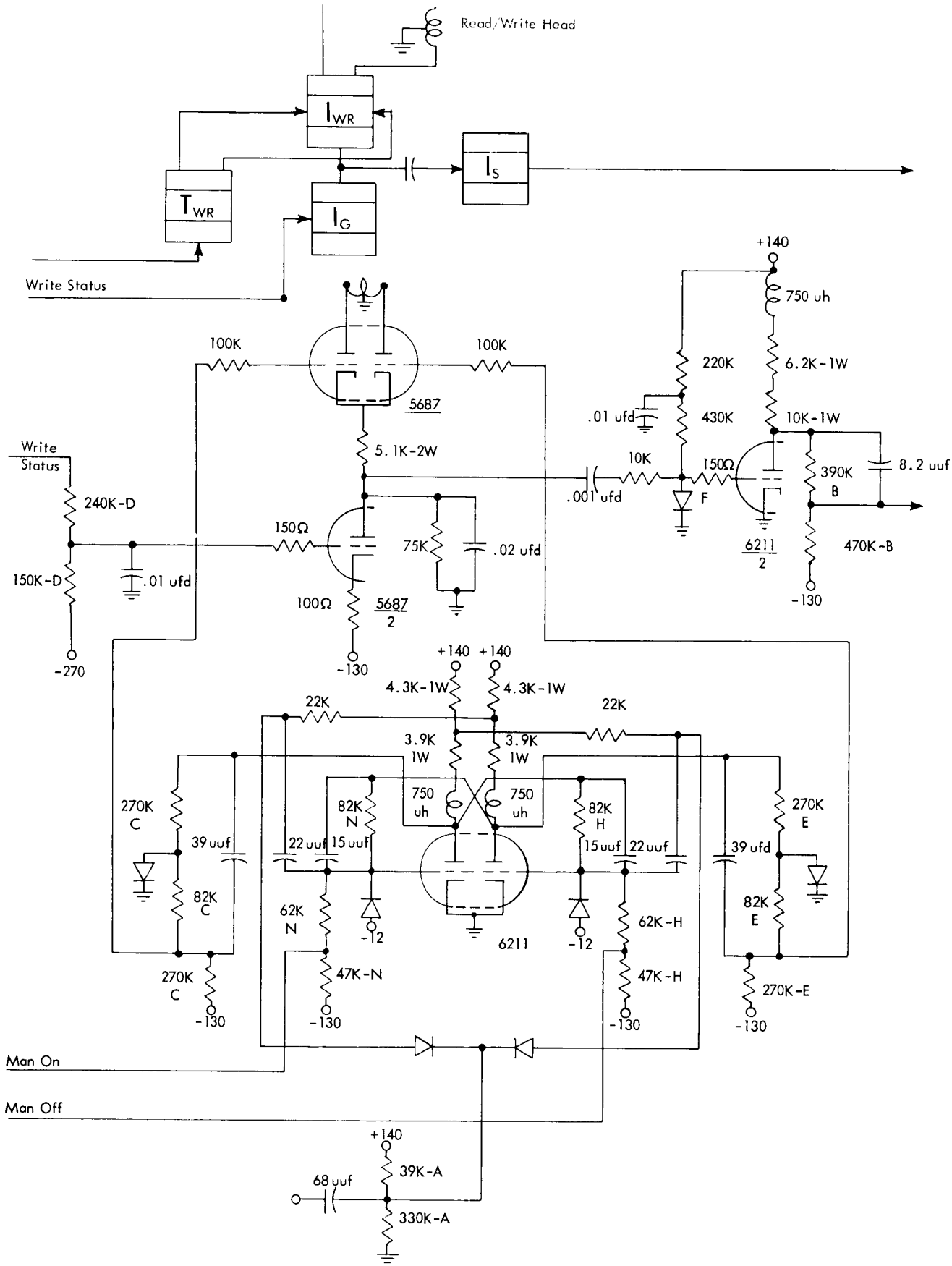


FIGURE C11. WRITE CIRCUITS -- T_{WR}, I_{WR}, I_G, I_S

2.01.07 Tape Write Circuit (T_{WR}, I_{WR}, I_G, I_S)

The tape write circuit T_{WR}, I_{WR}, I_G, I_S is used in the tape drive unit to provide controlled current to the write coil. Current through the write coil in one direction or the other provides the change in flux that is necessary to write on tape. This method is the NRZI system.

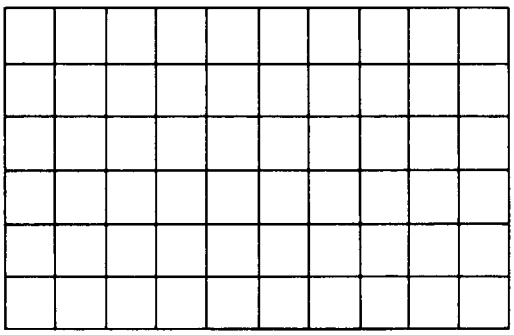
Circuit Description. The T_{WR} is a standard trigger with non-standard outputs (Figure C11). The self-gated binary input allows each negative input shift to change the trigger status. The input to the T_{WR} is a diode gate that samples the write bus every 67.2 usec. The fall of this pulse triggers the T_{WR}. The output levels of the T_{WR} are -30 volts and -52 volts, depending on the trigger status. The clamping diode in the output divider circuit prevents that junction point of the divider from rising above ground, thus setting the upper level of -30 volts.

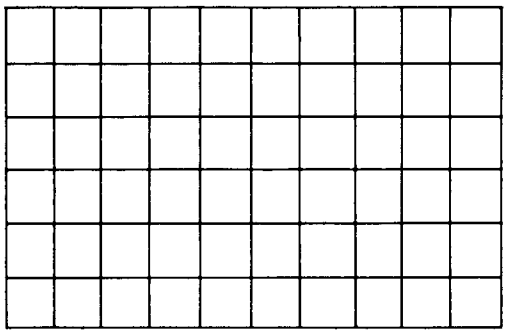
The I_G is used as an electronic switch to allow conduction through the I_{WR} only when write status is up. Write status down (+50 volts) sets the input to the I_G at -147 volts and the tube is cut off; write status up (+138 volts) sets the I_G input at -113 volts and the tube is able to conduct. The I_G, conducting, produces a -40v cathode voltage for the I_{WR}. With the I_G not conducting, both the plate and cathode of the I_{WR} are at ground level and no conduction through the write coil is possible. The 75K resistor to ground prevents the I_{WR} cathode and the I_G plate from floating. Thus, the I_G conditions the I_{WR} for conduction, dependent, of course, upon the input to the I_{WR}.

The T_{WR} outputs feed both sides of the I_{WR}. If one T_{WR} output is at -30 volts, then the other is at -52 volts. Thus, one side of the I_{WR} is able to conduct while the other side is cut off (I_{WR} cathode at -40 volts). As long as the I_G is conducting and setting the I_{WR} cathode at -40 volts, all changes in the status of the T_{WR} are reflected as changes in direction of the current flow through the write coil. When the current flow through the write coil changes direction, a character is written on tape.

Because of the heavy inductive load (the write coil), the I_{WR} cannot switch conduction from one side to the other as fast as the T_{WR} flips. The I_{WR} cuts off for several microseconds because cutting off of the induced voltage from one side lowers the opposite plate voltage sufficiently to prevent conduction even with the grid going up. The I_{WR} cathode, therefore, reflects this delay as a 17v minus shift during T_{WR} flip time. The negative shift is coupled to the grid of the I_S. The I_S cuts off for about 8-12 usec and the output pulse (echo pulse) is used for redundancy checking.

2.01.08 Unassigned





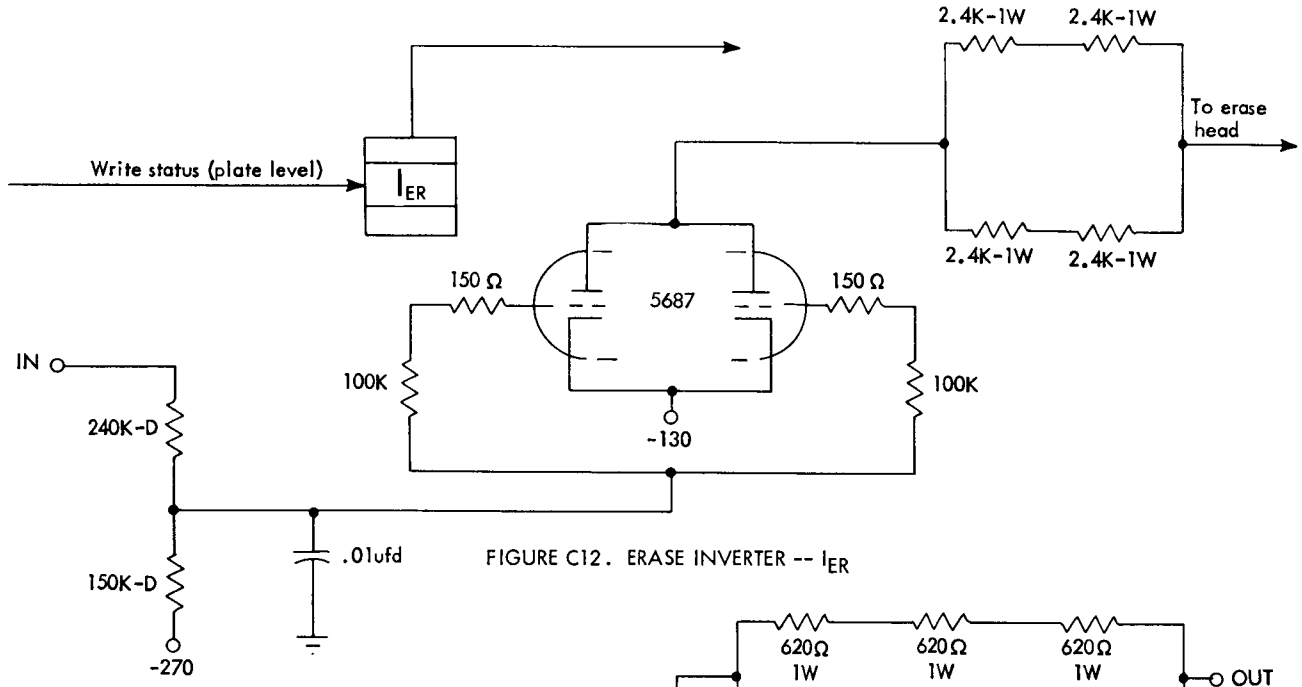


FIGURE C12. ERASE INVERTER -- I_{ER}

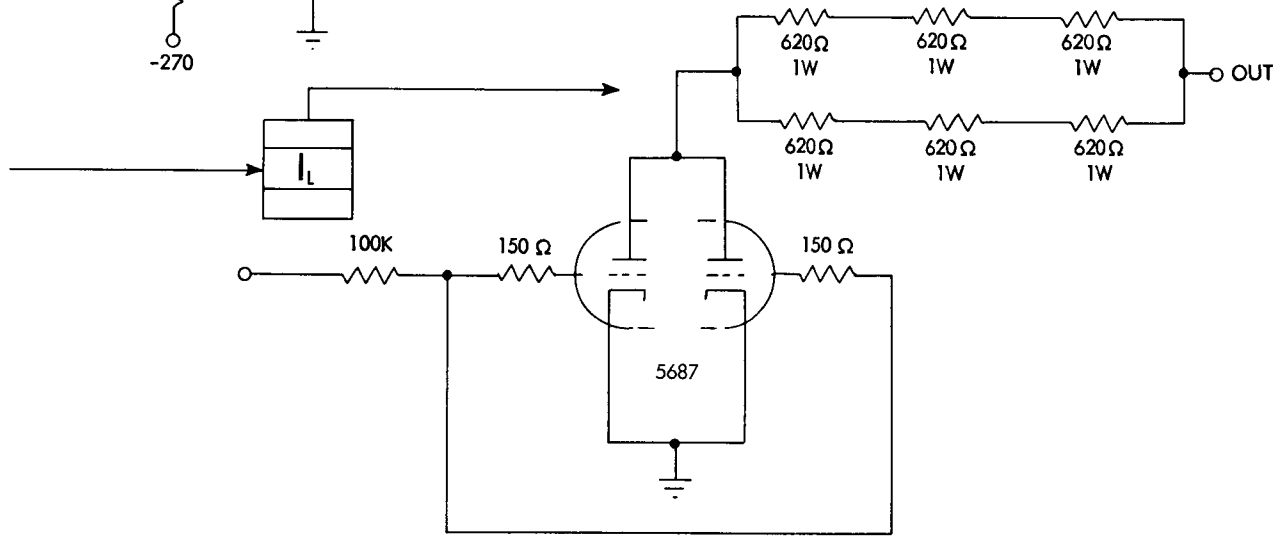
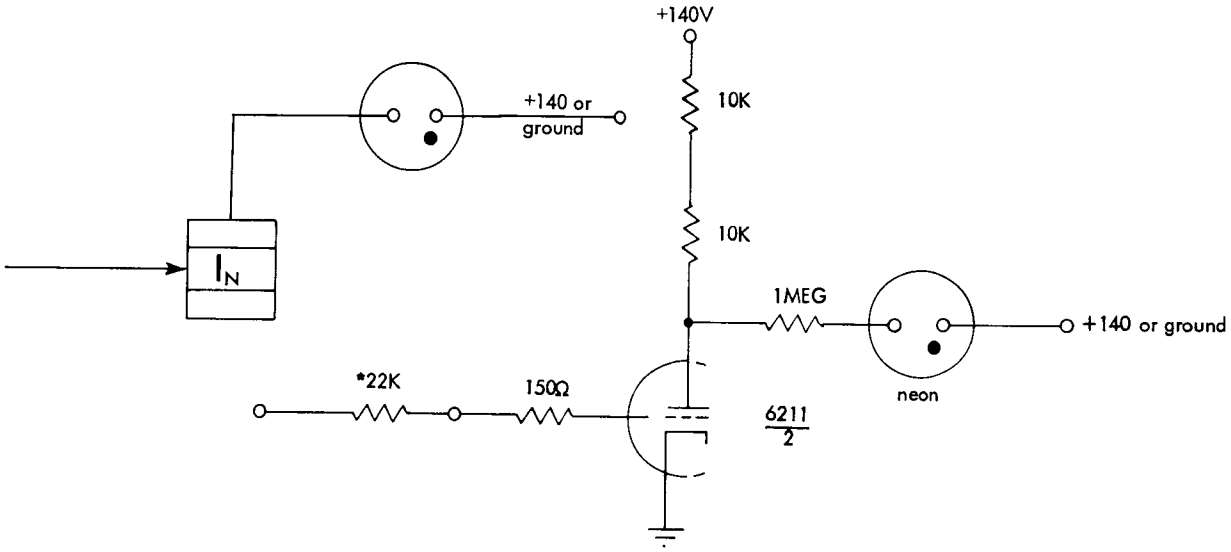


FIGURE C13. INVERTER (LIGHT) -- I_L



*22K grid current limiter to be used when driving source is low impedance

FIGURE C14. INVERTER (NEON) -- I_N

2.01.09 Tape Erase Circuit (I_{ER})

The inverter I_{ER} is used in the tape drive unit as a current switch for the erase head (Figure C12). During write operation, the tape is erased before it reaches the read/write head

"Write status" is plate level, +138v to +50v nominal. When this line is down, the midpoint of the divider is at -157 volts and the I_{ER} is cut off. When "write status" is up, during writing, the divider provides -130 volts to the I_{ER} grids. The I_{ER} goes into full conduction and 33 ma are fed through the erase coil to ground. While erasing, there is a 17v drop across the erase coil and the I_{ER} plate voltage is about -80 volts.

2.01.10 Inverter (Light) (I_L)

The inverter (light) I_L (Figure C13) is used in various places in the system to turn on 55v indicator lamps. The lamp makes up somewhat more than one half of the inverter load. The lamp will draw somewhere between 40 to 65 ma of current; therefore, a full 5687 is needed in parallel to supply this current.

2.01.11 Pull-Over Buffer Inverter (I_{PB})

This component is assigned to the 776 and 760 Record Storage Unit only, and is found in Book D, Section 3.05.00.

2.01.12 Inverter Neon (I_N) (I_{NK})

The inverter neon I_N (Figure C14) is used to supply the proper voltage to operate a neon lamp. The circuit may operate one of two ways. If the neon is to be lit when the input is up, the neon will be returned to +140 volts. If the neon is to be lit when the input is down, the neon will be returned to ground. When the I_L conducts, it draws approximately 5 ma and the plate voltage is about +35 volts. This voltage is not enough to light the neon if it is returned to ground, but is enough to light the neon if it is returned to +140 volts. On the other hand, when the tube is cut off and its plate is at +140 volts, a neon returned to +140 volts does not light while one returned to ground does light.

When the driving source to the I_N is low impedance, the 22K grid current limiting resistor is placed in series with the 150-ohm parasitic suppressor. An I_{NK} is the same circuit but uses one half of a 5965 tube.

2.01.13 Pull-Over Inverter (I_{PS})

The pull-over inverter I_{PS} (Figure C15) is one of several inverters used to pull over triggers or single shots. The tube is initially cut off (bias of -15 volts). The capacitor allows only a short period of conduction when a positive pulse is applied.

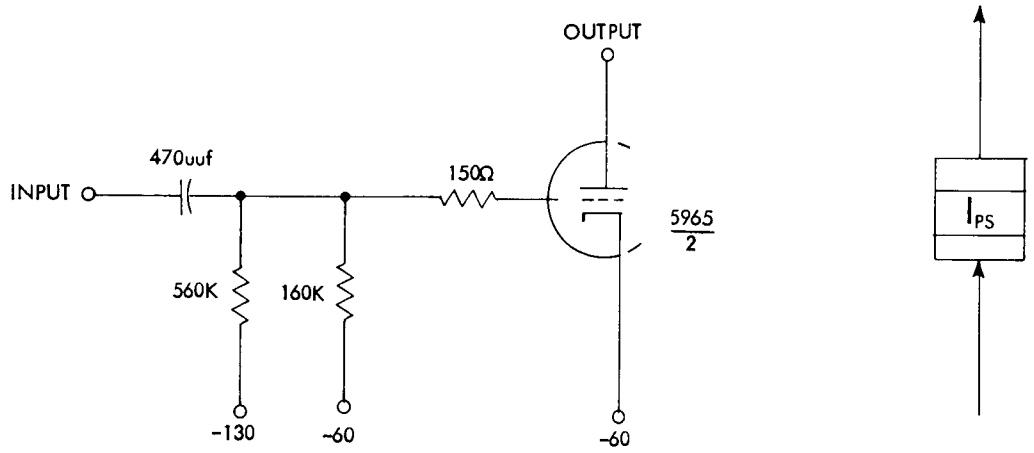


FIGURE C15. INVERTER (PULLOVER) -- I_{PS}

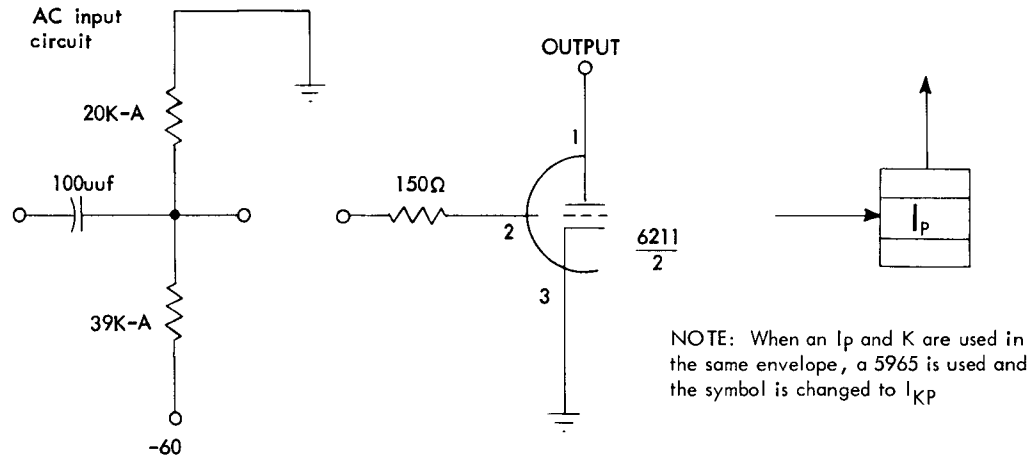


FIGURE C16. INVERTER (PULLOVER) -- I_P

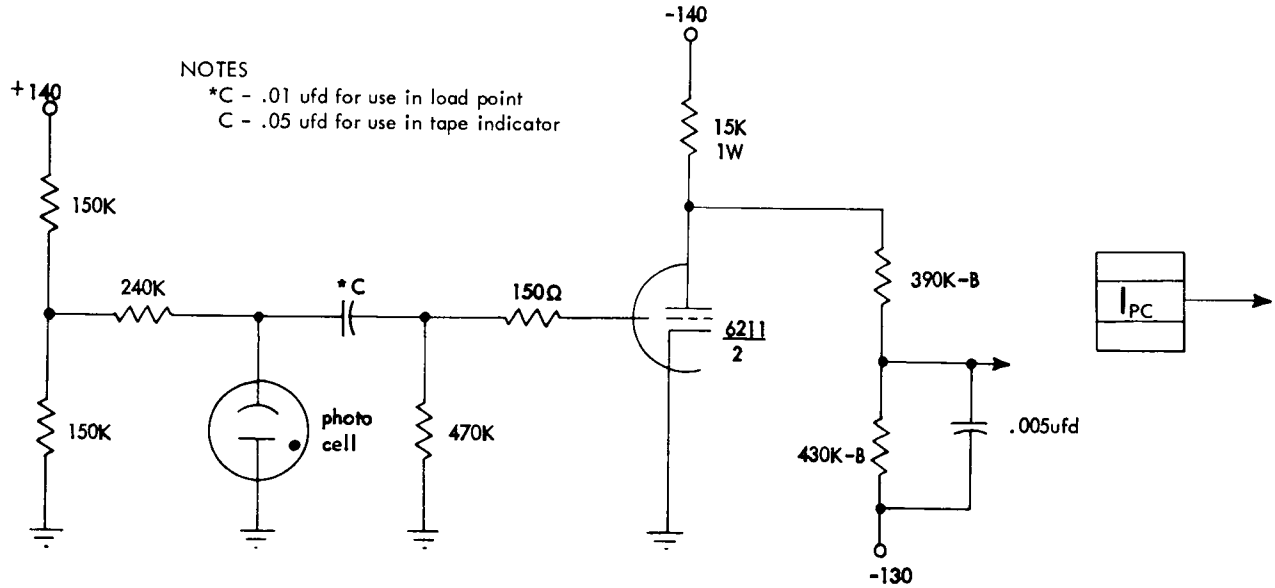


FIGURE C17. INVERTER (PHOTO PICKUP) -- I_{PC}

2.01.14 Inverter (Pull-Over) (I_P)

The inverter (pull-over) I_P (Figure C16) is one of the several pull-over inverters used in the system. Pull-over inverters share a plate load with the circuit that they pull over.

The I_P is cut off in its quiescent state, since the input divider sets the grid level at approximately -20 volts. When a positive shift is applied to the input of the I_P, it conducts and draws plate current through the common load resistor. The I_P is used to pull over the single shot SS_M (section 2.03.04, Book C). In this case, the negative shift at the left plate of the SS_M is transmitted to the right grid of the SS_M through the coupling capacitor, thus cutting off the right side.

The I_P, SS_M, combination appears in the card stations where the I_P input is the output of a buffer amplifier. The output of the buffer amplifier is a +48v spike of one microsecond duration. This one-microsecond, 48v spike causes the I_P to conduct, pulling over the SS_M. These one-microsecond pulses disappear before the SS_M cycles off its six microsecond duration.

2.01.15 Inverter (Photo Pickup) (I_{PC})

The photo pickup inverter I_{PC} (Figure C17) is used in the 727 Magnetic Tape Unit to indicate the load point and the presence of a tape indicator or a break in tape. The output of the I_{PC} causes a relay to be picked. Operation of the circuit is described below.

The photo cell used in the I_{PC} is the photo-conductive type. This type of photo cell exhibits different resistances when illuminated and when unilluminated. These resistances are referred to as the light and dark resistances. The photo cell has a dark resistance of about 300K. In its quiescent state, the tube is in full conduction. The voltage at the centerpoint of the input divider is about +70 volts and the voltage drop across the photo cell is about 34 volts (unilluminated). When the photo cell is illuminated, the potential across it drops to 24v. This -10v shift is coupled to the grid of the inverter, cutting the tube off. Because the coupling network at the input to the inverter itself has a long time constant, and a rise or change in voltage across the photo cell is relatively slow, the output of the inverter has a slow rise and fall time (one usec). The output of the inverter (+10 volts to -30 volts) is tied to a relay driver circuit to pick up a relay. A .005 ufd capacitor is placed across the lower resistor of the divider output to eliminate noise caused by variation in the input.

When the light to illuminate the photo cell is properly adjusted (727 Magnetic Tape Unit, "Adjustments"), a photo cell of this type exhibits a change in voltage of about 14 volts when illuminated from its dark state voltage. Because the difference between the dark and the light resistance of particular photo cells may vary considerably, the drops across the photo cells also vary considerably. The photo cell is rejected if the voltage shift across it, when illuminated, is not in the range from 8 to 20 volts.

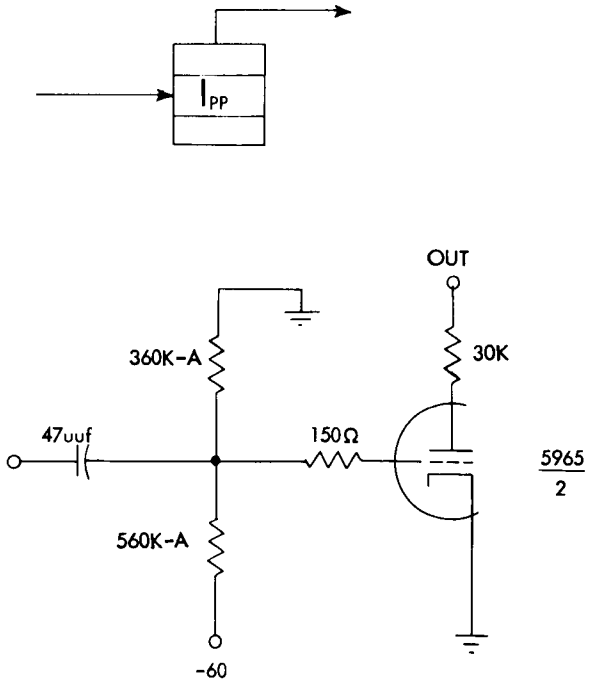


FIGURE C18. INVERTER (TRIGGER PULLOVER) -- I_{PP}

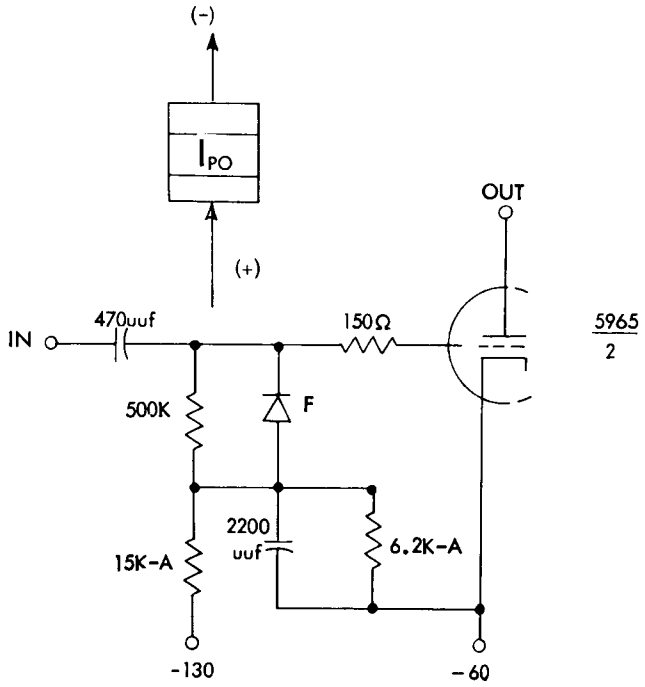


FIGURE C19. INVERTER (SS_D PULLOVER) -- I_{PO}

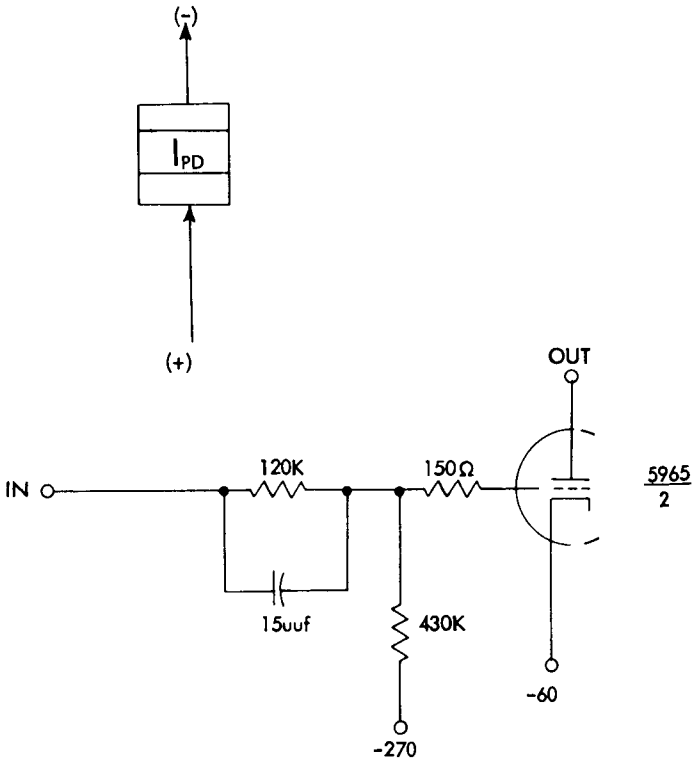


FIGURE C20. INVERTER (SS_D PULLOVER) -- I_{PD}

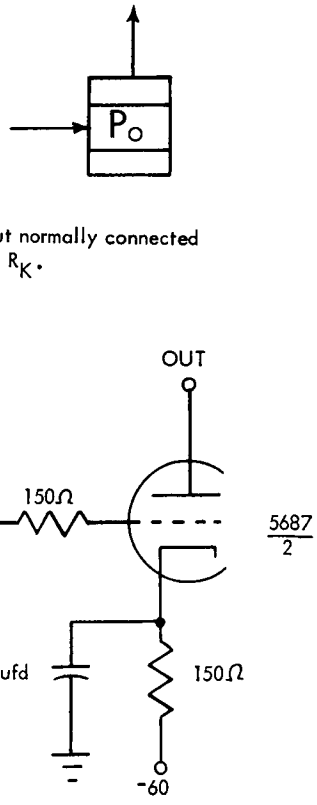


FIGURE C21. LINE CAPACITY YANKER -- P_O

2.01.16 Trigger Pull-Over Inverter (I_{PP})

The trigger pull-over inverter (Ipp) (Figure C18) is used in the card reader to pull over triggers. The input pulses to the Ipp are from the reader buffer amplifier BA_R (section 2.04.15, Book C). In its quiescent state, the I_{PP} is cut off. The grid is at -23 volts because of the divider at its input. The plate of the I_{PP} is returned to the plate of the T through a 30K resistor. The purpose of this 30K resistor is to limit the shift when the I_{PP} conducts. This prevents overshoot at the grid of the T because of the heavily conducting Ipp. The input pulses from BA_R are approximately 50v in amplitude and one microsecond in duration. The pulses cause the I_{PP} to conduct, pulling over the trigger.

2.01.17 Pulse Forming Inverter (I_{PF})

The pulse forming inverter I_{PF} is described under "Standard Circuits," section 2.12.00, Book A.

2.01.18 Pull-Over Inverter for the Hold-Over Single Shot (I_{PO})

The pull-over inverter I_{PO} (Figure C19) is used to pull over the hold-over single-shot SS_D. The input to the I_{PO} is a series of positive pulses (20 to 70 volts in amplitude and 4 to 10 percent of the duration of the single shot duration). The resistor-capacitor diode network at the input to the I_{PO} acts as a DC restorer when the input pulses cease. When the pulses cease, the input voltage drops to a level determined by the divider network at the input. The plate of the I_{PO} is returned through the 2.2 MEG resistor from the right grid of the SS_D to the +140v power supply. When the input pulses to the I_{PO} cause the grid to swing positive, the I_{PO} conducts momentarily (because of grid current and sharp drop in plate voltage) drawing plate current through the 2.2 MEG resistor in the SS_D, driving the right grid negative and cutting off the right side of the SS_D. As long as the positive shifts occur at a repetition rate higher than the duration of the SS_D, the I_{PO}, coming into conduction, continues to pull the grid of the SS_D down. The SS_D is held cut off, hence, the name pull-over inverter for the hold-over single shot. When the incoming pulses to the I_{PO} cease, the I_{PO} cuts off as the DC restorer at the input brings the grid voltage more negative than the cathode voltage (to about -80 volts). The I_{PO} cuts off, and no longer has any effect on the hold-over single-shot SS_D. The natural timing of the SS_D determines how much longer the SS_D is held over.

2.01.19 Pull-Over Inverter for the Hold-Over Single Shot (I_{PD})

The pull-over inverter I_{PD} (Figure C20) serves the same function as the I_{PO}. The main difference is that the I_{PD} has a DC input and holds over the single shot as long as the input pulse is available. The SS_D starts timing after the input pulse to the I_{PD} falls.

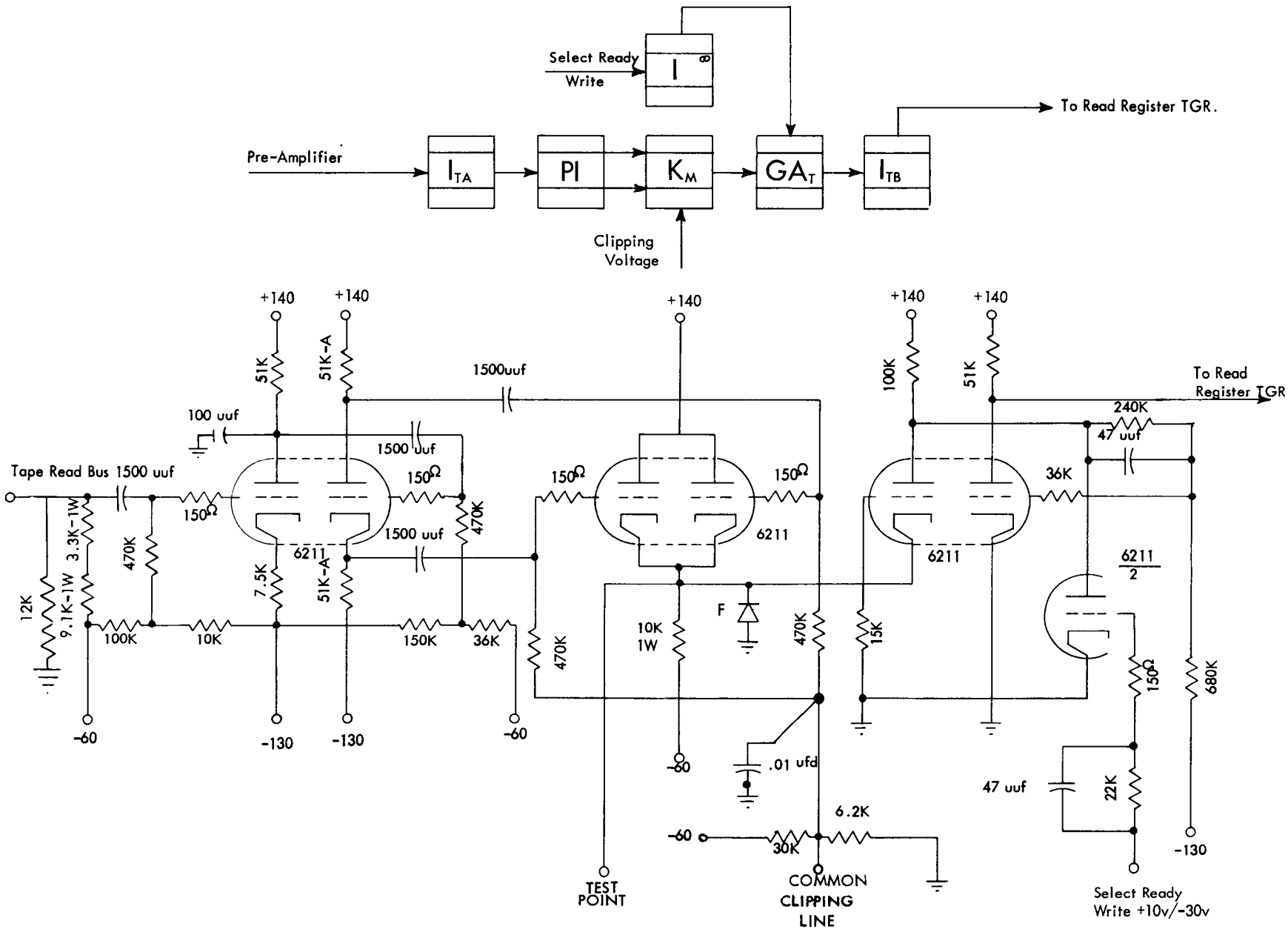


FIGURE C22. FINAL AMPLIFIER -- I_{TA}, PI, K_M, GA_T, I_{TB}

2.01.20 Tape Final Amplifier (I_{TA}, PI, K_M, GA_T, I_{TB}, I_H)

The tape final amplifier (Figure C22) consists of the inverters I_{TA} and I_{TB}, the phase inverter PI, the cathode follower mixer K_M, and the grounded grid amplifier GA_T. This circuit is in the reader, punch, and printer control units to amplify the signals from the tape unit and feed them to a register. The circuit is modified in the tape control unit to accept signals from one of two entry buses. The addition of a cathode follower mixer K_M, feeding the I_{TA}, does not materially affect the general operation discussed here. There is an individual amplifier for each bit line (seven in all).

The input to the amplifier is at one of two DC levels, +10 volts or ground as determined by a +10v or -30v input to a driving cathode follower. The input diode prevents a voltage lower than ground level. When the input to the driving cathode follower is down at -30 volts (not in read status), the output signals from the pre-amplifier cause a -20 to -40v swing at the cathode follower input. The diode (amplifier input) prevents the signals from affecting the rest of the amplifier circuit. However, when the input to the driving cathode follower is at +10 volts (conditioned to read), the signals from the pre-amplifier cause voltage variations of +20 volts to ground to hit the amplifier circuit. These variations are in the form of positive and negative spikes and are coupled to the I_{TA} where they are inverted and level set. The I_{TA}, in its quiescent state, is conducting and the 20v variations at the input cause the plate voltage to swing 40 volts above and below the steady DC plate level.

The 40v variations are applied to the phase inverter PI. When the grid goes positive, the plate goes negative and the cathode goes positive. When the grid goes negative, the plate goes positive and the cathode goes negative. Thus, there is a positive output, either at the plate or cathode for any change at the input to the phase inverter. The cathode is fed to one grid of the mixer, K_M, while the plate is fed to the other grid of the mixer. Because one of these grids is positive-going while the other grid is going negative, the positive-going grid brings up the cathode level and the other half of the tube cuts off. This means that the mixer cathode rises whenever there is a voltage variation applied to one of the grids. The net result is that all changes at the amplifier input appear as positive peaks at the output of the K_M. Because the K_M output is clamped to ground, the output variations are from ground up.

The positive spikes are applied to the normally conducting GA_T. The rising cathode voltage cuts the GA_T off and the plate rises. The GA_T stays cut off until the cathode falls and thus produces a square wave output. These output pulses are inverted by the I_{TB} and fed to the grid of a register trigger.

The GA_T has another input. An inverter shares the GA_T plate load. Whenever this inverter is told to conduct (+10 volts), the plate of the GA_T is held down and the GA_T is inoperative. The amplifier can thus be deconditioned for as long as necessary (read delay being the time necessary for the tape to get to proper operating speed befor reading). The common clipping line input to the K_M sets the bias level on the K_M.

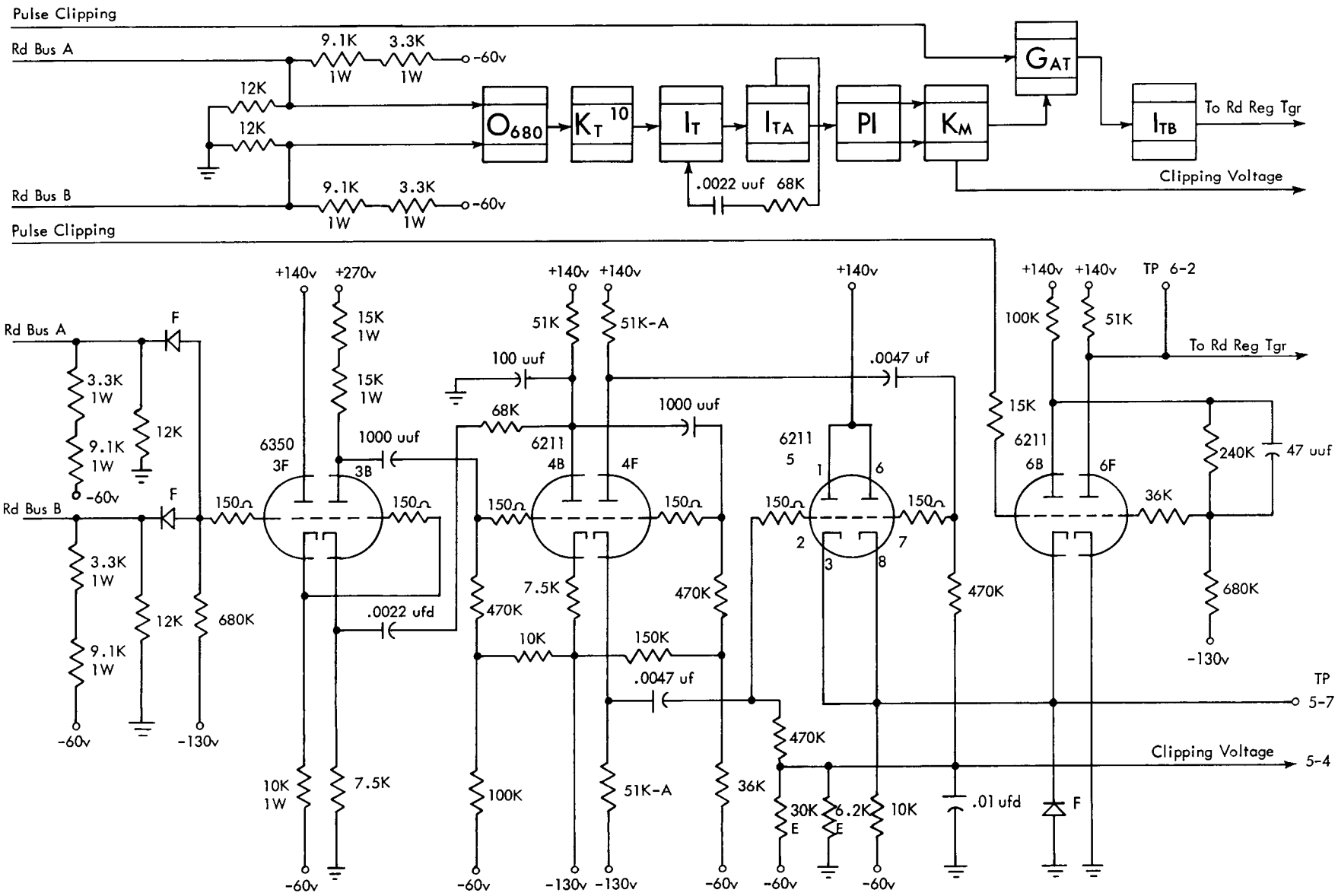


FIGURE C23. 754 FINAL AMPLIFIER O, K_T, I_T, I_{TA}, PI, K_M, GA_T, I_{TB}

2.01.21 754 Final Amplifier (O, K_T, I_T, I_{TA}, PI, K_M, GA_T, I_{TB})

The 754 Final Amplifier (Figure C23) is similar in operation to the Final Amplifier (section 2.01.20, Book C).

Input to the amplifier is from Read Bus A or B through the OR circuit to the K_T for powering. The pulses are shaped in the I_T and I_{TA} with the aid of the feedback circuit.

The pulse clipping line is brought up during character gate to increase sensitivity after the first bit.

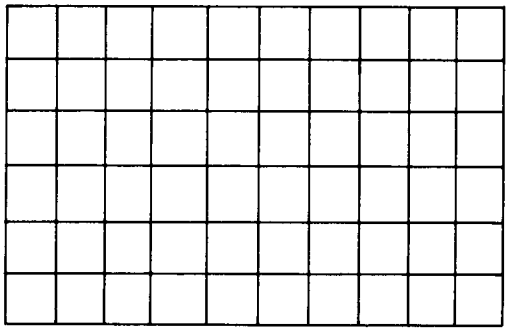
2.01.22 777 Final Amplifier (I_{TA}, PI, K_{M2}, GA_T, I_{TB}, I_H)

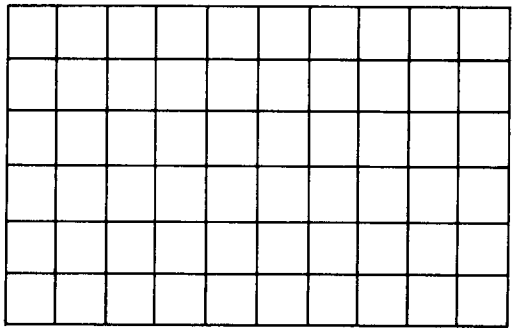
This component is assigned to the 777 Tape Record Coordinator (section 5.01.01, Book D). For circuit description see section 2.01.20, Book C.

2.01.23 Line Capacity Yanker (P_O)

The line capacity yanker (Figure C21), as its name implies, is used to pull or yank down a high-capacity line such as the write bus in the tape control unit. The circuit is a low impedance source that can supply the high current necessary to discharge line capacitance rapidly The same input that feeds the cathode follower powering the line is inverted and AC-coupled through another cathode follower to the P_O. As the input to the powering cathode follower goes down to -30 volts, the voltage level of the output should also fall. The inverted -30 volts (+10 volts) tells the P_O to conduct momentarily (AC-coupled) and the resultant plate current discharges the line capacitance. The input to the powering cathode follower at +10 volts is inverted (-30 volts) to cut off the P_O until it is again needed to help to bring down the bus. The P_O output is normally connected across the cathode resistor of the powering cathode follower.

2.01.24 Unassigned





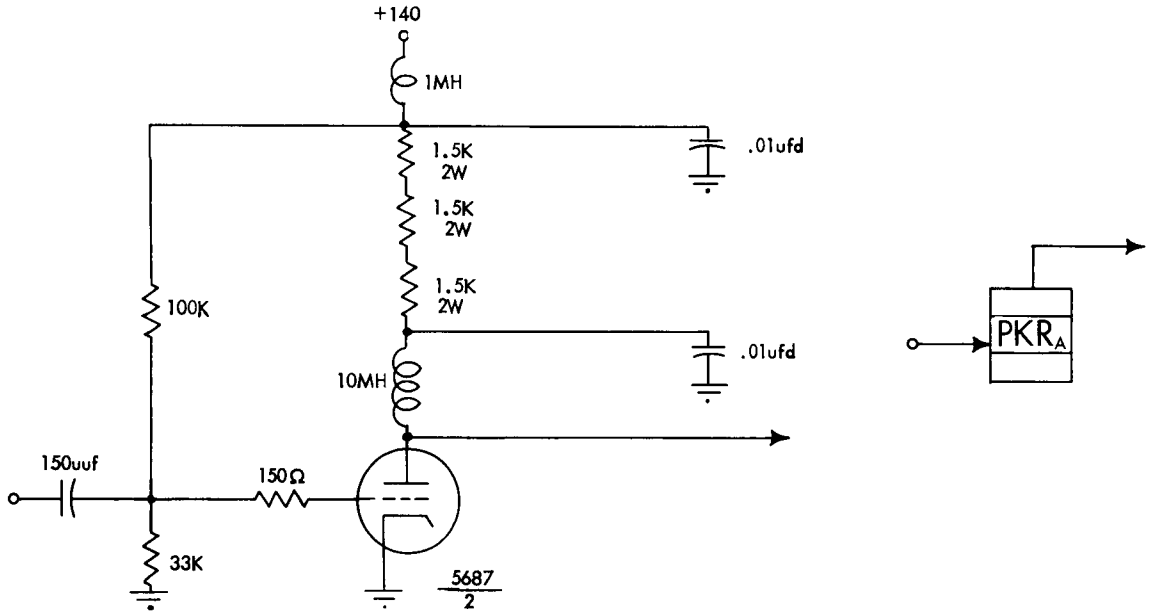


FIGURE C24. PEAKER (WRITE AMPLIFIER -- DRUM) -- PKR$_A$

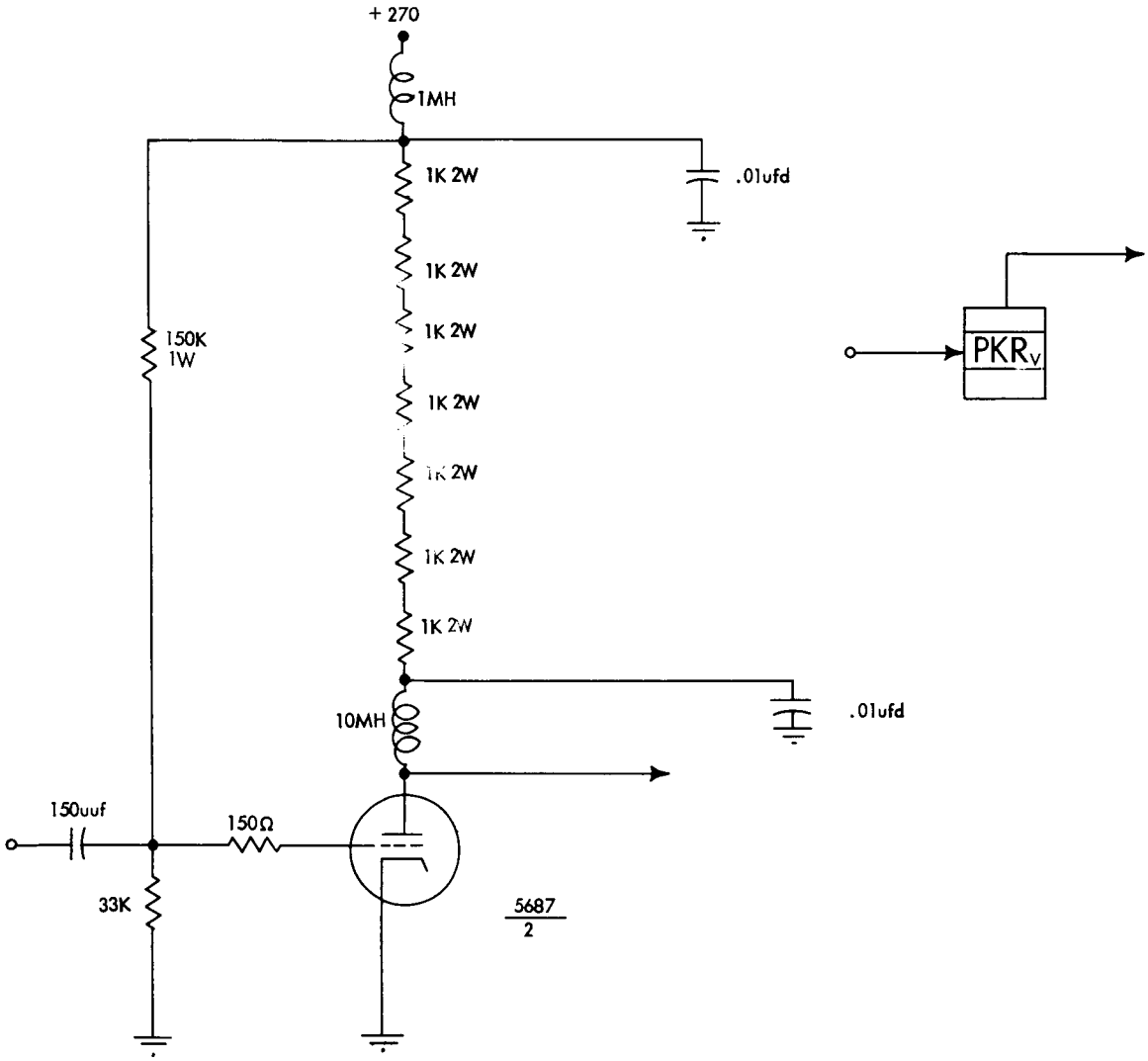


FIGURE C25. PEAKER (WRITE VOLTAGE -- DRUM) -- PKR$_V$

Peaker (PKR)

The principles of peaker operation are described in section 2.15.00, Book A.

2.01.25 Peaker (Write Amplifier--Drum) (PKR_A)

The peaker PKR_A (Figure C24) is used in the drum to generate one of the pulses used in writing. (Writing is accomplished by coincident current of peaker PKR_A and PKR_V). The input to the PKR_A is from the tap of a standard inverter. The output of the PKR_A is fed to a cathode follower K_D. The K_D itself, when used with a PKR_A, has a +140v plate supply.

In its quiescent state, the grid draws 1.4 ma of grid current. The tube in this state draws 26 ma. As the general section on the peaker explains, the plate voltage rises above the supply voltage when the tube is cut off. With the plate drawing 26 ma, the output is around 25 volts; it swings up to +150 volts as the tube is cut off. This is a total swing of 125 volts.

The clamping diodes, mentioned in the general section on peakers, are not necessary with a PKR_A because the tube itself seems to provide sufficient damping to prevent objectionable overshoot. The PKR_A has a pulse width of two usec at 50 percent amplitude.

2.01.26 Memory Peaker (PKR_B)

This component was assigned to 702 electrostatic memory and is not used now.

2.01.27 Peaker (Write Voltage--Drum) (PKR_V)

The peaker PKR_V (Figure C25) is used in the drum to generate one of the pulses used in writing (section 2.01.25, Book C). The input to the PKR_V is from the inverter I_D (section 2.01.05, Book C). The negative 60v shift from the I_D cuts the tube off and causes the output to swing from +25 volts to +170 volts. The output of the PKR_V is fed to a cathode follower K_D having a +270v plate supply. As with the PKR_A, it is unnecessary to use clamping diodes at the output. See general peaker circuit operation. The PKR_V has a pulse width of two usec at 50 percent amplitude.

2.01.28 High Capacity Pull-Down Circuit (I_Z)

This component is assigned to the 767 Data Synchronizer and the 777 Tape Record Coordinator (section 5.01.02, Book D).

2.01.29 Wave Form Generator Peaker (PKR_Z)

The wave form generator peaker PKR_Z is covered under "Standard Circuits," section 2.15.02, Book A.

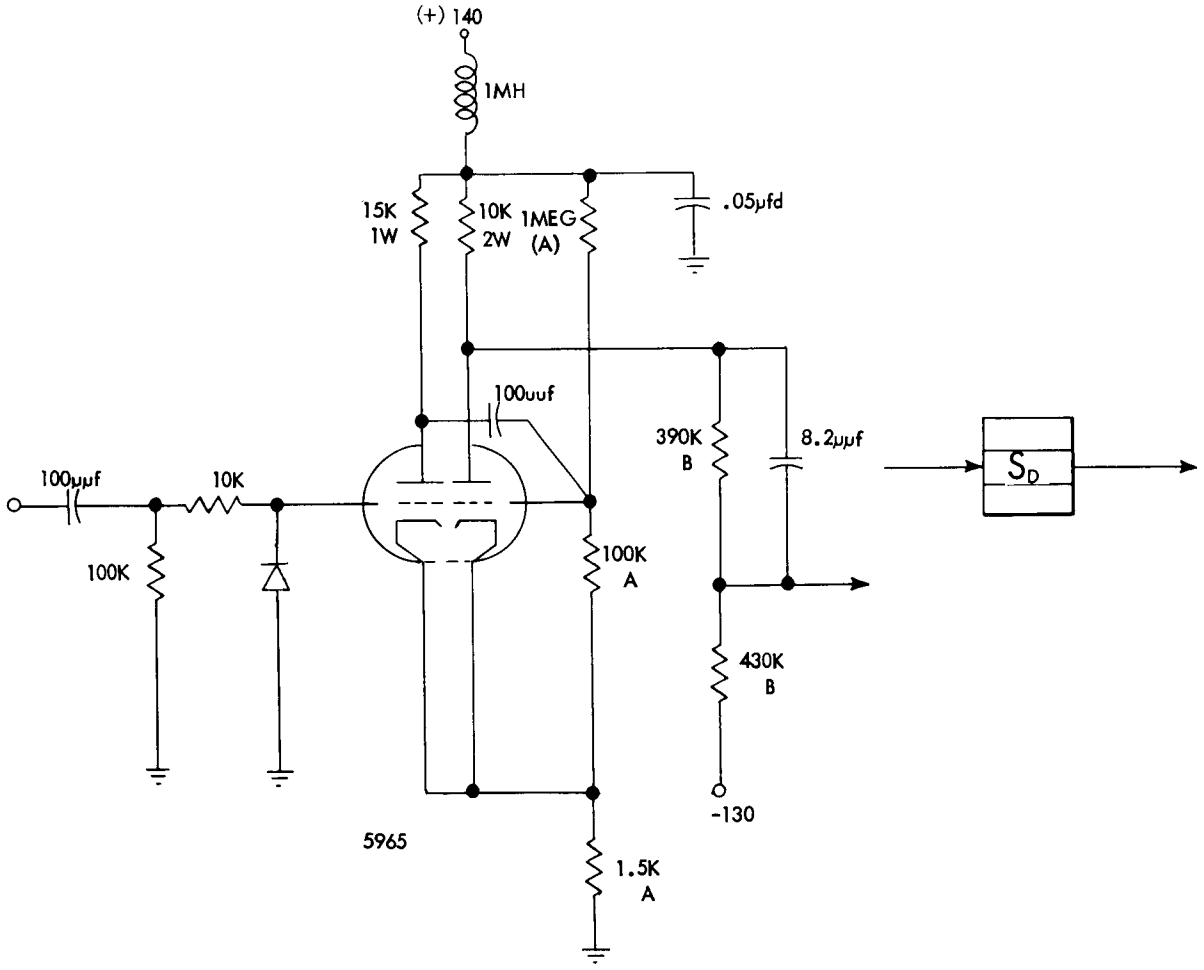


FIGURE C26. SHAPER (DRUM) -- S_D

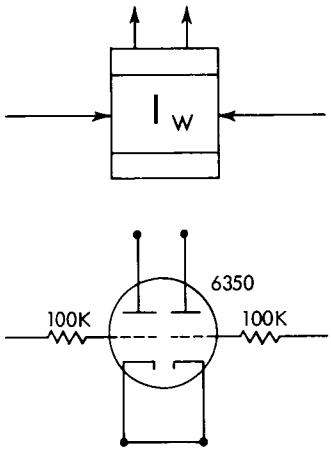


FIGURE C26A. WRITE INVERTER -- I_W

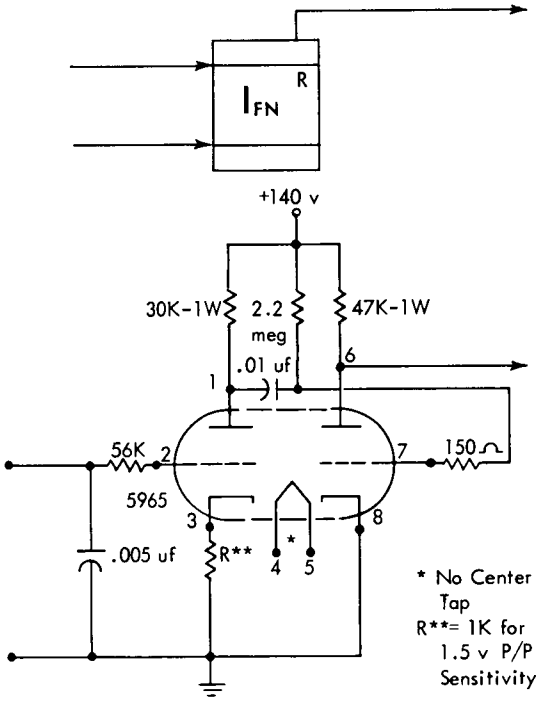


FIGURE C26B. OPEN FILAMENT NEON DRIVER -- I_{FN}

2.01.30 Shaper (Drum) S_D

The shaper (drum) (Figure C26) is used to shape the output pulses from the amplifiers in the drum, the amplifier drum (timing) and the amplifier drum (common). Consider the circuit operation with the input down.

The right tube is conducting with the right grid drawing about 0.12 ma grid current. The cathode potential is +12.2 volts because of the right plate current through the 1.5K cathode resistor. The left grid is down at ground or below, because of either lack of a signal or a negative signal from the amplifier; the left tube is cut off. The right plate is down to around +58 volts, and the divider output is -30 volts.

Although the left grid is AC-coupled, the time constant of the input circuit is so long (10 microseconds), compared to the length of the incoming pulse, that it may be considered as DC-coupled. The circuit flips on when the input grid reaches cut-off and flips back again when the input drops back. When the potential on the left grid rises toward that of the cathode, the left tube begins to conduct. The fall in plate voltage is coupled to the right grid and cuts the right tube off. The rise in voltage on the right plate (to approximately +140 volts) gives a divider output of +10 volts.

When the input voltage drops back down again, the left tube is cut off, and the rise in its plate voltage brings up the right grid, which brings down the right plate. The divider output drops back down to -30 volts. The circuit is completely recovered in three to four microseconds. The output of the S_D is fed to a cathode follower Kx. The coil and capacitor (0.05 ufd) isolate plate voltage variations from the power supply.

2.01.31 Unblank Driver UD

This component was assigned to 702 electrostatic memory and is not used now.

2.01.32 Write Inverter (I_W)

The I_W (Figure C26A) is used in the 729 I Magnetic Tape Unit. The circuit is driven by a standard trigger (T) coupled to the grids through 100K resistors. The plates are connected to the read-head windings on each side of the common. The cathode is grounded. A 6350 tube is used.

2.01.33 Open-Filament Neon Inverter (I_{FN})

The I_{FN} (Figure C26B) is used to drive the open-filament neon indicators. In the quiescent state, the input from the secondary of the open-filament detection transformer is at zero volts. The left half of the tube is conducting with the plate at about 90 volts. The right half is conducting with the grid at zero volts and the plate at 26-30 volts. Thus the neon is not conducting.

With a 1K cathode resistor, the sensitivity of the circuit is about 1.5 volts peak-to-peak (for full neon brilliance). On a signal (in Figure C26C, about 4 volts, peak to peak, for one open half filament) from the detection transformer, the left half operates as a class A amplifier. The plate follows the input signal (Figure C26C)

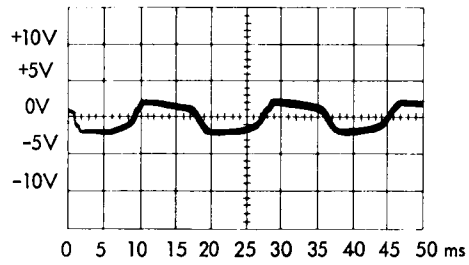


FIGURE C26C. I_{FN} INPUT (FROM DETECTION TFMR)

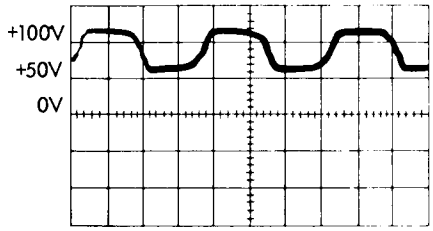


FIGURE C26D. LEFT PLATE

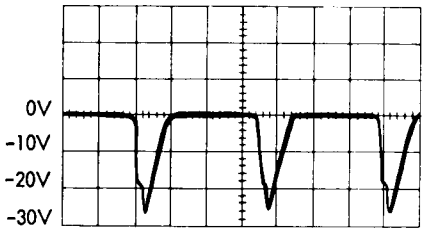


FIGURE C26E. RIGHT GRID (DIFFERENTIATED INPUT)

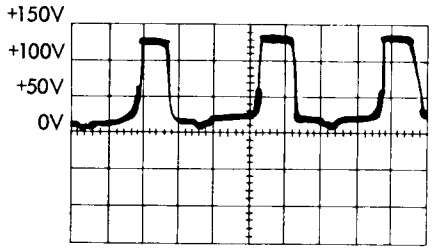


FIGURE C26F. I_{FN} OUTPUT

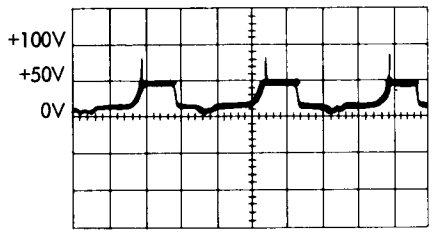


FIGURE C26G. OPEN FILAMENT NEON INDICATOR

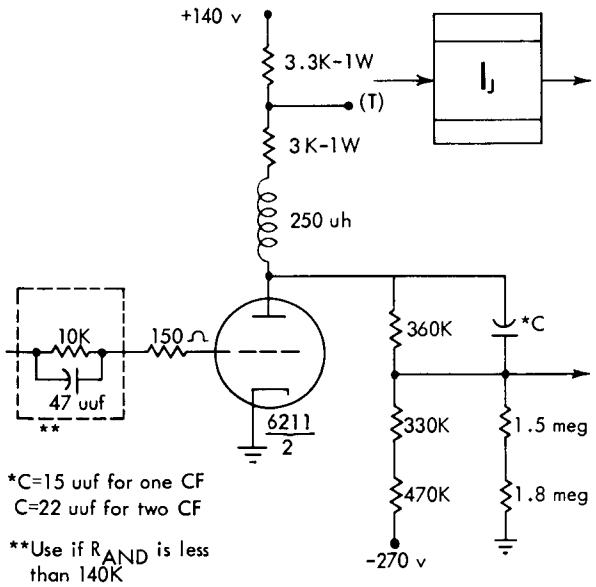


FIGURE C26H. INVERTER -- I_J

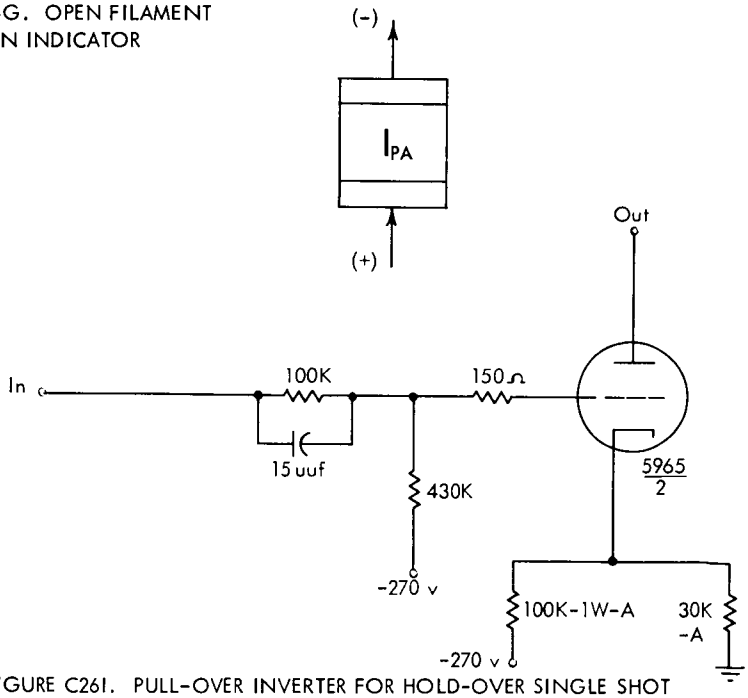


FIGURE C26I. PULL-OVER INVERTER FOR HOLD-OVER SINGLE SHOT

and C26D). The differentiated plate output is coupled to the grid of the right half of the tube. As the signal swings about 25 volts negative (Figure C26E) the tube cuts off, allowing the plate to rise toward +140 volts (Figure C26F). At about 90 volts (Figure C26G) the neon starts to conduct and the voltage across it drops to 50 volts.

When the differentiated signal recovers, it causes the right half to conduct, lowering the plate voltage and causing the neon to stop conduction. Thus, for each cycle of the 60-cycle line, the neon conducts less than one third of the time, or about five ms out of every 17 ms.

This circuit is designed for high sensitivity and may be used with more than 20 pluggable units.

2.01.34 Inverter (I_J, I_{JK})

The I_J (Figure C26H) is used where a better down-level is needed than that obtained from the inverter (I). The I_J is similar to I except that the output divider has been changed to give the better down-level. The I_{JK} is an I_J using a 5965 tube.

2.01.35 Pull-Over Inverter for Hold-Over Single Shot (I_{PA})

The pull-over inverter (I_{PA}) (Figure C26I) is used to pull over the hold-over single shot SS_D. The I_{PA} has a DC input, and holds the SS_D as long as the input pulse is available. The SS_D starts timing when the input pulse to the I_{PA} falls. Reference to the more widely used I_{PD} (section 2.01.19, Book C) shows that the I_{PA} is similar to the I_{PD} except for the cathode return. The I_{PA} is more stable under negative bias.

2.01.36 Inverter, Open Filament Detection (I_{NF})

This circuit (Figure C26J) is used in an open-filament detection circuit. When the filament in a half-tube opens, the bridge circuit becomes unbalanced. The unbalance causes a voltage to appear at the input of the I_{NF}, and the output is used to light indicating neons.

The function of the I_{NF} is basically the same as the I_{FN} (Book C, section 2.01.33) but has lower sensitivity and is used with less than 20 pluggable units.

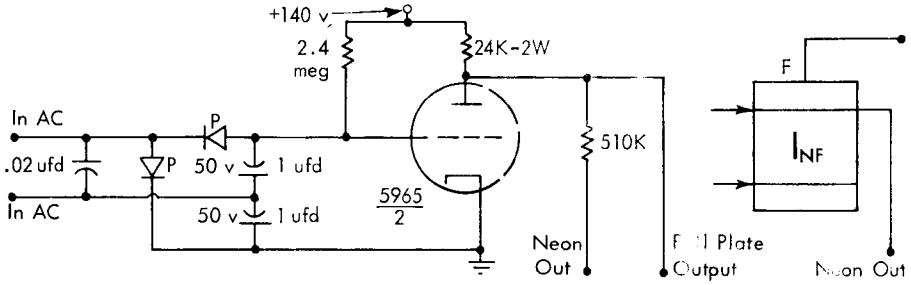
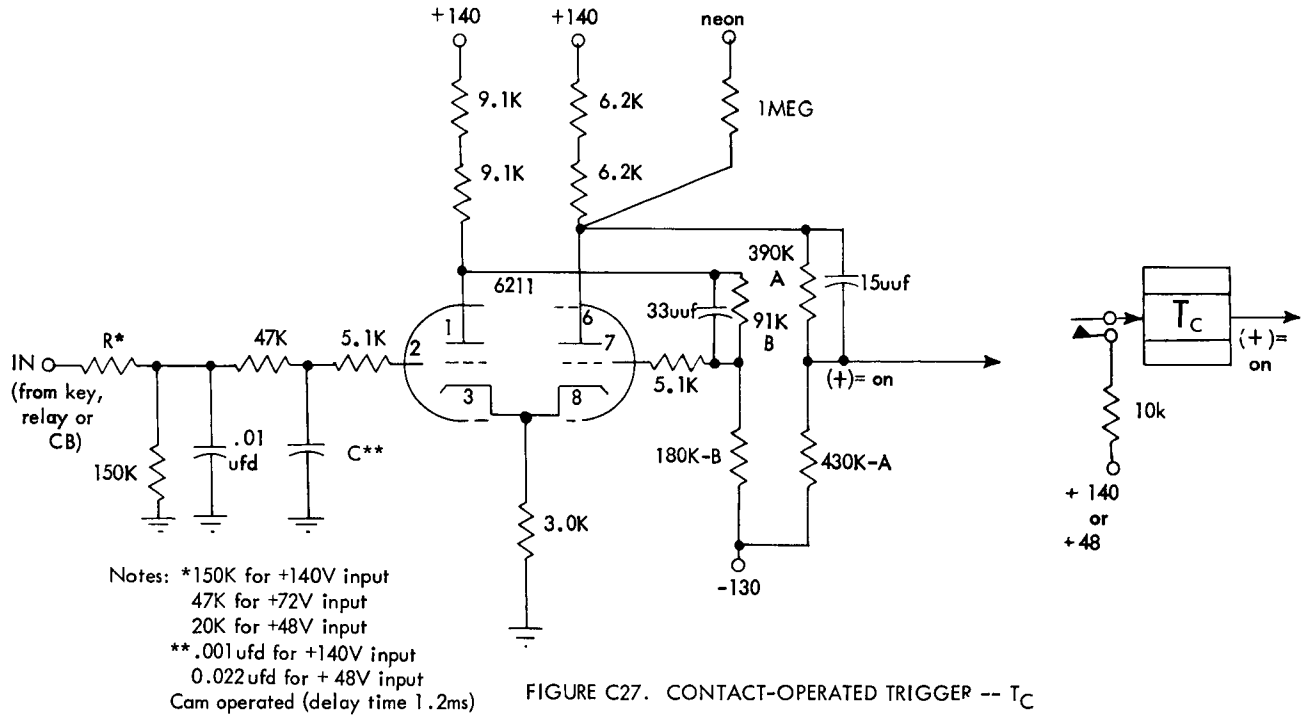
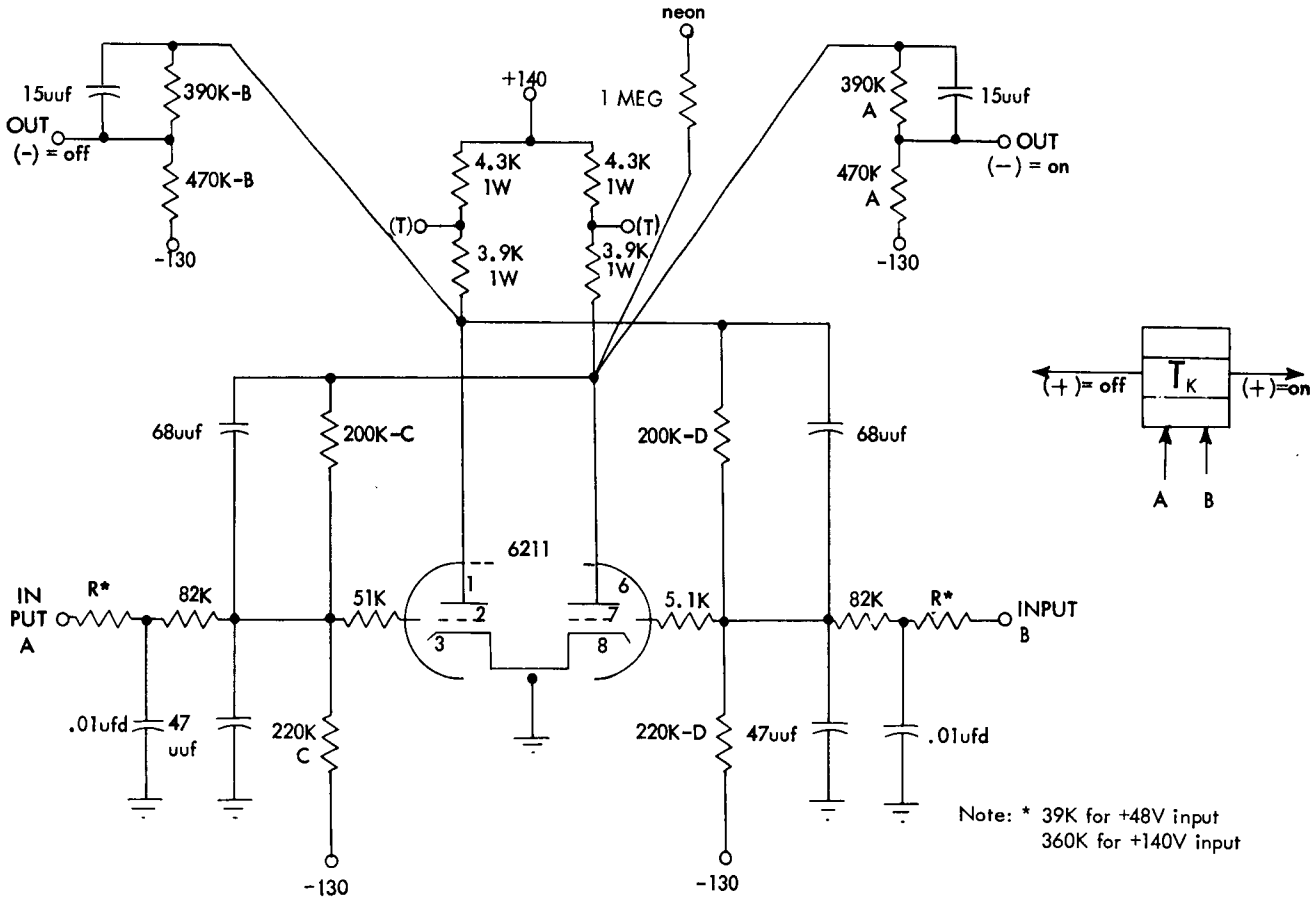


FIGURE C26J. INVERTER FILAMENT DETECTION NEON



Notes: *150K for +140V input
47K for +72V input
20K for +48V input
**.001ufd for +140V input
0.022ufd for + 48V input
Cam operated (delay time 1.2ms)

FIGURE C27. CONTACT-OPERATED TRIGGER -- T_C



Note: * 39K for +48V input
360K for +140V input

FIGURE C28. KEY TRIGGER -- T_K

2.02.00 TRIGGERS

2.02.01 Standard Trigger T (T_A)

The trigger T is described under "Standard Circuits," section 2.06.00, Book A.

The trigger T_A is essentially the same circuit as trigger T with a change in the plate circuit. Each plate circuit in the T_A has two 5.6K resistors and a 750 uh choke in place of the 500 uh choke. The divider outputs swing from +7 to -36 volts nominal. The T_A has slower rise/fall times, and is not satisfactory for fast operation (one megacycle rate) or self-gated binary operation.

2.02.02 Unassigned

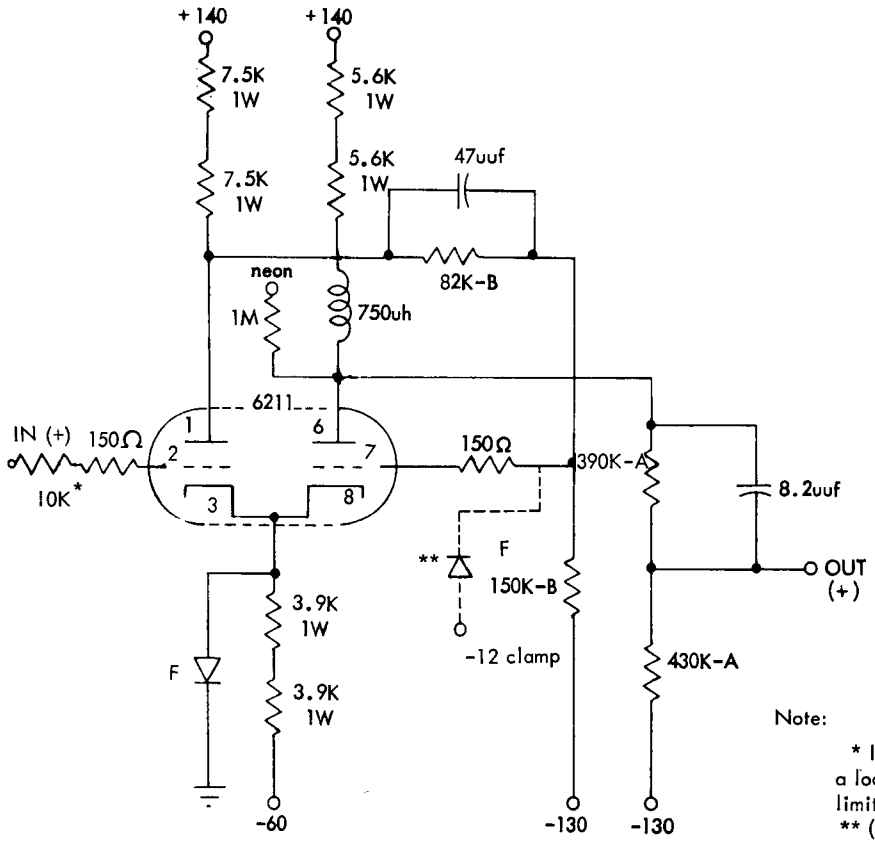
2.02.03 Contact-Operated Trigger (T_C)

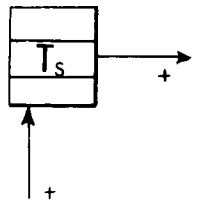
The contact-operated trigger T_C is used to tie a mechanical timing device (key, relay or cam) to the electronic circuits. It is a slowly-operating monostable trigger; it returns to its original state after the input pulse is removed. Shown with the block symbol for a T_C in Figure C27 is a 10K resistor in series with the contacts to either +140 volts or the 48 volts, whichever is being used. The 10K resistor is added to reduce noise, caused by contact bounce as the contacts close to the +140v or to +48v supply. To pass an appreciable amount of current through the contacts (0.5 ma is normal for the above mentioned network), the resistor may be paralleled with the contacts and returned to ground. Noise protection is lessened when the parallel method is used. The value of the resistor depends uppn the current-carrying capacity rating of the contacts in the circuit.

Circuit Description. The purpose of the input network to the grid of the T_C is to integrate any sudden voltage changes that are coming into the circuit. The time constant of an integrating network, being long with respect to the variations caused by contact bounce, is such that the capacitor cannot charge up as fast as the voltage variations. The voltage across the capacitor tends toward the average value of the input. When the contacts cease to bounce, the capacitor charges, and the voltage across it reaches the steady state value of the input voltage.

In its quiescent state, the T_C conducts on the right side with 6.7 ma plate current and about 0.6 ma grid current. The cathode and right grid are about +20 volts with right plate at about +55 volts. The divider output is down at -32 volts. As the positive voltage is applied to the integrated input, the left tube starts to conduct. The falling left plate voltage and the momentary rising cathode voltage both help to cut the right tube off. With the left side in full conduction (5.3 ma), the grid and cathode voltages are about +15.5 volts and grid current of 0.45 ma dissipates the balance of the applied voltage. As the input slowly falls (because of the integration), the left tube starts to cut off. When the left grid falls back down to around +10 volts, the rise of the left plate voltage, coupled to the right grid, causes the right side to conduct, once more pulling the cathode up to +20 volts. Thus, the T_C flips back off.

The right-plate up level is around +135 volts, while the down level is around +55 volts to give a total nominal swing of 80 volts. The right divider output swings from +10 to -32 volts to give a total nominal swing of 42 volts. The approximate rise and fall times are two usec.

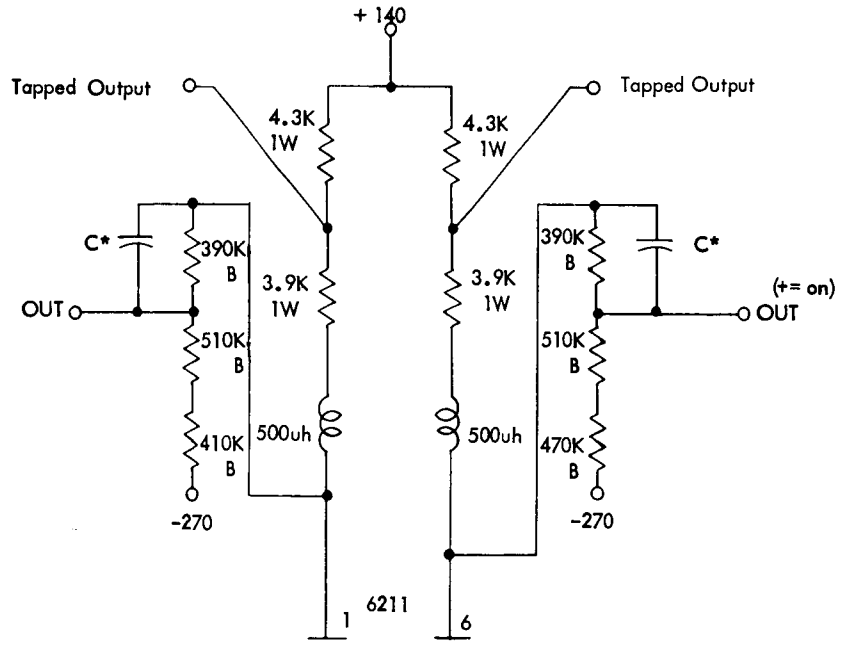


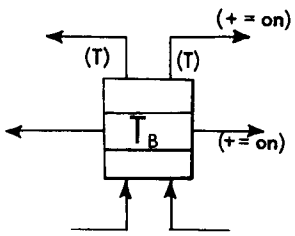


Note:

* If input is from an AND circuit with a load resistor of 140K or more, the 10K limiting resistor is removed.
** (Optional) The addition of this diode improves reliability when biased at -78 volts and input down level is less than -20 volts.

FIGURE C29. TRIGGER -- T_S





Standard Trigger Circuit
Non-Standard Divider Out

FIGURE C30. TRIGGER -- T_B

The 150K to ground provides a DC path to ground for the grid circuit. The two resistor-capacitor combinations (R* with C**, and 47K with .001 ufd) provide a double integrating network. The 5.1K resistor to the grid has a triple effect. It serves to limit grid current, to suppress parasitics, and to increase the integrating action of the input network.

2.02.04 Key Trigger (T_K)

The key trigger T_K in Figure C28 is used wherever a key, cam or relay is to operate a storage type trigger. The input circuits on both the on and off (left and right) side of the T_K are integrated inputs. See section 2.02.03, Book C, on the contact trigger T_C for operation of integrated inputs to a trigger. The current-limiting and noise-suppressing features used with the T_C are also employed with the T_K. In most other respects the T_K is similar to the standard trigger T (section 2.06.00, Book A). Unlike the standard trigger, however, the key trigger does not have peaking coils in the plate circuits. This results in slower rise for the T_K than for the T.

The plates of the T_K swing from +132 to +52v. The divider outputs swing from +13 to -31v. The approximate rise and fall times of the T_K are two microseconds. The comparatively slow times are due to the slowing effects of the integrating input networks as well as the elimination of peaking coils.

2.02.05 Trigger (T_S)

The trigger T_S (Figure C29) is a monostable trigger, similar in operation to the TC. It restores to its quiescent state after the positive input pulse is removed. The T_S uses a pulse input and does not require an integrated input.

Circuit Description. When the input is down to -30 volts, the left tube is cut off because the cathode is at ground. (An 8.2-ma current is drawn by the right tube through the common cathode resistor.) Actually, the cathode tends to rise above ground if all this plate current is drawn through the resistor, but the diode clamps it to ground, and some of the current comes through the diode. The right grid draws approximately 0.57 ma and the output is -36 volts. When the input rises to a level somewhere between -5 volts and -1 volt, the left plate comes down, driving the right grid to cut-off through the 82K coupling resistor and the 47 uuf coupling capacitor. The 750-uh coil aids in speeding this shift. When the right tube is cut off and the left tube is conducting, the output is +10 volts. When the input again drops to a level between -3 to -6 volts, the left side is cut off; the trigger flips off. Again the 750-uh coil aids somewhat in flipping the circuit. The response of the circuit is such that the rise and fall times of the circuit are not dependent on the input signal. Below is a summary of the circuit's currents and voltages with the standard inputs.

E_g (v)	I_{P1t} (ma)	I_{Prt} (ma)	I_{G1t} (ma)	I_{Grt} (ma)	E_{B1t} (v)	E_{Brt} (v)	E_o (v)
-30	0	8.2	0	0.57	+122	+49	-36
+10	7.25	0	1.0	0	+22.5	+135	+10

2.02.06 Trigger (T_B)

The trigger T_B (Figure C30) is a standard trigger T with a special divider output. A 510K resistor is added in series to the 470K and the divider is returned to -270

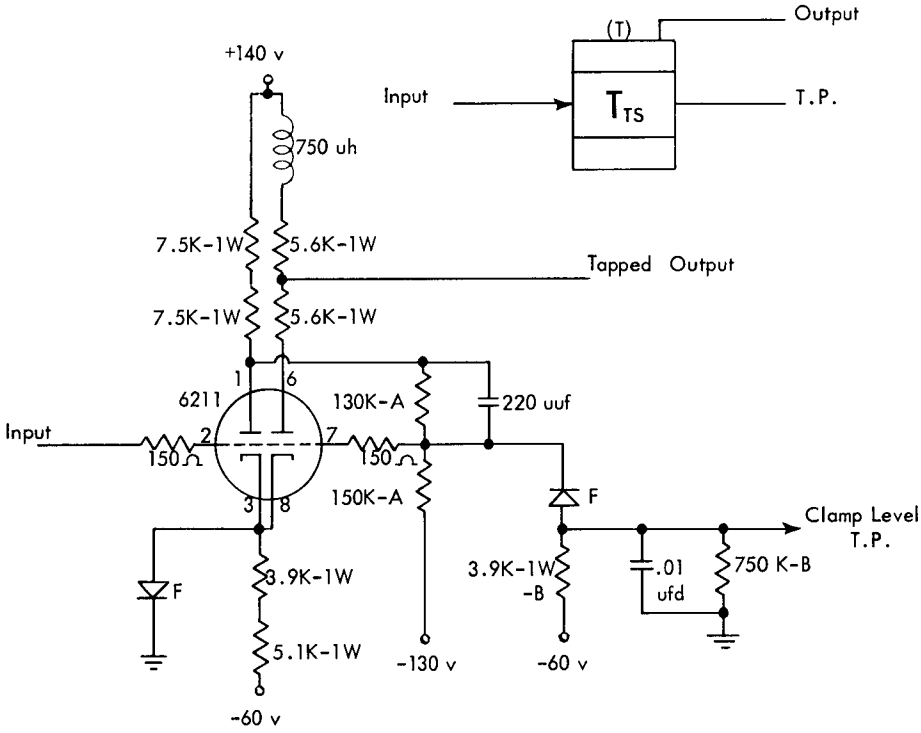


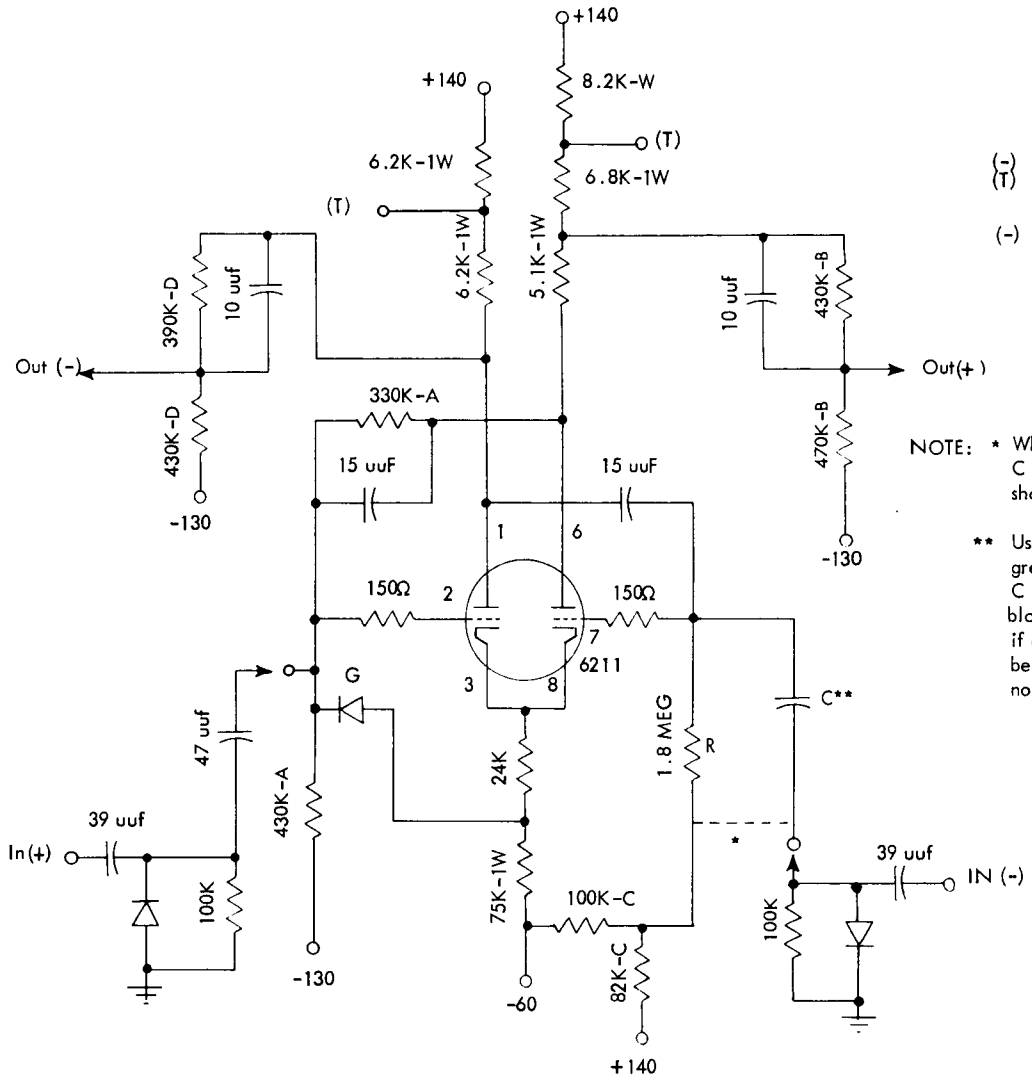
FIGURE C30A. SCHMITT TRIGGER, TAPE -- (T_{TS})

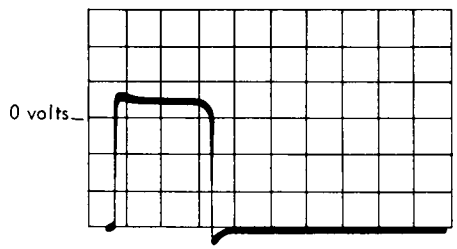
volts. The T_B has a nominal output swing from +10 to -38 volts. The lowered-down level is necessary when feeding several cathode followers to prevent down-level loss (down-levels rising above -30 volts).

2.02.07 Schmitt Trigger--Tape (T_{TS})

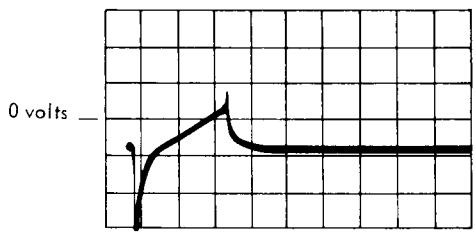
The Schmitt trigger T_{TS} (Figure C30A) is a monostable trigger similar to the more widely used T_S (section 2.02.05, Book C). The input to the T_{TS} is an integrating AND circuit. The function of the components is to sense amplified signals from magnetic tape if these signals are of sufficient energy content. Before reaching the T_{TS}, the signals read from the tape pass through a final amplifier where they are amplified and rectified to become positive-going pulses rising above a fixed bias voltage. These positive-going pulses gate the AND circuit input to the T_{TS} and cause it to flip if the input has enough width and amplitude to drive the left grid above -5 volts. The left side remains in conduction until the input drops below -6 volts.

The only output used is a negative shift from the right plate as the input voltage drops. The clamp level of the right grid determines the input voltage at which the trigger flips. When several T_{TS} components are used in parallel, the clamp levels are wired together to insure that all triggers have the same sensitivity.





Right Divider Out 20 usec/sd 10 V/sd



Right Grid 20usec/sd 10 V/sd

FIGURE C31. SINGLE SHOT -- SS

2.03.00 SINGLE SHOTS

Single shots are monostable multivibrators; that is, the circuit has one stable state. When impulsed or triggered, the single shot changes to its quasi-stable state and returns to its stable condition after a predetermined length of time. These circuits are used to generate gates or pulses of specified duration and to provide delays.

2.03.01 Single Shot (SS)

The single shot (SS) is used to produce pulses, gates and delays. The timing of the SS is variable and, by proper selection of the timing resistor R and the timing capacitor C, the timing can be varied from about 10 usec to about 500 milliseconds.

Circuit Description. Initial status is with the right tube conducting because the right grid is effectively tied to +50 volts (the junction of the 100K-82K divider circuit). With the right side conducting, the cathode voltage is about -8 volts for most tubes; hence, the right grid is also approximately -8 volts with grid current flowing. The diode, from the lower end of the 2.4K cathode resistor to the left side of the 150-ohm left-grid resistor, clamps this grid to about 12 volts below the cathode when the circuit is quiescent. This voltage remains constant regardless of the tube's condition because the combination of the cathode resistors and the right plate resistor is very large compared with the tube resistance. In the quiescent state, the various nominal voltage levels are:

Left Plate	Right Plate	Left Grid	Right Grid	Cathode
+135v	+26v	-20v	-8v	-8v

The SS remains in this state until impulsed from an external source.

Consider a positive 40v shift being applied to the positive input. The input circuit contains a diode to clamp all negative shifts and has a time constant of 3.2 usec (the 100K in parallel with the back resistance of the diode). With this time constant, the input pulse must be of at least 4-usec duration in order for the negative shift of the pulse to be clamped out. The differentiated positive spike is coupled through the 47-uuf capacitor to the left grid bringing the grid voltage up. As the left grid voltage is brought up through cut-off, the left tube begins to conduct. The resultant drop in voltage at the left plate is coupled over to the right grid, tending to cut off the right tube. Two other actions aid in cutting off the right tube and the increase in positive voltage on the left grid. The increased current in the left plate circuit causes the voltage across the common cathode resistor to increase, aiding in cutting off the right tube. The decrease in the right plate current causes the right plate voltage to go up and this condition is coupled to the left grid to increase the action. With the left tube in full conduction, the various nominal voltage levels are:

Left Plate	Right Plate	Left Grid	Right Grid	Cathode
+50v	+126v	+7v	-20v*	+7v

*With C = 100 uuf. The amount that the right grid is lowered depends upon the value of C. The 85v shift at the left plate is proportionately divided between the

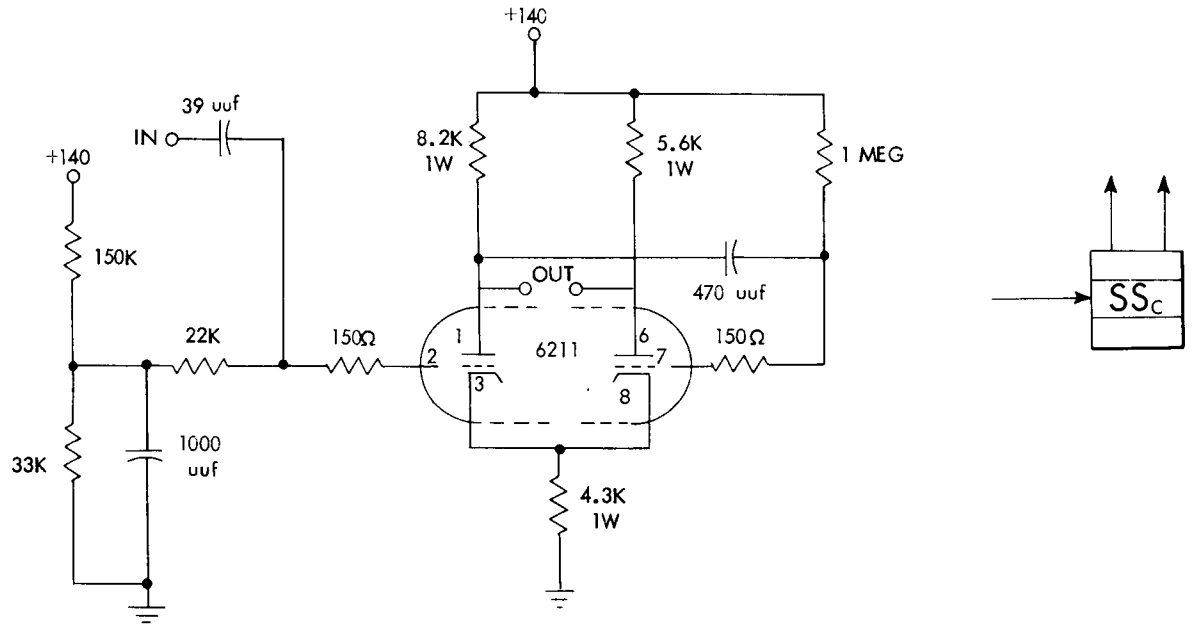
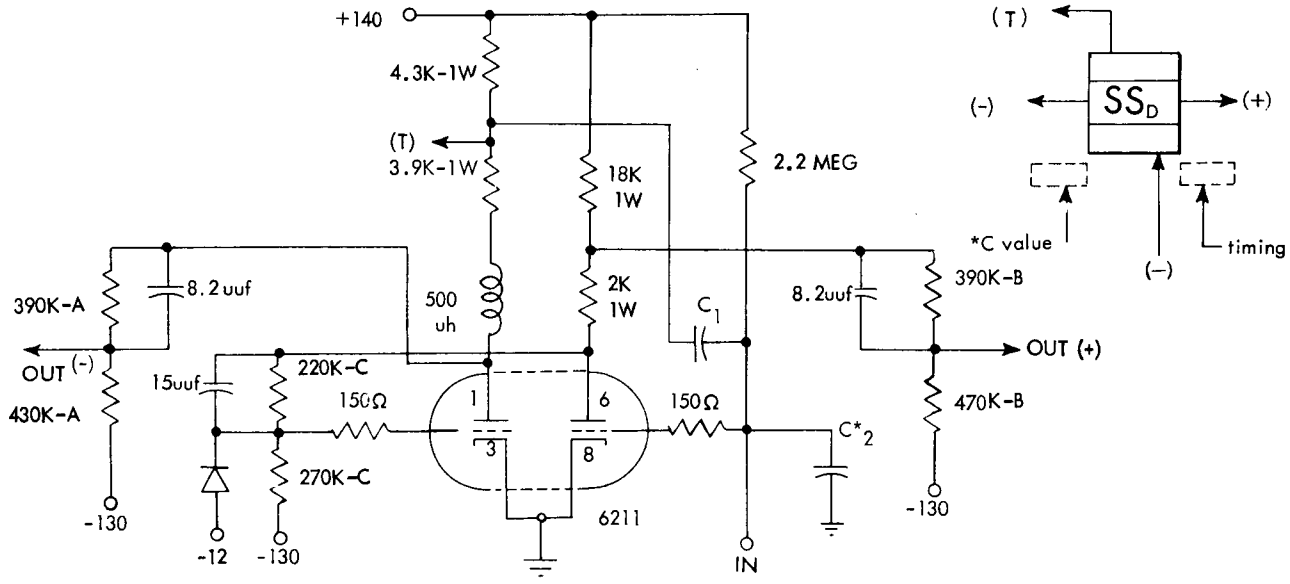


FIGURE C32 CLOCK SINGLE SHOT -- SS_C



NOTES: $C_T = (C_1 + C_2) = 1.42T$ with C_T in uuf & T in usec
If $C_T \leq 200$ uuf ($T \leq 155$ usec), then $C_1 \cong 47$ uuf
If $C_T > 200$ uuf, then $C_1 \cong 1/2\ C_2$
*When a left-hand output is used, clamp left grid to -12

FIGURE C33. HOLDOVER SINGLE SHOT -- SS_D

coupling capacitor and the timing capacitor C. With C being 100 uuf, the grid is lowered about 12 volts.

Timing. Although almost all of the elements in the circuit affect the timing to a greater or less extent, the capacitor C and the 1.8 MEG resistor to ground are the components used to vary timing. The value of C is varied to determine the duration between 35 microseconds and several milliseconds, while the 1.8 MEG resistor must be decreased (by experimentation) to obtain pulses down to 10 microseconds. The action of the circuit is as follows in regard to timing. The time constant of the 15-uuf coupling capacitor and the 82K resistor is short compared to the timing of the single shot, so that the right grid returns quickly to -8 volts. The timing capacitor acts as a source of electrons aiding in discharging the coupling capacitor. The timing capacitor C begins to discharge through the 1.8 MEG resistor toward an equivalent voltage of +50 volts determined by the 82K and 100K resistor in the cathode circuit. This capacitor charges from -8 to about +2 volts. At this point, the right tube begins to conduct once more, and the regenerative effects described previously restore the circuit to its quiescent condition. The right grid returns to -8 volts as the right side comes back into full conduction. See wave form (Figure C31).

Restoration. As to the restoration of the circuit to its original condition, be careful that the circuit has completely recovered before it is pulsed again. If this is not done, the duration of the SS will be shorter the second time because the left plate is partway down. The negative shift will then be smaller and the resulting pulse shorter. The recovery time for the circuit is about 10 percent of the duration of the single shot for all timings.

Inputs. The positive input to the left grid must be a positive-going 25v to 70v pulse. The SS can also be impulsed by applying a negative-going 15v to 70v pulse to the grid. Note in Figure C31 that the negative input requires that the wiring for C be changed. In this case, the input pulse is coupled through C to the right grid. The discharge path is changed to include the input components and the power supply.

Outputs. The right divider output is a -32v to +8v pulse with a rise time of 1.2 microseconds and a fall time of 0.8 microseconds. (See wave form, Figure C31.) The left divider output is a +10v to -30v pulse with a rise time of 0.7 microseconds and a fall time of 0.8 microseconds. The SS time is noted to the lower right or left of the SS block on the system diagrams.

2.03.02 Clock Single Shot (SS_C)

The clock single-shot SSC (Figure C32) is used in the clock reset circuit in the 702 arithmetic and logical unit. The output of the SS_C is about a 70-usec pulse.

In the quiescent state, the right tube is conducting and the left tube cut off with the following nominal voltage values in the circuit:

Left Plate	Left Grid	Right Plate	Right Grid	Cathode
+140v	+25v	+80v	+38v	+38v

The input is a negative pulse from the left divider of another single shot. The negative portion of the pulse is ignored because the left tube is cut off. The positive shift causes the left tube to go into conduction. The rising cathode and the falling left

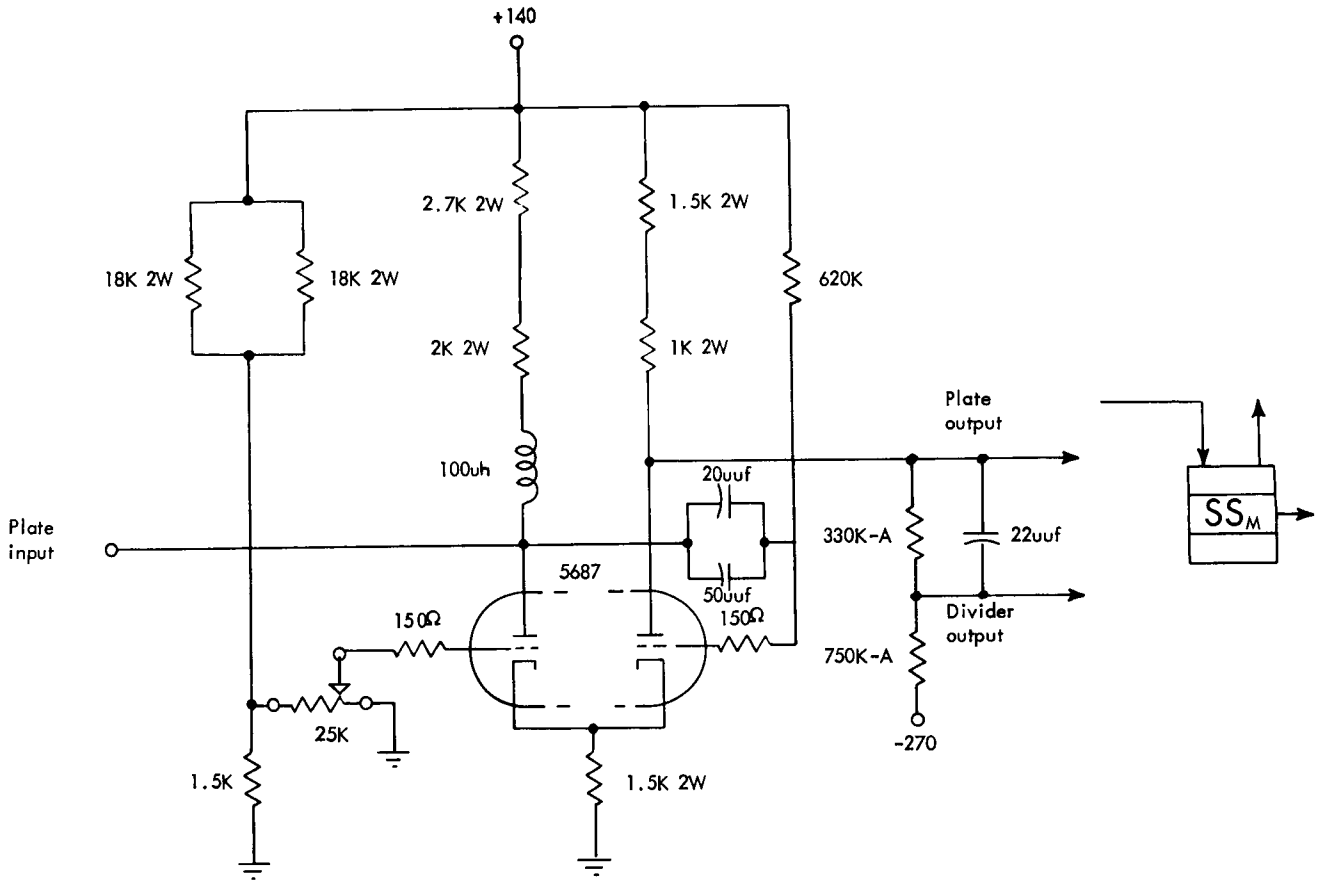


FIGURE C34. SINGLE SHOT (MEMORY) -- SS_M

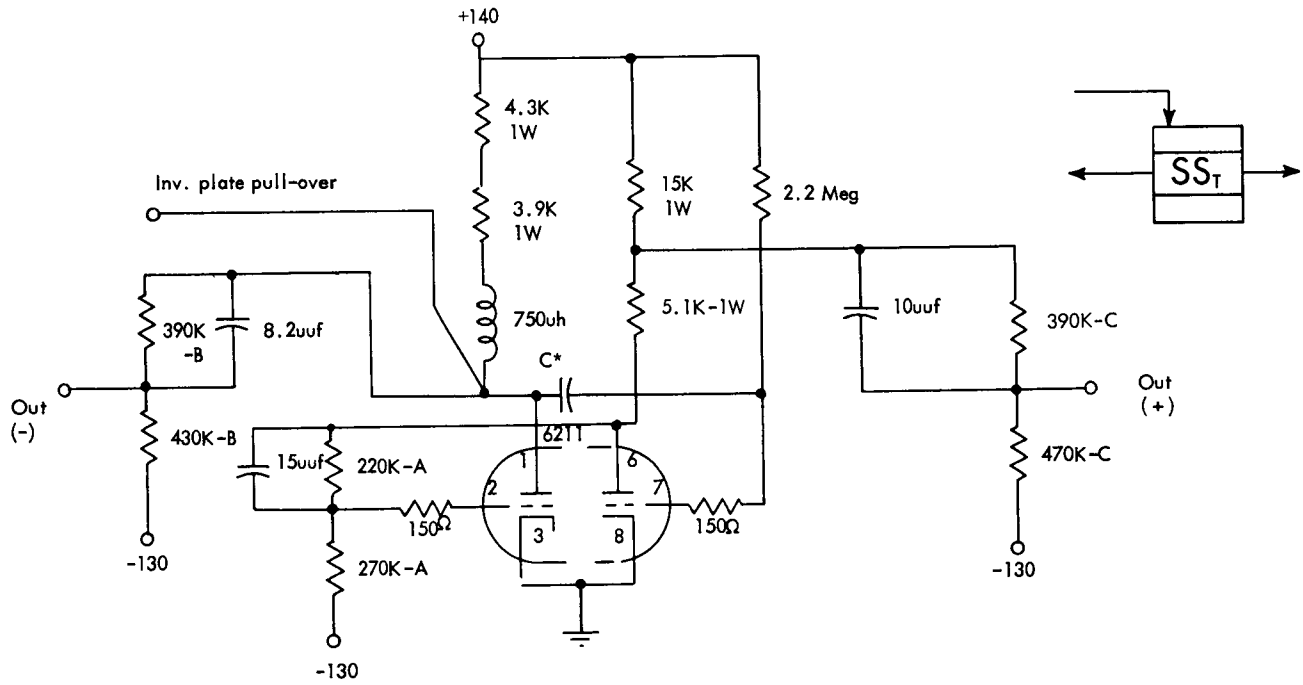


FIGURE C35. PHOTOCELL SINGLE SHOT -- SS_T

plate voltage both tend to cut off the right tube. The left grid quickly falls back to +25 volts as set by the divider. With the left tube in conduction and the right tube cut off, the following nominal voltage values are in the circuit:

Left Plate	Left Grid	Right Plate	Right Grid	Cathode
+90v	+25v	+140v	-12v	+26v

The SS_C stays in this quasistable state until the right grid returns to about +18 volts; as the 470-uuf capacitor charges toward +140 volts through the 1 MEG resistor. The right tube, going back into conduction, raises the cathode voltage and the left tube cuts off.

2.03.03 Holdover Single Shot (SS_D)

The holdover single shot (SS_D) (Figure C33) has a peculiar characteristic in that the left plate is held down as long as the input pulse repetition rate is greater than the single shot timing. Timing does not begin until the last input pulse in a series is reached. For example, suppose that the single shot timing is set for 200 microseconds. If the interval between input pulses is less than 200 usec (for example every 190 usec), the SS_D flips with the first pulse and does not time out until 200 usec after the last pulse has arrived at the input. Thus, the SS_D is a useful circuit to indicate the end of a record on tape (the absence of regularly spaced characters).

Circuit Description. The input to the SS_D is from the pull-over inverter I_{PO}. (See section 2.01.18, Book C, for I_{PO} operation.) The I_{PO}, conducting through the 2.2 MEG resistor, causes the right tube to cut off rapidly with its grid falling to about -60 volts. Cross-coupling speeds the regenerative action and the circuit stabilizes momentarily with the left tube conducting and the right tube cut off. The right tube stays cut off as long as its grid is held down below -8.5 volts. Once pulled down by the I_{PO}, the grid is immediately released to rise under the control of the discharge time of the timing capacitors. If the I_{PO} conducts 190 usec later (using a 200-usec SS_D), the right grid is pulled down to -60 volts before the cut-off voltage is reached. Therefore, the SS_D stays in the quasistable state until 200 usec after the last input pulse to the I_{PO}. Once the right tube is allowed to conduct, the regenerative action returns the SS_D to its stable state.

Outputs The following nominal output levels can be obtained from the SS_D:

Output	Levels	Rise/Fall Time
Left Plate	+137v, +59v	1.2/0.8 usec
Left Tap	+138v, +97v	1.2/0.8 usec
Left Divider	+9v, -32v	1.2/0.8 usec
Right Plate	+125v, +40v	0.4/0.3 usec
Right Divider	+9v, -32v	0.4/0.3 usec

2.03.04 Memory Single Shot (SS_M)

The SS_M (Figure C34) is a special single shot used to give a very short pulse of variable duration, and to have a short recovery time. The width of the output pulse is controlled by varying the bias on the left grid. The more positive the grid voltage, the wider the output pulse.

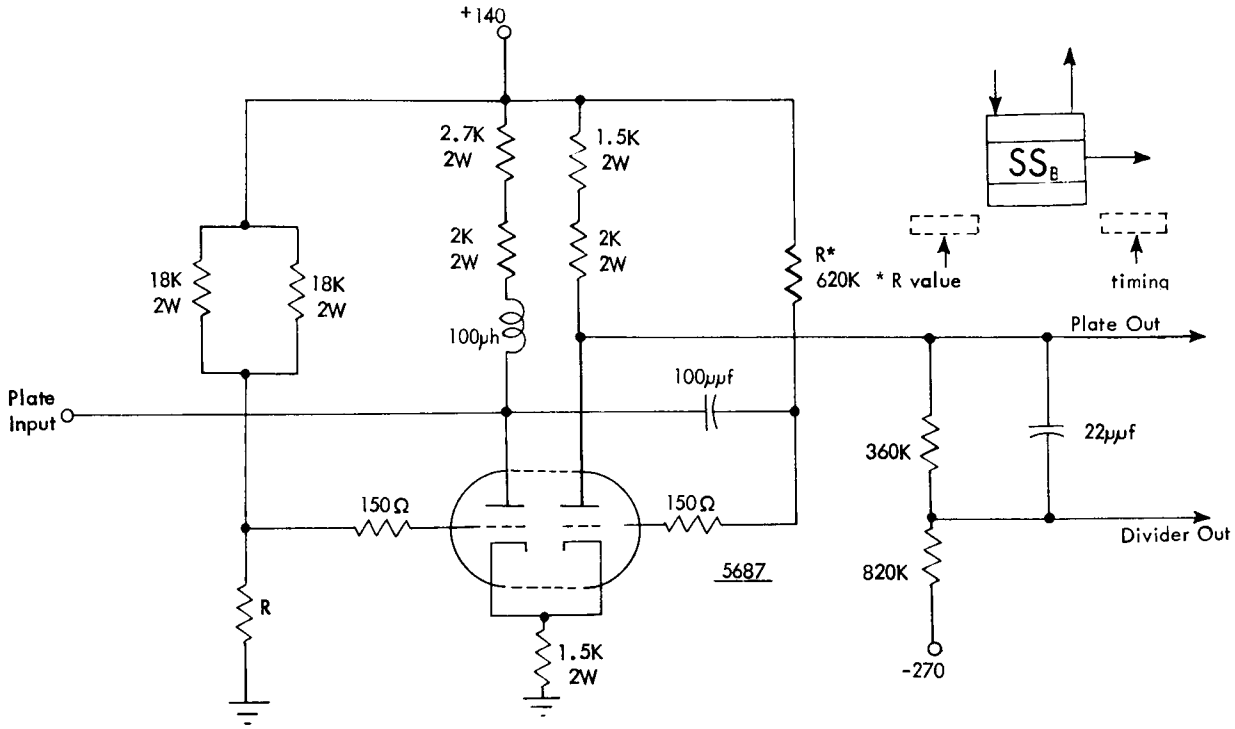


FIGURE C36. SINGLE SHOT (BUFFER) -- SS_B

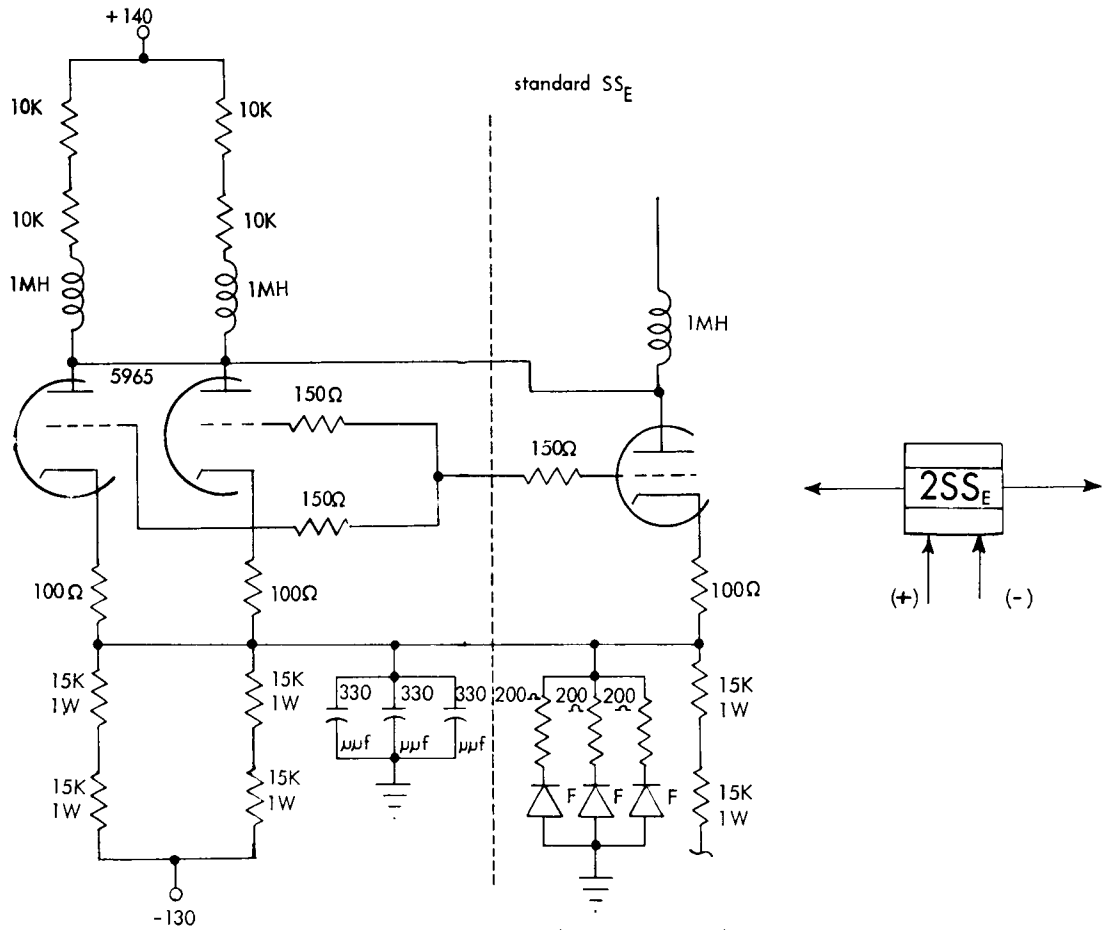


FIGURE C37. SINGLE SHOT (FAST RECOVERY) -- $2SS_E$

Circuit Description. In its quiescent state, the right tube is conducting about 22.5 ma and the cathode voltage is +34 volts. The left tube is cut off because the bias limits are 0-20 volts as set by the potentiometer. The input to the SS_M is a negative shift at the left plate that is coupled through 70 uuf to the right grid. The right tube cuts off and the cathode voltage falls. The left tube assumes a level of conduction dependent upon the bias setting. The right grid rises exponentially toward +140 volts. The point where the right tube goes back into conduction is governed by the preset cathode voltage caused by the left tube's conducting. The right tube's conducting again raises the cathode voltage and the left side cuts off. The coil in the left plate circuit speeds the regenerative action without affecting response of the circuit.

Outputs. The plate output of the SS_M swings from +139 volts to +83.7 volts while the divider output swings from +44 volts to -35.3 volts. The output pulse width may vary from two to five microseconds, and the circuit is quite stable within this range, despite variation in plate supply.

2.03.05 Photo-Cell Single Shot (SS_T)

The photo-cell single shot (SS_T) (Figure C35) is used in the tape drive unit to generate a 20-millisecond gate in the load point, tape break, and end-of-file recognition circuits. The SS_T is pulled over by an inverter sharing the SS_T left plate circuit. As the reflective spot or tape break is sensed by a photo-cell, the I_{PC} (section 2.01.15, Book C) cuts off and causes the pull-over inverter to conduct. The SS_T flips and stays in its quasistable state as long as the RC circuit holds the right grid down. The circuit returns to its stable state as the right tube returns to its conducting status.

The left divider output has a nominal swing from +8 volts to -36 volts. The right divider output has a nominal swing from +6 volts to -32 volts.

2.03.06 Single Shot (SS_B)

The single shot (SS_B) (Figure C36) is similar in operation to the SS_M. The common cathode resistor is used to accomplish the regenerative action common to all single shots. The input to the SS_B is plate pull-over with the resultant negative shift causing the circuit to flip and start timing. The SS_B timing is varied by changing the value of R in the left grid return. Most common usage is a nominal 6-usec output pulse. The plate output swings from +138 volts to +75 volts while the divider output swings from +14 volts to -32 volts.

2.03.07 Single Shot (SS_E and SS_F)

The single shots SS_E and SS_F are described under "Standard Circuits," (section 2.11.00, Book A).

2.03.08 Single Shot--Fast Recovery ($2SS_E$)

The fast-recovery single shot (Figure C37) is used in applications where a short recovery time is needed. The $2SS_E$ employs two additional paralleled left tubes of the standard SS_E. This procedure allows a lower effective resistance path to charge C_T (section 2.11.02, Book A).

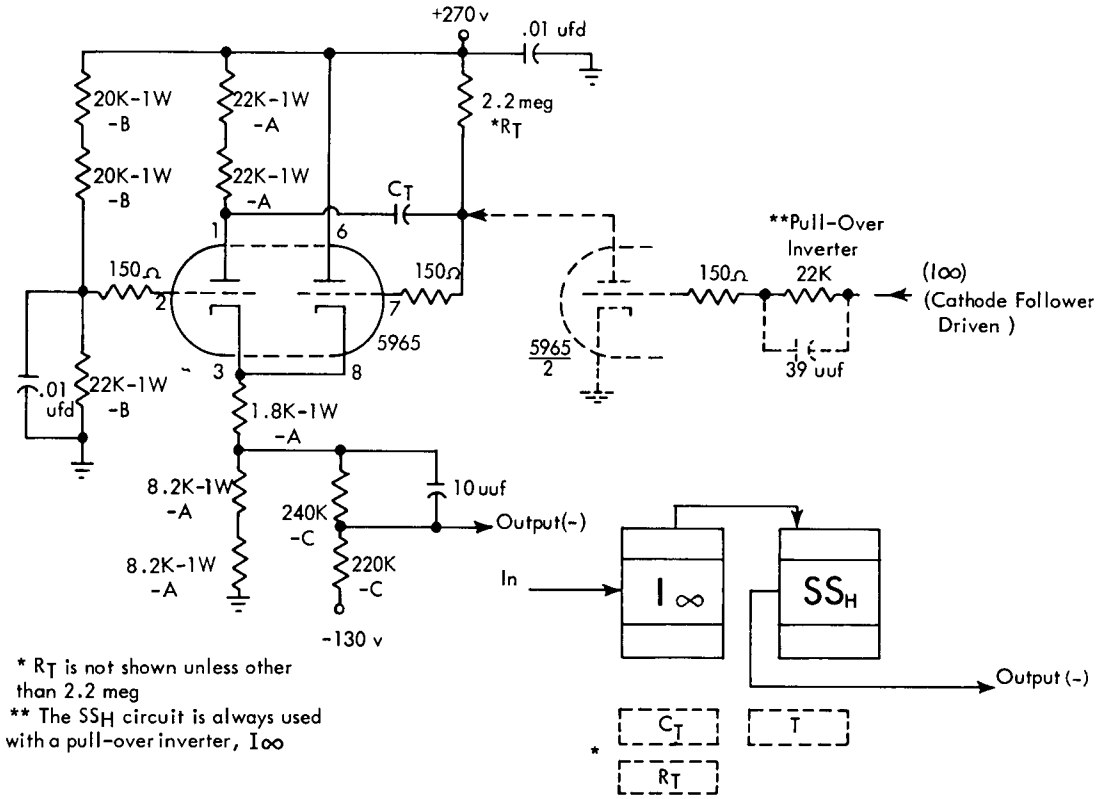


FIGURE C37A. DIRECT-COUPLED HOLD-OVER SINGLE SHOT--SS_H

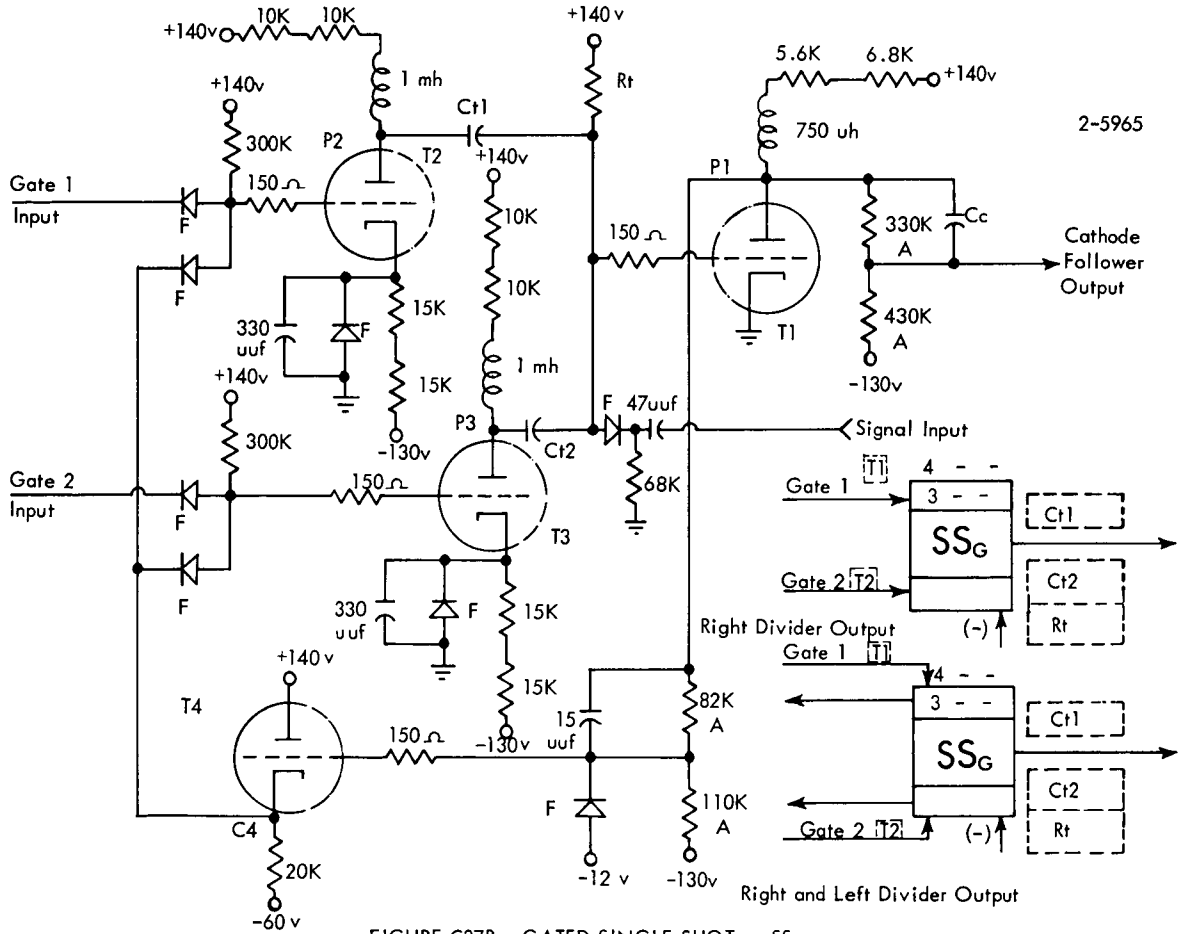


FIGURE C37B. GATED SINGLE SHOT -- SS_G

2.03.09 Direct-Coupled Hold-Over Single Shot (SS_H)

The basic difference between the SS_H (Figure C37A) and the standard SS is that the SS_H is driven by a direct-coupled pull-over inverter. The only output is a negative output from the cathode. A positive input to the grid of the inverter causes the SS_H to change to its quasi-stable state. As long as the input is retained, the SS_H does not begin its timing period.

To make the circuit operation stable, the 270v supply is used for all positive returns. The cathode circuit is grounded. Stability is improved by the direct connection of the right plate to the positive line. The SS_H is useful for adding several milliseconds of time, and is stable under bias conditions.

2.03.10 Gated Single Shot (SS_G)

General Description. The SS_G (Figure C37B) will operate as a normal single shot in that it will generate a timed pulse at the output. However the duration of the output pulse can be controlled electronically by use of two gate-circuits. When pulsed at the input (-), the SS_G generates an output pulse of a duration that is determined by the gated circuit. One gate, when open, causes the SS_G to time out at a predetermined time (tl). The other gate causes a time-out of a different time duration (t2).

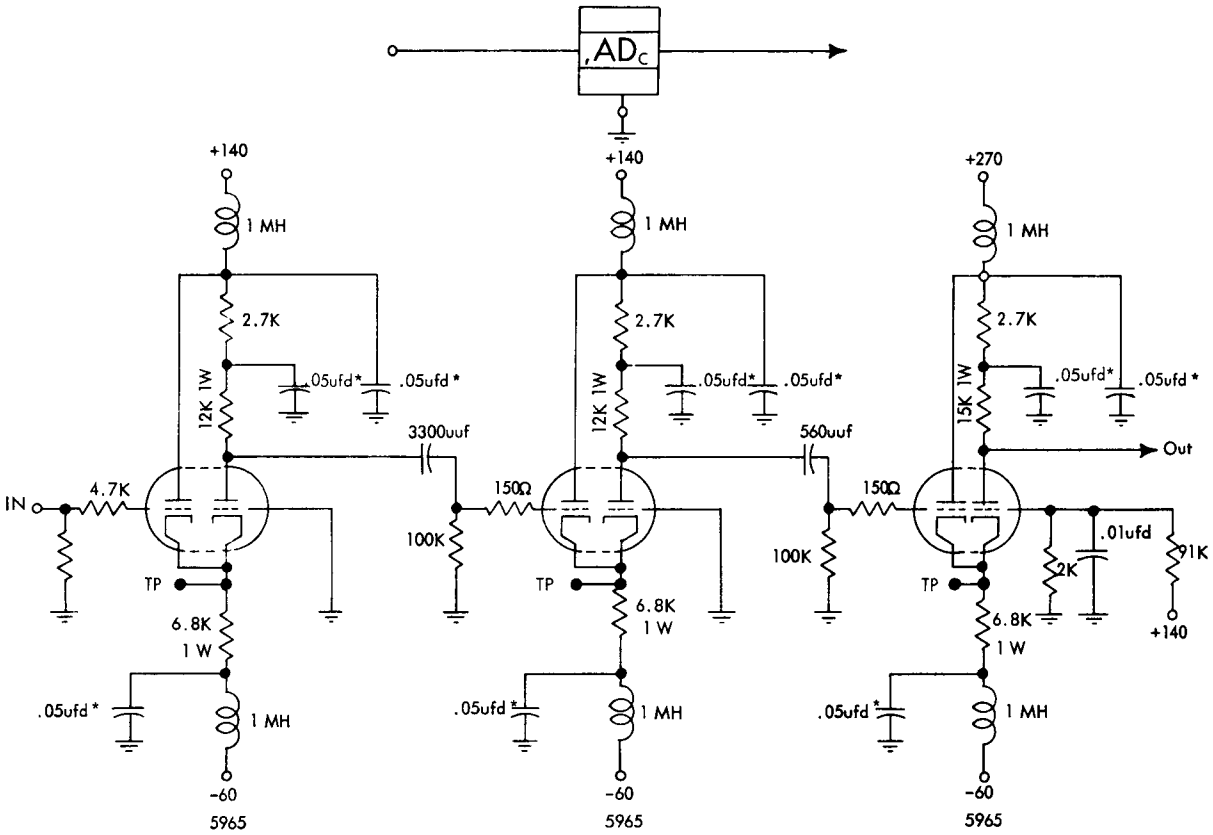
Circuit Operation. In the quiescent state, tube 1 (T1) is conducting. The grid is above cut-off because of the +140v supply through Rt. The timing capacitors Ctl and Ct2 have charged to +140 volts through the plate load resistors of tubes 2 and 3 (T2 and T3).

Only the negative shift of the input pulse is sensed through the input circuit. This negative shift drives T1 well beyond cut-off, allowing the output to rise (start of the timed pulse). If gate 1 is open (conditioned +10 volts) by the "gate 1" line and gate 2 is closed (-30 volts on "gate 2" line), the following occurs: The rise of P1 from +58 volts to +138 volts causes the left divider output of T1 to raise the grid of T4 from -12 volts (-12v clamp) to about +15 volts. T4 conducts and K4 rises to +10 and, because gate 1 is open, the grid of T2 causes T2 to conduct.

Gate 2 is closed (-30 volts). Therefore, T3 remains cut off. As T2 goes into conduction, P2 drops from +138 volts to +40 volts, thus discharging Ctl. The change reflects to the grid of T1 and holds it below cut-off as the capacitor Ctl charges through Rt. When the grid of T1 reaches -6 volts, T1 conducts (thus ending the timed pulse).

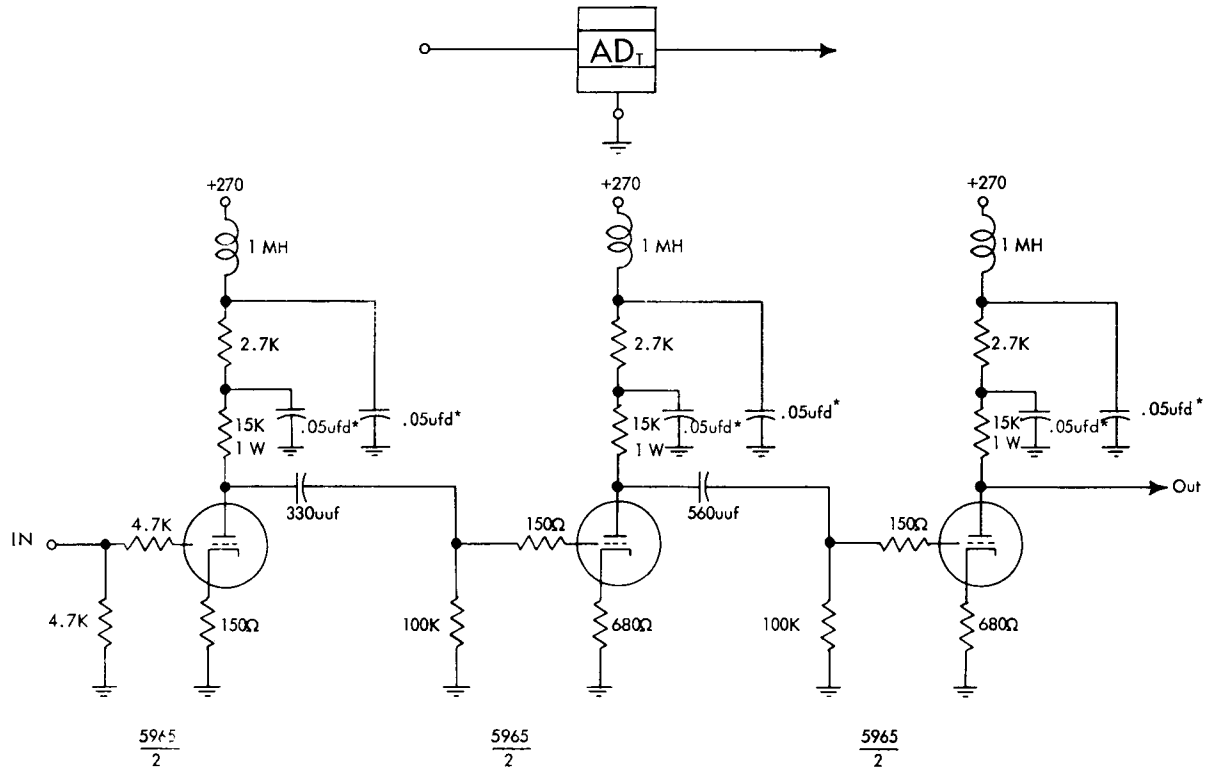
T1 remains cut off for a length of time determined by the Rt Ctl combination. When gate 2 is conditioned and gate 1 deconditioned, the time duration is determined by Rt Ct2 combination. Thus, two different SS_G timings can be used under control of the "gate 1" and "gate 2" lines.

An inverted pulse can be obtained by use of a divider from the plate of T2 or T3.



*Signifies Gudeman Capacitors

FIGURE C38. AMPLIFIER DRUM (COMMON) -- AD_C



*Signifies Gudeman Capacitors

FIGURE C39. AMPLIFIER DRUM (TIMING) -- AD_T

2.04.00 AMPLIFIERS

2.04.01 Amplifier Drum (Common) (AD_C)

The AD_C (Figure C38) is used in the drum to amplify the voltages from the read heads. The AD_C uses grounded-grid amplifiers throughout, because of their advantages of better recovery time and increased stability. The AD_C employs 1-MH coils and .05-ufd capacitors, as do most drum circuits, as an aid in keeping variations occurring in the circuits from entering the power supply. Note that the test points are at cathode level and do not reflect the true output voltage swing for each stage.

The input to the AD_C is from the preamplifiers PA (section 2.04.11, Book C). All of the preamplifiers share the 1.5K resistor at the input to the first stage of the AD_C as common cathode resistor. Only one preamplifier at a time has the required plate voltage for conduction at any particular time. The preamplifiers have a gain of better than 0.6 and a minimum input voltage of 100 millivolts. This means that the input to the AD_C will be around 60 millivolts. Each stage has a gain of approximately ten for an over-all gain of 1000 for the amplifier. The output of the AD_C is then 60 volts (peak to peak) or greater. The output of the AD_C is fed to a shaper (drum) SD (section 2.01.30, Book C).

2.04.02 Amplifier Drum (Timing) (AD_T)

The AD_T (Figure C39) is used in the drum to amplify the signal from the read coil of the timing track. The AD_T is composed of three stages of RC-coupled amplifiers. The first stage has a gain of 15 while the second and third stages have a gain of approximately ten for an over-all gain of 1500. The average signal input to the AD_T is about 40 millivolts so the output will be near 60 volts.

The AD_T employs decoupling between stages for decreased interaction and to keep amplifier variations out of the power supply. Stability is maintained through the use of degeneration. The output of the ADT is fed to the shaper (drum) S_D (section 2.01.30, Book C).

2.04.03 Unassigned

2.04.04 Read Preamplifier (AT, D_T)

The read-preamplifier AT, D_T (Figure C40) is used in the tape unit to amplify the signals from the read head. The AT is an RC-coupled amplifier with RC decoupling in the plate circuits. The decoupling decreases interaction between stages and tends to isolate the +270v power supply from circuit variations. Cathode degeneration is used for stability. Degenerative feedback from the third stage back to the first is controlled by the setting of the 50-ohm potentiometer. This procedure sets the gain of the amplifier and stabilizes the output amplitude. The plate-to-ground capacitor at the third stage tends to keep noise pulses out of the output.

Circuit Description. Input signals are about 35 millivolts (peak to peak) directly from the read head. The output signals are 20 volts (peak to peak) and are AC-coupled to the grid of a cathode follower through a 51K resistor. The DC level of the K grid is set by "gate read pulse" through the tube diode D_T.

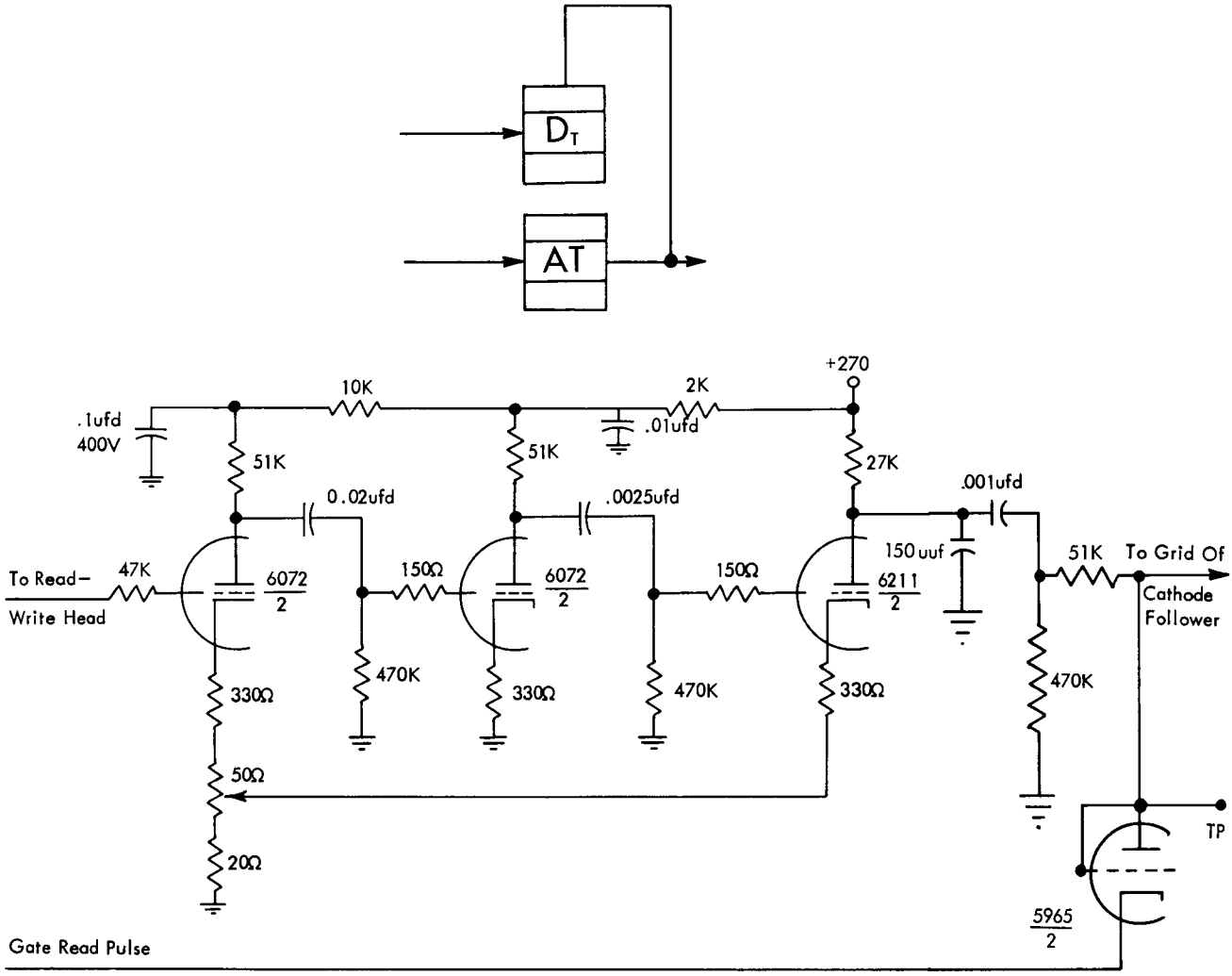


FIGURE C40. READ PRE-AMPLIFIER -- AT

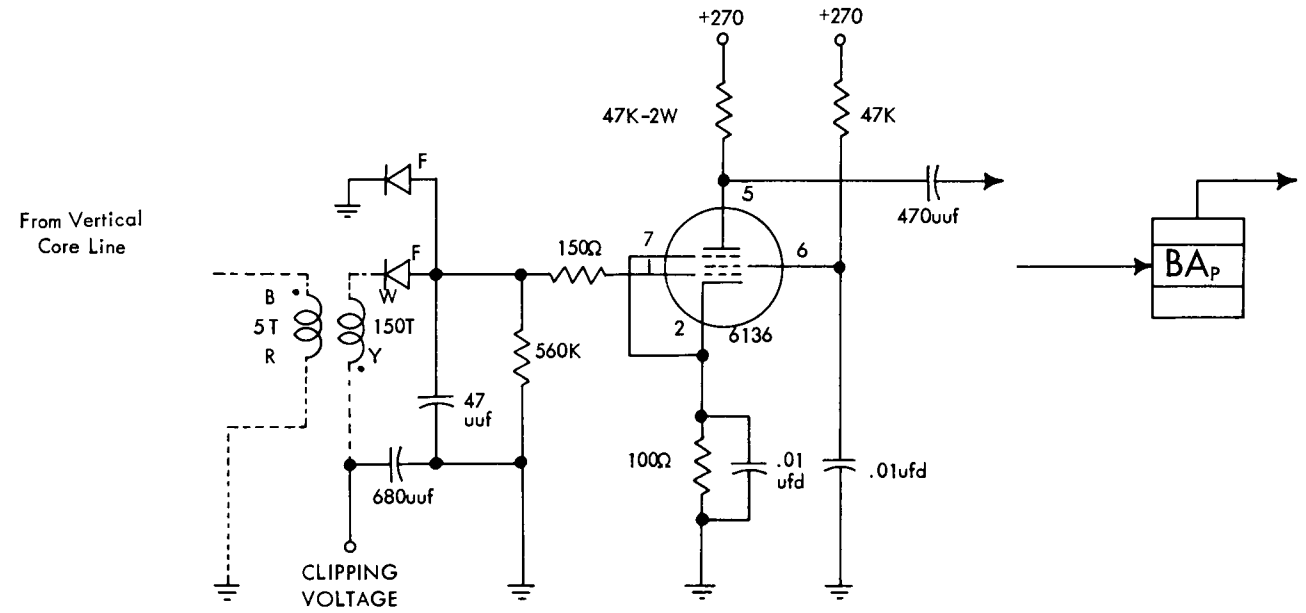


FIGURE C41. PRINTER/PUNCH BUFFER AMPLIFIER -- BA_P

With "gate read pulse" down (approximately -25 volts) the diode conducts through the 51K and 470K resistors to ground; the DC level at the diode plate is -24 volts. Any signal or noise will be effectively swamped out because the plate of the diode is not able to go more positive than this level, regardless of the amplitude of the noise passed by the .001-ufd input capacitor.

With "gate read pulse" up (approximately +11 volts), the diode is cut off and the diode plate is at ground level through the 51K and 470K resistors. The input signal to the grid of the K varies between +10 volts and -10 volts. The output pulse of the K also varies between +10 volts and -10 volts.

2.04.05 Grounded Grid Amplifier (GA_F)

The grounded grid amplifier (GA_F) is covered under "Standard Circuits," section 2.10.00, Book A.

2.04.06 Printer/Punch Buffer Amplifier (BA_P)

The printer/punch buffer amplifier (BA_P) (Figure C41) is used in the printer/punch circuits to fire the print or punch magnet thyratrons. A pulse transformer is used as part of the input circuit to the BA_P. The transformer has a 1:10 turn ratio and is so wired as to invert the signal. Thus, a rising voltage at the top of the primary winding provides an amplified falling voltage at the top of the secondary winding. The placing of the dots near the windings indicates the polarity reversal.

Circuit Description. In its quiescent state, the BA_P is conducting with its grid returned to ground and no signal applied. The 100-ohm resistor and its bypass capacitor in the cathode set the bias of the BA_P at about -1 volt. Screen current of about 3.3 ma sets the screen voltage at +115 volts. Plate current of about 5.3 ma sets the plate voltage at +20 volts. The grid is diode-clamped so that it cannot rise above ground potential. The clipping voltage sets the cathode of the input diode about two volts positive with respect to the grid. (See machine acceptance specifications for exact value.) Because core lines produce ringing pulses, the clipping voltage isolates the amplifier from the unwanted portion of the input pulses and noise.

As the first pulse from the core line (about 450-600 millivolts peak-to-peak) goes positive, the top of the transformer secondary goes negative. Once the clipping bias is overcome, the input diode conducts and the tube is cut off. The 47-uuf capacitor and the 560K in the grid circuit act as a pulse stretcher. Thus, the grid is held below cut-off (about -3.5 volts) for several microseconds after the input diode has cut off. The procedure also tends to isolate the tube from the normally ringing core line.

The cut-off tube produces about a 100v positive shift at the plate with an indefinite duration of about 30-usec because of the pulse stretching effects. The pulse stretching effect is needed to insure proper thyratron operation. When the grid returns to its quiescent state, the BA_P again conducts at its steady state rate, and its output voltage falls. The actual magnitude that the AC-coupled output voltage reaches depends upon the loading of output circuits.

2.04.07 Read-In Current Driver (CD_H)

The read-in current driver (CD_H) (Figure C42) is used in the printer and punch read-in circuits to supply half the necessary currents to read into the printer and

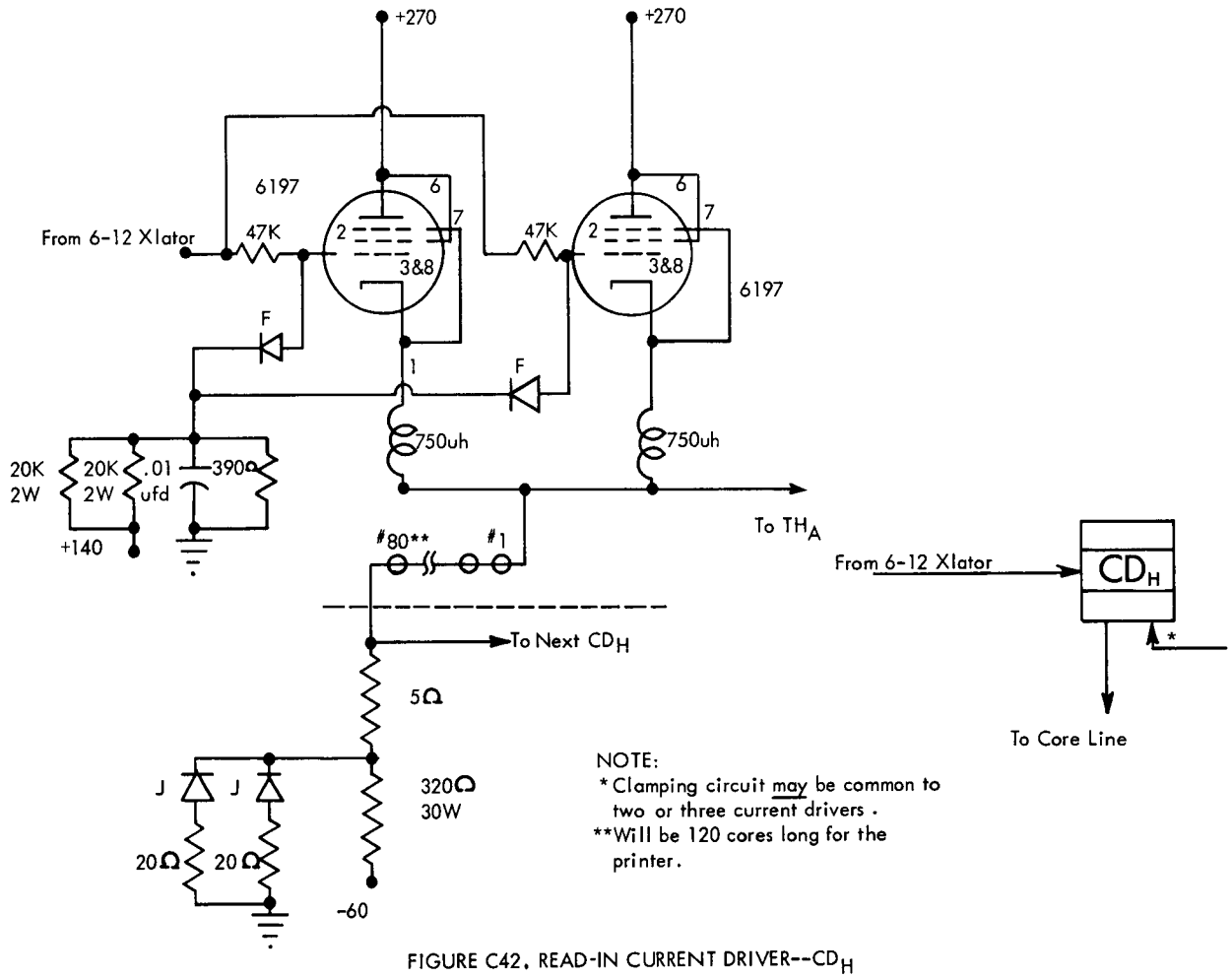


FIGURE C42. READ-IN CURRENT DRIVER--CD_H

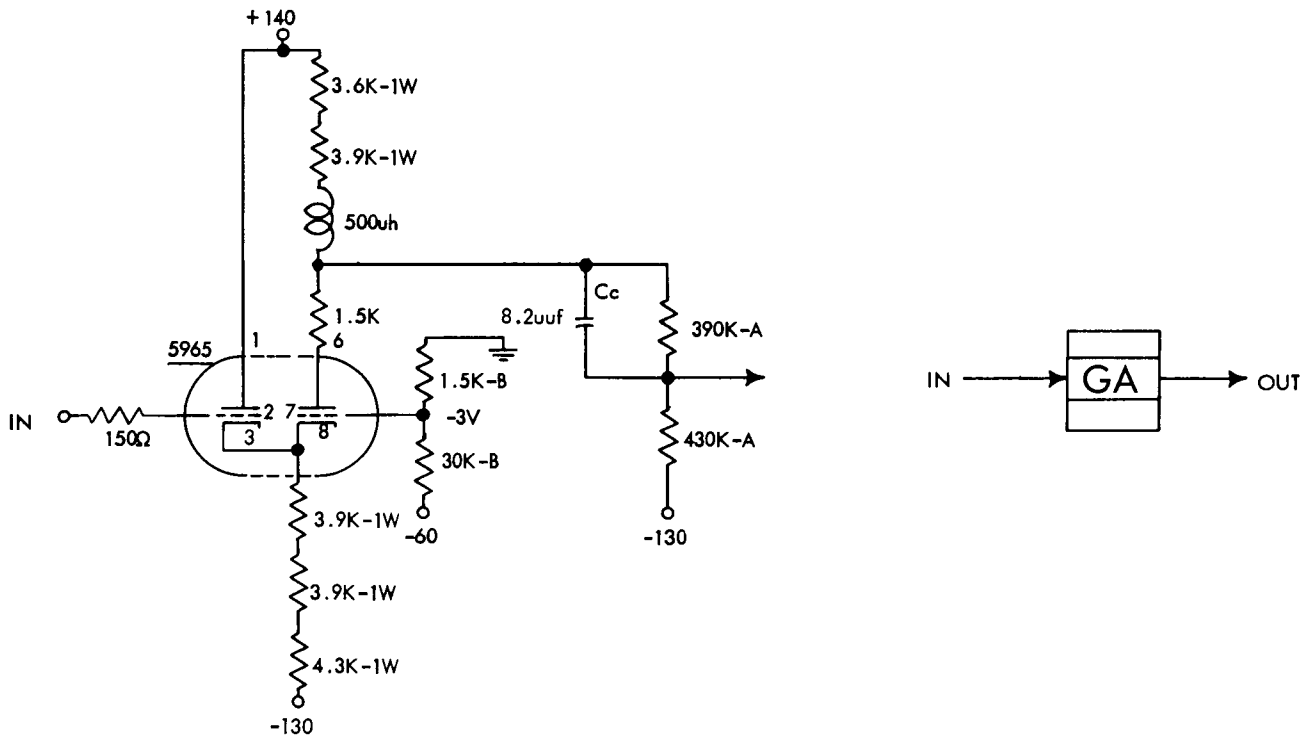


FIGURE C43. STANDARD GROUNDED GRID AMPLIFIER -- GA

punch buffers. The CD_H provides the horizontal coincident half-current while the thyratron ring provides the vertical coincident half-current. A CD_H uses two parallel 6197 tubes.

Circuit Description. The input to the CD_H is the 6-12 translator line. The status of this line is either +10 volts or -30 volts. When this line is down to -30 volts, the current driver is cut off, and has no effect on the horizontal core line. When the input rises to +10 volts, the current driver conducts, drawing its current through the core line. The control grids to the current driver are clamped to +5 volts by the diode. The grids themselves actually never go above +5 volts even when the translator line comes up to +10 volts. The series-parallel network of junction type diodes and 20-ohm resistors returned to ground at the end of each horizontal core line prevents this end of the line from going below ground. Junction type diodes are necessary to carry the relatively heavy current that exists when the current driver is cut off. The 750-microhenry coils in the cathodes of the CD_H slow the rise time of the current pulse when the current drivers start to conduct. This slowing of the rise time aids in shaping the read-in pulse.

2.04.08 Differential Amplifier (DA)

This component was assigned to 702 electrostatic memory and is not used now.

2.04.09 Grounded Grid Amplifier (GA)

The grounded grid amplifier (GA) (Figure C43) is similar to the grounded grid amplifier GA_F (section 2.10.00, Book A). The principal difference is the tapped plate connection in the GA. The different connection causes the divider output to vary from +10 to -30 volts rather than from +10 to -38 volts. In all other considerations, the two circuits are alike.

2.04.10 Unassigned

2.04.11 Preamplifier (Drum) (PA)

The drum preamplifier (PA) (Figure C44) is used to power the signals from the drum read heads. Preamplifiers are primarily cathode followers and no voltage amplification takes place in this stage. The amplification of preamplifiers is about 0.6 The input signal to the preamplifier is approximately 100 millivolts, and the output is approximately 60 millivolts. Preamplifiers are connected in a cathode-follower OR circuit configuration with one preamplifier for each track in each channel. Each OR circuit composed of the preamplifiers, therefore, contains 30 preamplifiers with one common load resistor. This common load resistor is the 1.5K resistor at the input to the AD_C (section 2.04.01, Book C). This preamplifier OR-circuit configuration is somewhat unusual in that each preamplifier has its input voltage up at the same time, but only one preamplifier is supplied plate voltage at a time. Therefore, only one preamplifier at a time has an output, and an input to the common amplifier.

2.04.12 Relay Driver (R_D)

The relay driver (R_D) (Figure C45) is used to supply the current for operation of relays. A load resistor in series with the relay that is to be operated is chosen so that the total load on the R_D is not less than 2000 ohms. When the input is brought up, the tube conducts and the relay is picked. An R_{DX} is an R_D using a 5965 tube in place

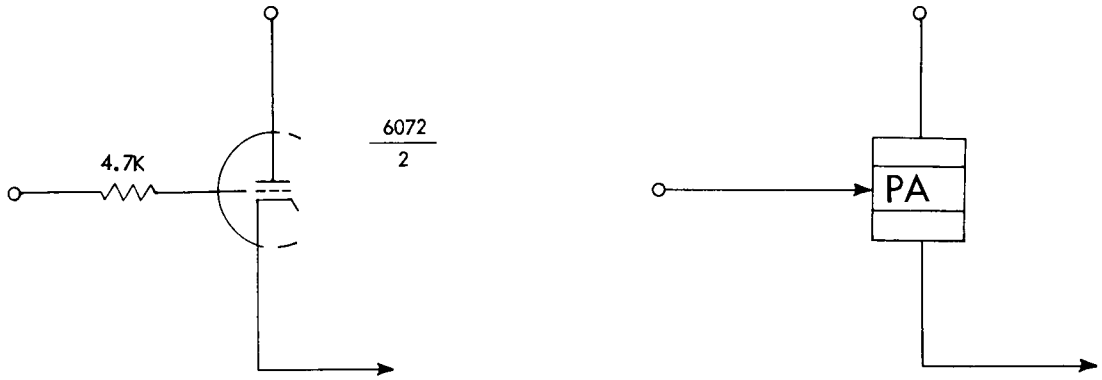


FIGURE C44. PREAMPLIFIER (DRUM) -- PA

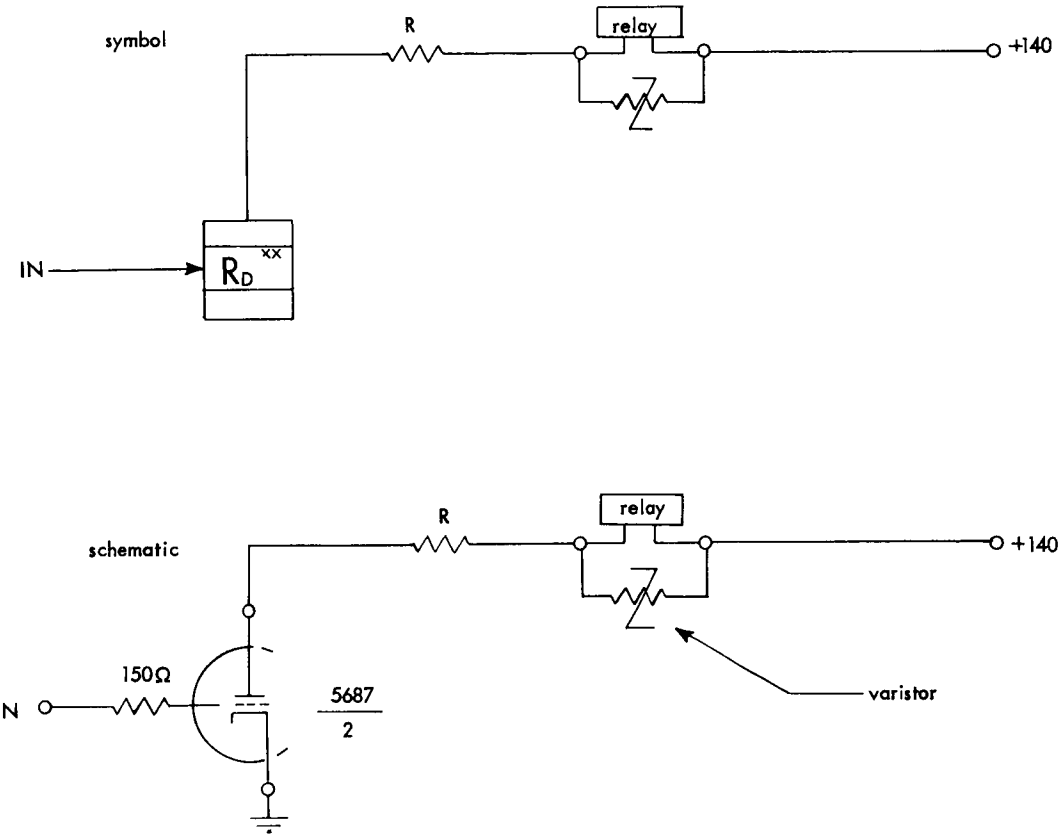


FIGURE C45. RELAY DRIVER -- R_D

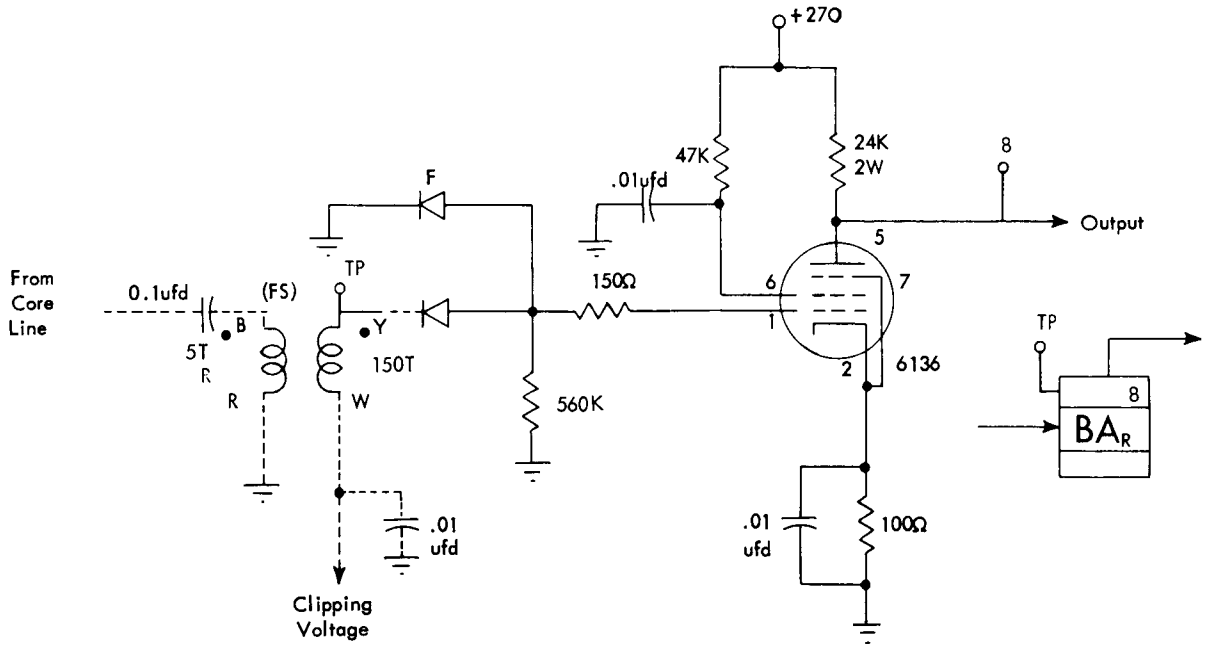


FIGURE C46 READER BUFFER AMPLIFIER -- BA_R

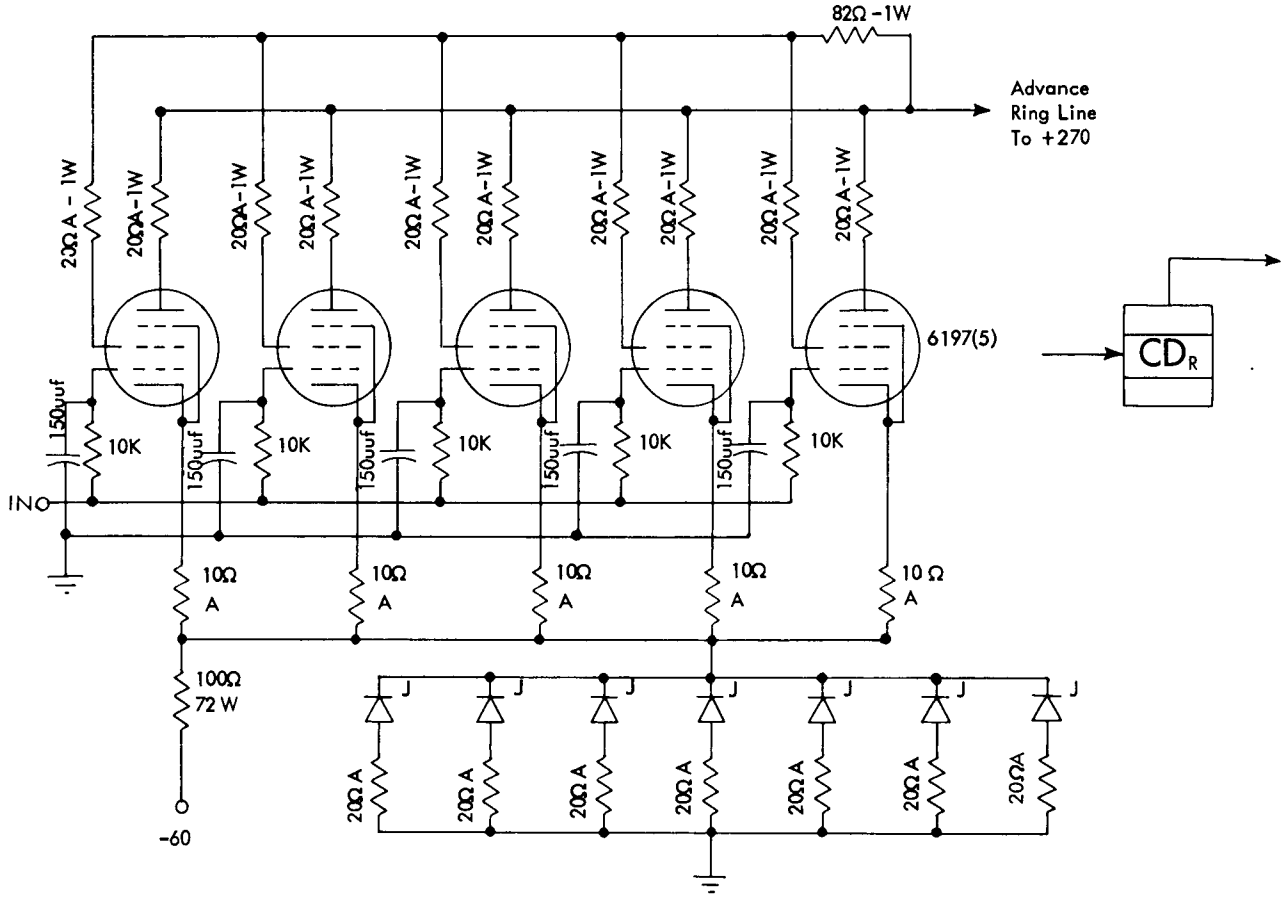


FIGURE C47. RING CURRENT DRIVERS -- CD_R

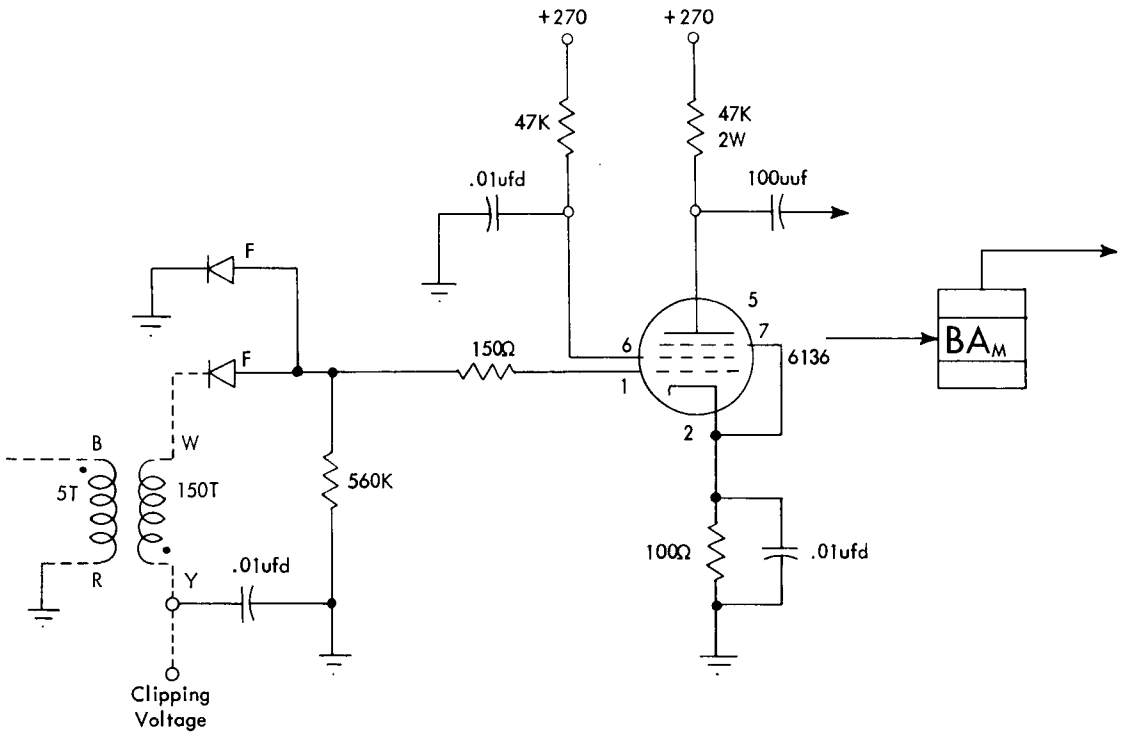


FIGURE C48. PRINTER/PUNCH ROW MEMORY BUFFER AMPLIFIER--B_{AM}

of the 5687. The resistor R is chosen so that the total load in the plate of one half of a 5965 is not less than 6000 ohms. An RD_1 uses a 6350 in place of a 5687.

2.04.13 Unassigned

2.04.14 Video Amplifier (VA)

This component was assigned to 702 electrostatic memory and is not used now.

2.04.15 Reader-Buffer Amplifier (BA_R)

The reader buffer amplifier (BA_R) (Figure C46) is used to amplify the signals from the row memory core lines in the reader. Because the cores in the reader are set in the opposite direction from punch/printer, the initial swing of the output pulse is opposite too. Therefore, the pulse transformer is wired so as not to invert the signal. The initial swing is negative at both the primary and secondary windings.

As far as circuit operation is concerned, the BA_R is very similar to the BA_P (section 2.04.06, Book C) with one exception. The grid of the BA_R is not held down by an RC circuit. Therefore, the tube is cut off for a much shorter time than was the BA_P, although both circuits are impulsed very similarly The output pulse of the BA_R is a +48v pulse of approximately 1.2-usec duration. See the machine acceptance specifications for exact value of clipping voltage.

2.04.16 Ring Current Driver (CD_R)

The ring current driver drives the thyratron rings in the printer, punch, and card reader. The circuit for the CD_R is shown in Figure C47. The input pulse to the ring current driver is a two microsecond pulse from an I_{PF}. A current pulse from the output of the current driver resets the ring cores in the thyratron ring circuits. The 10-ohm resistors in the cathodes of the parallel tubes act as bias resistors. Should any one tube tend to conduct more than the other, the increased current flow in this tube would cause an increased voltage drop across its 10-ohm resistor. The increased drop tends to bias this tube somewhat more than the others. The series-parallel combination of J diodes and 20-ohm resistors, in the cathode circuit, is used to maintain the bottom of the 10-ohm resistors slightly below ground level when the current drivers are not conducting.

Because of the low plate circuit impedance, the plate swing does not vary too far from + 270 volts. The current pulse (about 600 ma) is measured by floating the oscilloscope across a 2.7-ohm resistor that terminates the ring core line. The pulse in question should be about 1.6 volts in amplitude (measured across resistor).

2.04.17 Read Amplifier Core (AR_C)

This component is assigned to the 760 Control and Storage Unit (section 2.00.00, Book D).

2.04.18 Current Driver Core (CD_C)

This component is assigned to the 760 Control and Storage Unit (section 2.00.00, Book D).

2.04.19 Current Driver Matrix (CD_M)

This component is assigned to the 760 High-Speed Wire Printer Control Unit (section 3.03.01, Book D).

2.04.20 Buffer Amplifier (BA_M)

The buffer amplifier (BA_M) (Figure C48) is the core line amplifier used in the punch/printer row memory outputs. Its operation is the same as the BA_R with the pulse transformer wired to invert the input pulse.

2.04.21 Ring Prime Current Driver (CD_P)

This component is assigned to the 774 Tape Data Selector (section 3.00.00, Book D).

2.04.22 Switch Core Write Drivers (Figure C48A)

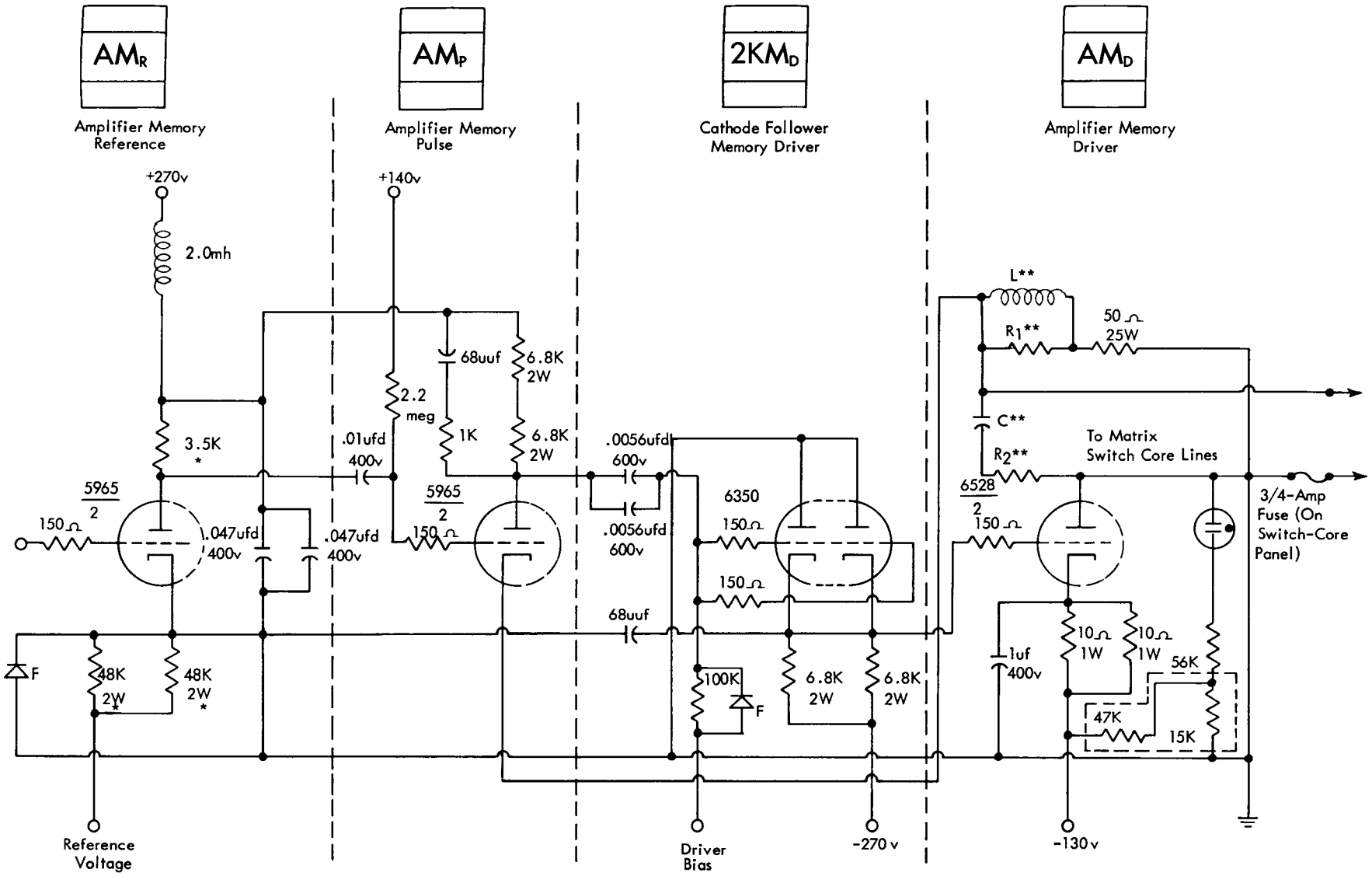
The switch core write drivers serve two purposes:
1. To supply a constant write current pulse to the switch cores.
2. To supply a constant read bias current pulse of somewhat greater amplitude to the switch cores.

When the switch core write driver provides write current, the input to the AM_R comes from AND circuits and cathode followers. When the write gate is up, the input pulse to the AM_R rises from about -25 volts to ground. This causes the switch core driving circuits to supply a constant pulse of current to the switch cores in the plate circuit of the AM_D. The AM_D plate load impedance is determined by the number of switch cores being driven.

Consider the case where the write pulse is required for read biasing of the switch cores. This pulse must be 10 percent greater than for write biasing. This is done by raising the up-level of the input pulse to about +14 volts. The +14v level is provided by a special AND circuit (Systems page 12.05.02). With the increased input level, the switch-core write drivers now provide a larger current pulse. Thus, the switch core write driver is used to provide two different current pulses by varying the input pulse voltage.

Basically, the first stage (the AM_R) generates a constant amplitude voltage pulse. This reference voltage pulse is fed to the second stage AM_P grid. The last three stages (AM_P, $2KM_D$, and AM_D) are a self-regulating amplifier because 100 percent voltage feedback is employed from the AM_D output to the cathode of the AM_P. The feedback insures stability and regulation. Over-all gain of the last three stages is about 0.9.

Quiescent State. Consider the driver in the non-conducting state. At this time, the first stage (AM_R) is cut off. The grid input is at -30 volts while the cathode is clamped to ground. Conduction now occurs from the negative reference voltage through the 48K parallel resistors and the diode to ground. The ground clamp loads the reference voltage supply when the driver is not conducting, thus insuring better reference voltage regulation. RC-coupling is used between the AM_R and AM_P. The AM_P is conducting because the plate connects to +270 volts and the cathode returns



* 1/2% Precision-Type Resistors

	L	C	R1	R2
** Memory Write Driver	10uh	220uuf	82Ω	1.5K
Storage Write Driver	5uh	47uuf	47Ω	510Ω

FIGURE C48A. SWITCH CORE WRITE DRIVER

through the 50-ohm resistor to ground. Grid current flows through the 2.2 meg resistor to +140 volts maintaining the grid only slightly above ground. RC-coupling is also used between the AM_P and the cathode followers ($2KM_D$). The $2KM_D$ grids are biased at -180 volts. DC-restoring is provided by the 100K and the F type diode to prevent the grid from dropping below -180 volts. The $2KM_D$ output (now at -180 volts) couples directly to the AM_D grids. The AM_D cathode is decoupled through five ohms and one ufd to -130 volts. Thus, the AM_D is cut off and load current cannot flow.

Conducting State. Current flows through the write primary winding when the driver input is up. The input signal to the AM_R rises to ground level. Conduction starts in the AM_R because it operates at -4.5v bias. This results in a -22v shift at the AM_R plate. The minus shift is AC-coupled to the grid of the AM_P. However, the time constant for the RC network (2.2 meg and .01 ufd) is 22 ms. This is effective DC-coupling for a pulse only several usec in duration.

Dropping of the AM_P grid causes its plate to rise from +94 to +138 volts. This positive shift is coupled to the $2KM_D$ grid, shifting it from -178 to -134 volts.

The $2KM_D$ output shifts a similar amount and raises the AM_D grids to about -134 volts. The AM_D conducts, supplying current to the switch core winding. Current flow is from -130 volts, through the AM_D, switch core write winding, and the 50-ohm precision resistor (R1) to ground. The drop at R1 is about 19 volts. This voltage is fed back to the cathode of the AM_P.

The voltage values in the preceding text are nominal and may vary from one machine to another. See Systems page 1X.13, sheets 1 and 2, for wave forms.

Regulation. Any change is the current pulse is automatically corrected. The grid of the AM_P remains relatively fixed. Any change in cathode voltage at the AM_P stage is reflected to the grids of the AM_D. Assume that the current pulse is decreased. This causes the feedback voltage to go more positive, reducing conduction in the AM_P. The AM_P output shifts positive. The positive shift goes through the $2KM_D$ to the AM_D grids. More conduction results through the AM_D, correcting the reduced current flow. The reverse condition holds true if the current pulse increases.

There is capacitive feedback from the cathode of the $2KM_D$ to the cathode of the AM_R. Thus, as the cathode of the $2KM_D$ swings positive with the positive input pulse, the cathode of the AM_R swings positive, to offset the grid rise and add more stability.

As stated previously, the reference voltage is variable through a special variable supply. This voltage is common to all drivers, thus helping to insure that there are equal current pulses. The -180v bias supply is also variable but it is supplied from a cathode follower with a variable input. A voltage regulator tube maintains a stable input voltage to this cathode follower supply.

The one microfarad capacitor in the cathode of the AM_D aids current flow as the tube starts to conduct.

Reference Voltage. The cathode of the first stage (AM_R) is returned through two parallel 48K precision resistors to a reference voltage. The reference voltage is a special variable supply. Varying this supply is the means used to vary the output current from the driver.

Consider increasing the reference voltage from -140 to -144 volts. The AM_R conducts more heavily because of the slightly different load line, more drop occurs across the AM_R plate load resistor, and the increased shift is felt through the driver. A larger current pulse than required is now supplied to the switch core winding. The driver regulates to the larger current pulse. Varying the reference voltage varies the voltage on the AM_R plate and, hence, the current pulse.

Marginal checking is done by varying the reference voltage. This procedure is completely outlined in the machine acceptance specifications.

Each driver load circuit is separately fused to protect the circuit. The fuses are mounted on the wiring side of the switch core matrix panels. Each driver load circuit also has a neon to indicate an open circuit.

2.04.23 Switch Core Read Drivers (Figure C48B)

The switch core read drivers supply a constant current pulse to the primary read-winding of the switch cores equal to the write current pulse of the write drivers.

The operation of this circuit is indentical to that of the write drivers, except that the load impedance of the AM_D has been changed to handle the different load.

2.04.24 Inhibit Winding Drivers (Figure C48C)

The inhibit winding drivers supply constant pulses to the inhibit windings. The circuit is essentially the same as that discussed in section 2.04.22. A three-legged AND circuit feeds the driver. Only one KM_D is needed to drive the AM_D because of the different load requirements.

Since the load on the AM_P is largely inductive, the feedback voltage tends to lag slightly. Any tendency to produce oscillation, which this lag might cause, is decreased by placing a damping resistor directly across the inhibit winding.

As in the other driver circuits, the load, including the damping resistor, is fused to prevent damage. The individual fuses are located on the terminal strips, mounted on the ferrite core array frame. A neon bulb, mounted on the taper pin adapter indicates an open drive line when lit.

2.04.25 Sense Amplifier (Figure C48D)

The sense amplifier for the 705 core memory is composed of two RC-coupled pentode stages feeding a cathode follower. The input to the sense amplifier is a full wave rectifier composed of a pulse transformer and two F diodes (TM_S). The 8000-core memory-plane requires a TM_S for each sense winding (C04.25B) (CPU Systems 12.07).

Circuit Operation. The input winding of the pulse transformer contains 40 turns with a damping resistance across the winding. The damping resistance is two 220-ohm resistors in series with the center tied to ground. The secondary is composed of 320 turns with the center tap grounded through 100 ohms. The two diode plates are tied to the opposite ends of the secondary winding. The diode cathode are tied together, and to ground through 10K, making a full wave rectifier. From this point the full wave rectifier feeds the first stage of the amplifier.

The pulse transformer input winding is connected to the core plane sense winding. Flipping a ferrite core induces a pulse on the sense winding of about 60 to 70 mv. The pulse transformer output amplitude is about 150 mv.

The input to the first stage is diode-clamped to a damping voltage of about 0.5 volt. This clips noise pulses which may be many times the 150 mv amplitude of the signal. Noise pulses run as high as 6 volts (+4 to -2). The recovery of the amplifier from a pulse of this magnitude would be slow enough to interfere with the desired signal.

The screen grids of the pentode stages are decoupled from +140 volts with 200 ohms and paralleled .047 ufd capacitors to ground. The plates are decoupled from +270 volts with a similar device. Both stages use cathode degeneration to limit the current. The pentode stages are RC-coupled and the second stage is diode-clamped to ground. Both stages draw about 6.6 ma plate current. The signal input to the first pentode stage is approximately 150 mv. This causes a 7v negative shift at the AM_{S1} plate. The shift feeds to the input of the second pentode stage. This causes an approximate 45v positive shift at the plate of the second pentode stage. The AM_{S2} output is RC-coupled to the output cathode follower. The grid of this cathode follower is diode-clamped to keep it from going below a bias voltage of approximately -20 volts. The cathode follower output should be a pulse starting from a -20v level and having a minimum amplitude of 40 volts.

The voltages given for the sense amplifier are nominal and may vary with tube life. The minimum allowable sense amplifier output is given in the machine acceptance specification 897038. Wave forms are included in 705 III C. E. Manual of Instruction, Volume I, Book B, Form R23-9401.

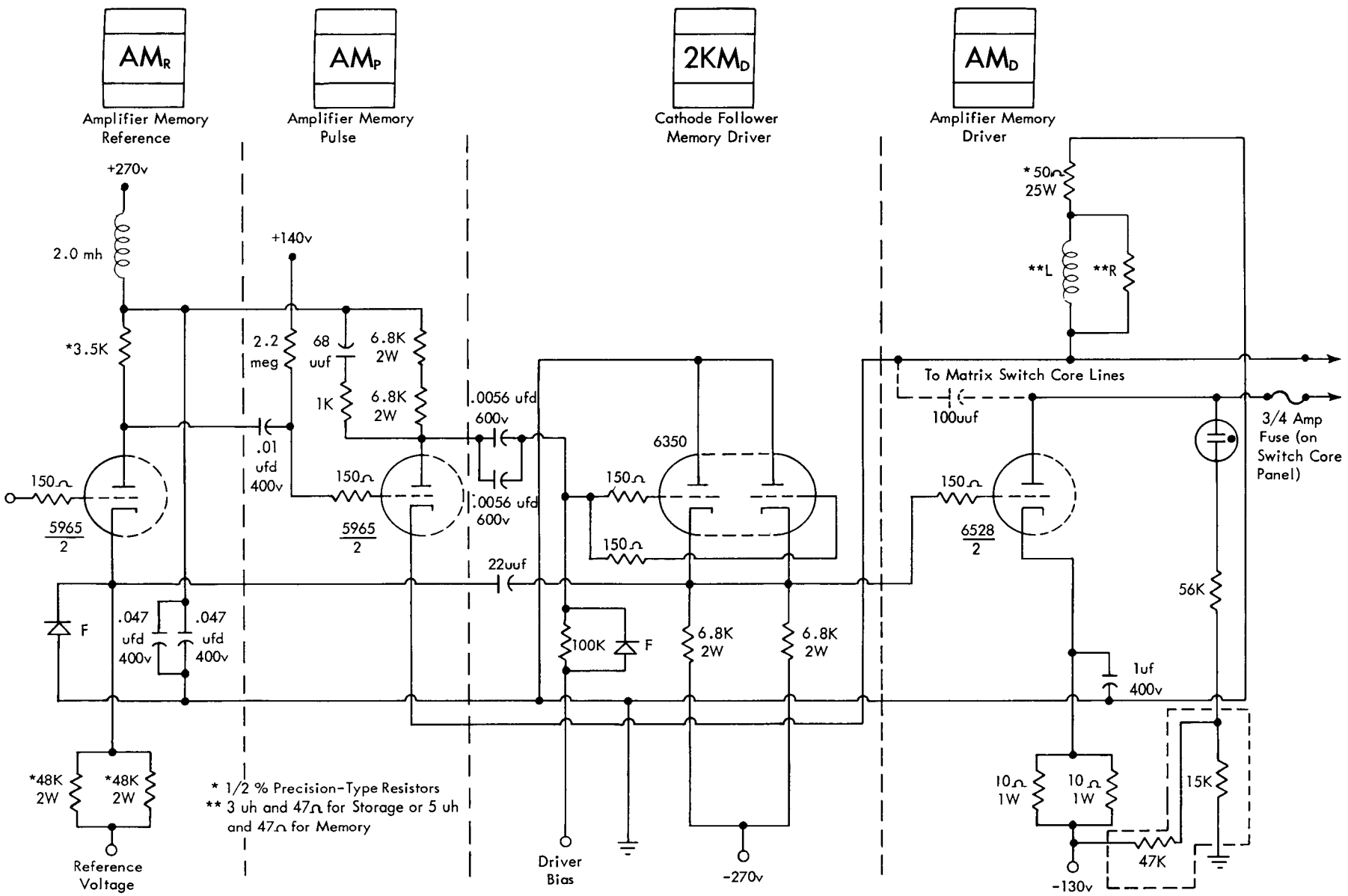
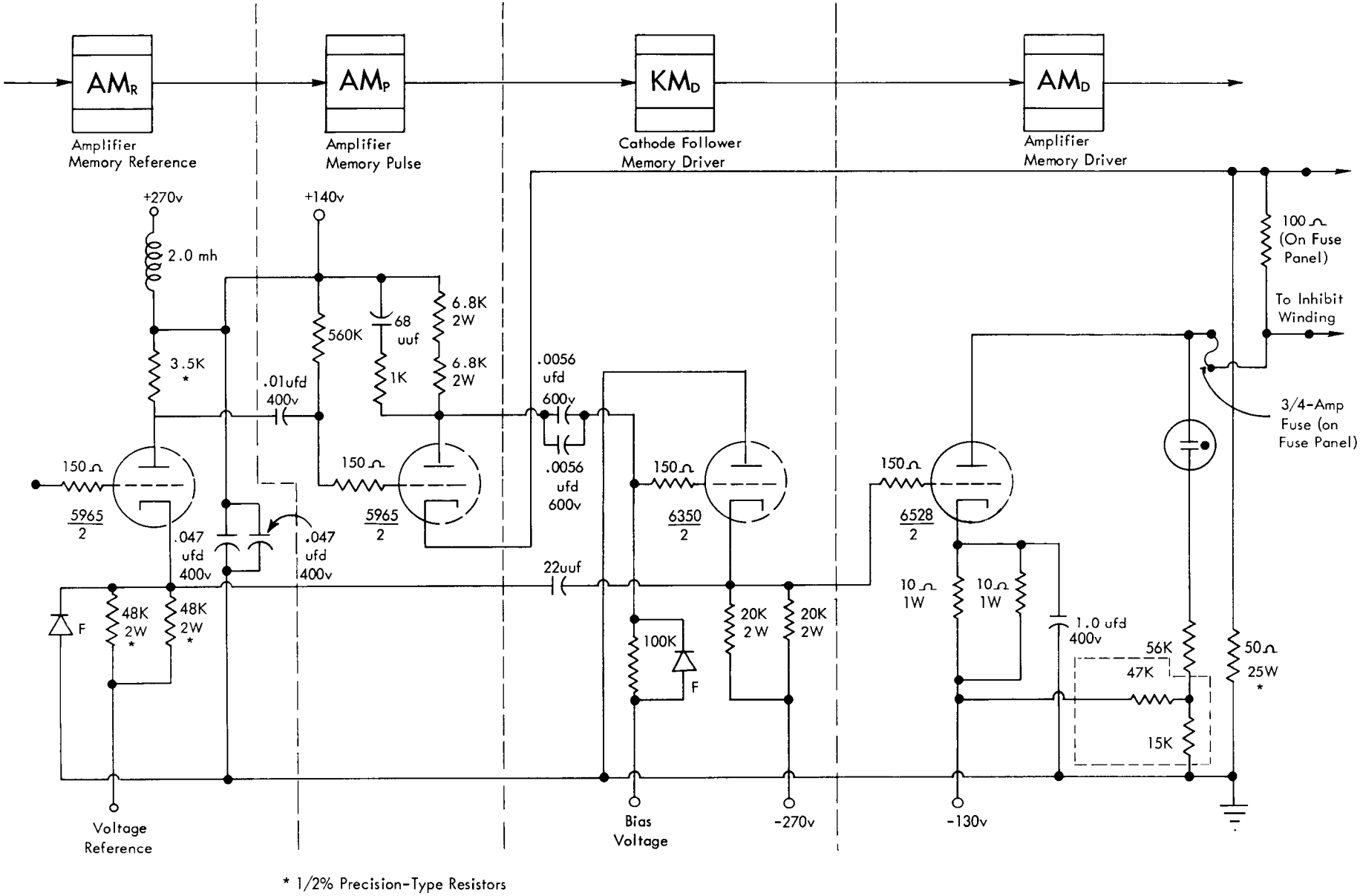


FIGURE C48B. SWITCH CORE READ DRIVER



* 1/2% Precision-Type Resistors

FIGURE C48C. INHIBIT DRIVER

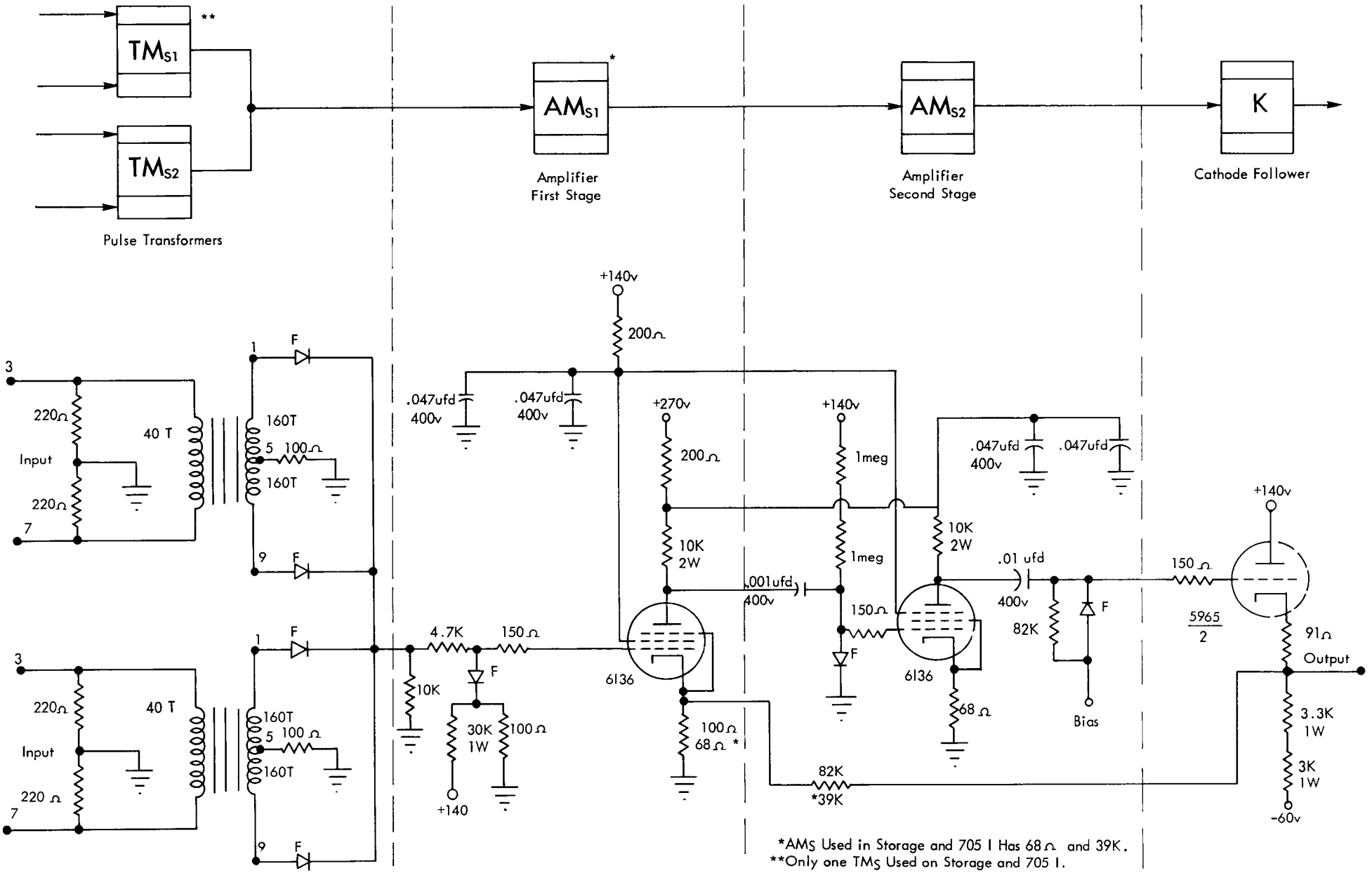


FIGURE C48D. MEMORY SENSE AMPLIFIER

2.04.26 Final Amplifier (I_T, I_{TC}, PS, O, K_J)

The final amplifier (Figure C48E) accepts a 20v peak-to-peak signal from a tape unit pre-amplifier. These signals, read from tape, are amplified, shaped and rectified to produce two separate outputs. These outputs are positive-going, low- and high-clipped inputs to separate read registers.

A nominal 10v input feeds two stages of class A amplification. An integrator circuit in the input suppresses high frequency noise above 7 Kc. A negative feedback from the second stage to the first stage cathode improves the low frequency gain so that the overall gain of the two stages is about 4.5, from 300 cycles to 4 Kc with gain dropping beyond these points.

A phase inverter and following OR circuit produces a 45v positive output for either a positive or negative input. A clipping voltage sets the static base line of the positive pulse. During reading of previously written tape, this clipping voltage is set for 17 volts. During checking of the writing process, the input voltage rises to 11 volts, and the clipping level is reduced by three volts to compensate for the increased amplitude of the input.

The output of the K_J is tapped to provide outputs rising above two different base lines. The cathode output rises 45 volts above a -12v base and the tapped output rises 41 volts above a -20v base for the nominal 10v input. The following components have a fixed input requirement of -5 volts. (See T_{TS}, section 2.02.07, Book C.) Therefore, a weak input signal of 2.5 volts would cause the cathode output of the K_J to rise to -1 volt and set the low-clip read-register trigger. The tapped output would rise to -10 volts but would not set the high clip read-register trigger.

2.04.27 Unassigned

2.04.28 Unassigned

2.04.29 Write-Echo Amplifier (AM_E)

The AM_E (Figure C48F) is used in the 767 Data Synchronizer to convert the 729 III echo pulses (about +8 to -4 volts) from transistor levels to tube levels. The 50v signals (+100v to +50v) of the AM_E output are used to drive a K_G. The circuit uses one half of a 5965 tube.

2.04.30 DS Final Amplifier (Figures C48G and H)

The amplifier is designed to operate with either 729 I or 729 III Magnetic Tape Units.

Input from the model III unit is an 8v peak-to-peak signal from the transistorized line driver. The driver output is loaded by the 1.5K resistor in the grid network of the AM_X. The LC section is used to remove noise from the +12 line. The AM_X is a 2 1/2-times amplifier to bring the model III signals to 20 volts (peak to peak) to match the input signal of the model I. The ground input to the AM_X is connected to the cathode circuit so that the cathode remains at about +8 volts if the model III connector is removed. This keeps the AM_X output at about -30 volts so the K_1 does not clip the model I signals coming into the K_1 cathode output circuit.

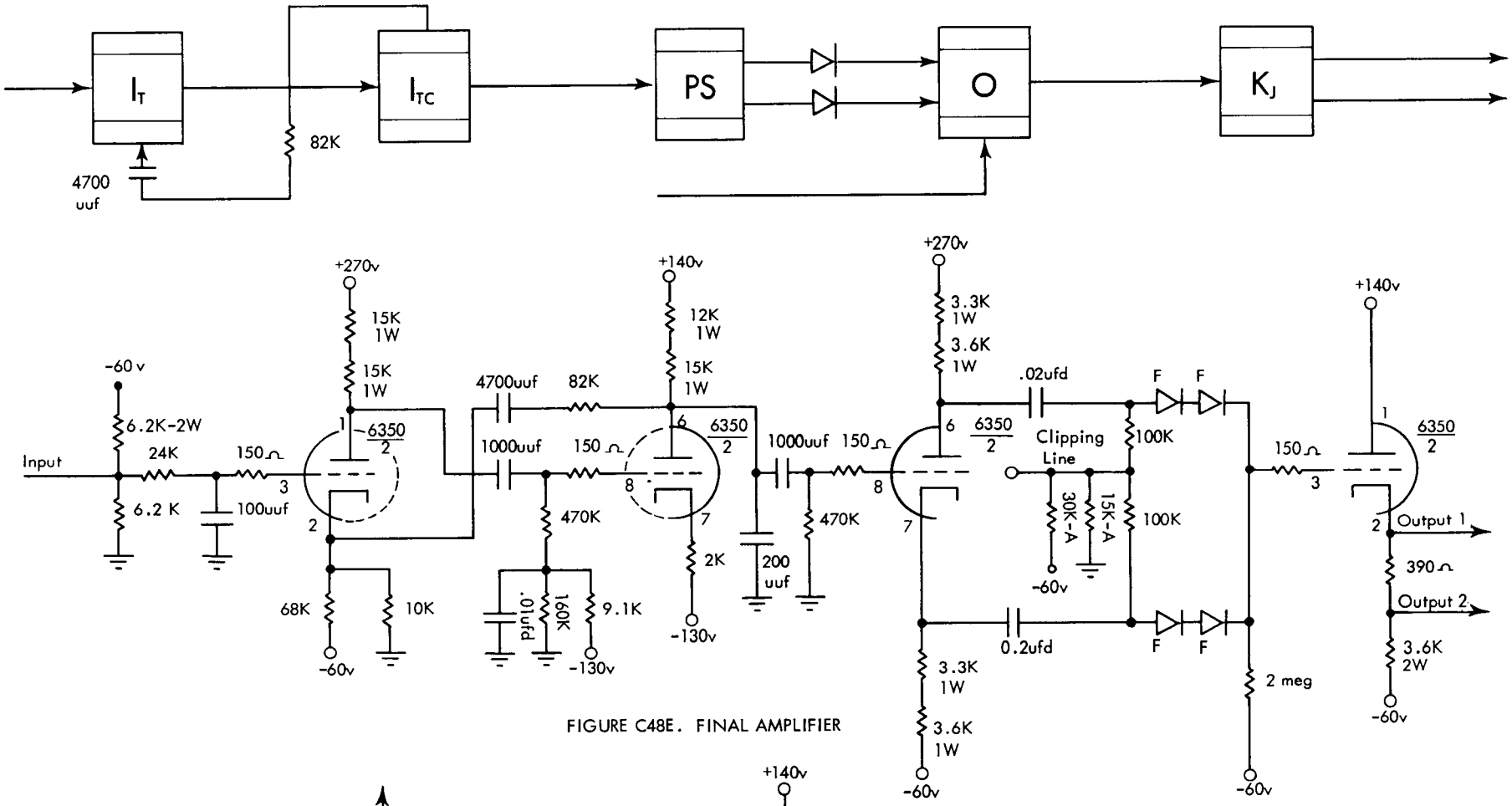


FIGURE C48E. FINAL AMPLIFIER

FIGURE C48F. WRITE ECHO AMPLIFIER -- AM_E

At this point, the model I and model III inputs are OR'ed and fed through a filter. The filter is used as a low-pass circuit; it cuts out everything above 110Kc. Thus, noise to the I_1 is reduced. The signal is powered at I_1 and then fed to the phase splitter (PS) or phase inverter, as it is sometimes called.

The two PS outputs, one from the plate and one from the cathode, are 180° out of phase. When one goes up the other goes down. These outputs are rectified by two full-wave rectifiers called mixers. Thus, the positive-going and negative-going bit signals from tape are both converted to negative-going pulses below ground.

Each rectifier is clipped at a different voltage level. The high-channel clip is set at 4.5 volts; the low, at 11.2 volts. Each clipped output is sent to a separate channel amplifier. The pulses are powered by a cathode follower. The output is fed through a differentiating network.

This differentiating action permits the peaks of the pulses to be sensed at the input to I_2. Thus, the channel amplifier functions as a peak sensing circuit rather than a shift senser. The peaks from the differentiating network (five volts, peak to peak), cause I_2 to cut off. The plate rises rapidly (80 volts, peak to peak). Tube I_3 is forced to cut conduct (normally cut off) and the plate drops. This causes the AM_L plate (normally conducting) to shoot up rapidly. These signals are now square waves with fast rises caused by the AM_L. The AM_L insures that even the weakest peaks, sensed by the channel amplifier after passing the mixer clipping, are given sufficient strength to slip the T_{TS}. The signals are now sent to a cathode follower and out to the T_{TS} input circuits.

The AB diode in the I_2 cathode circuit prevents damage to the 5 ufd capacitor if the tube is removed.

2.10.05 Read Pre-Amplifier (AT_3)

This arbitrarily-assigned number follows section 2.09.06 at the end of Book C.

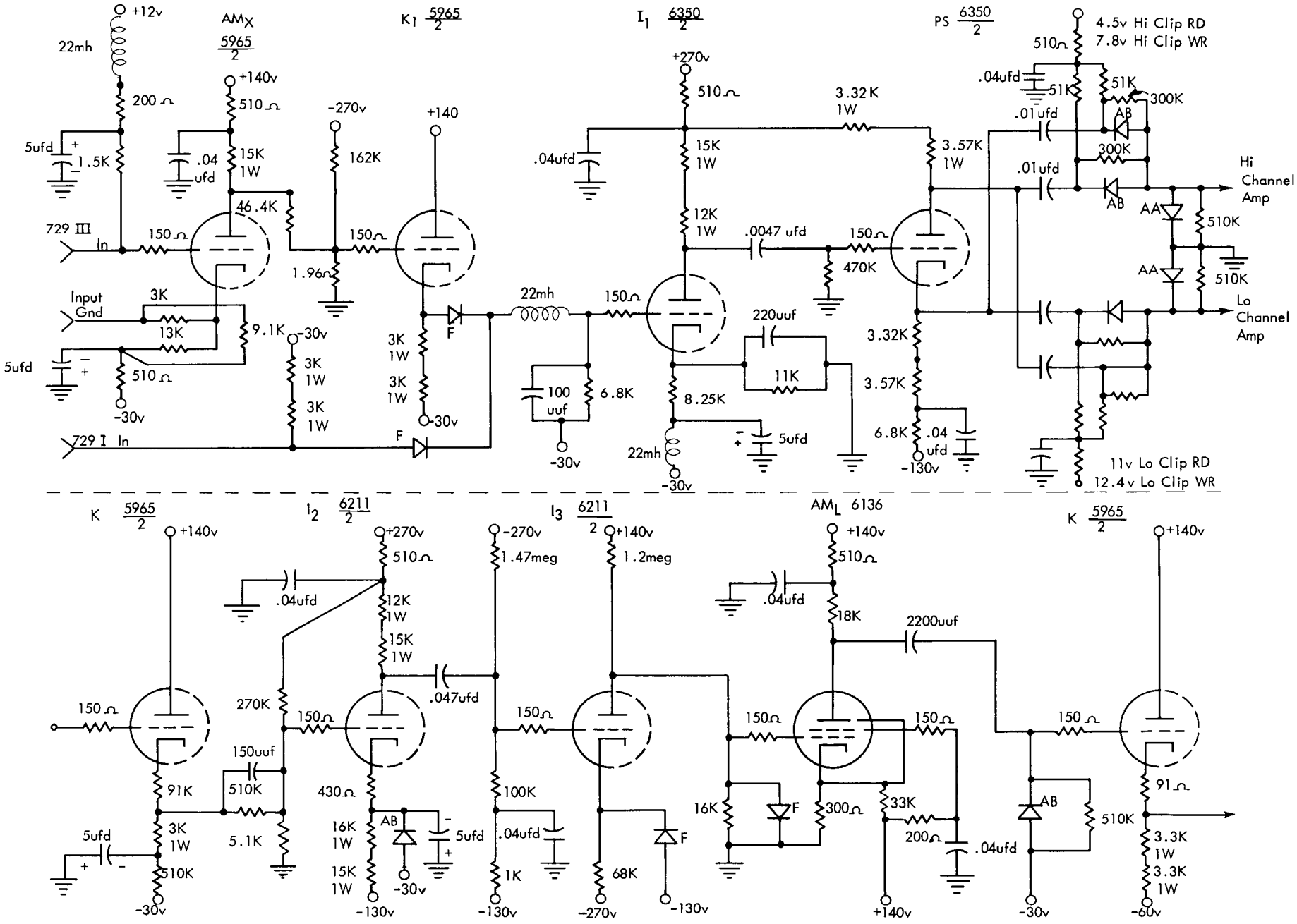


FIGURE C48G. DS FINAL AMPLIFIER (SCHEMATIC)

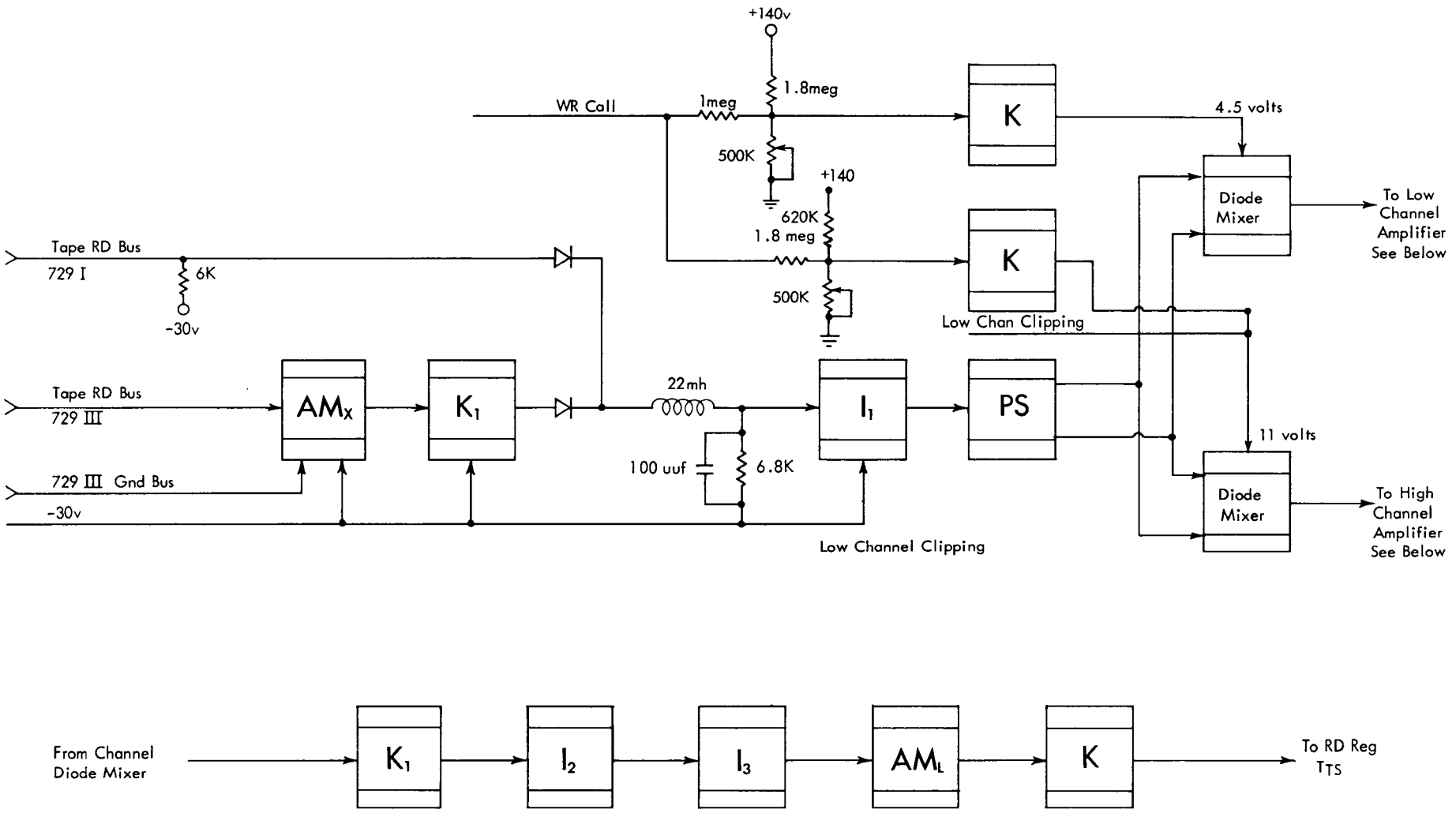
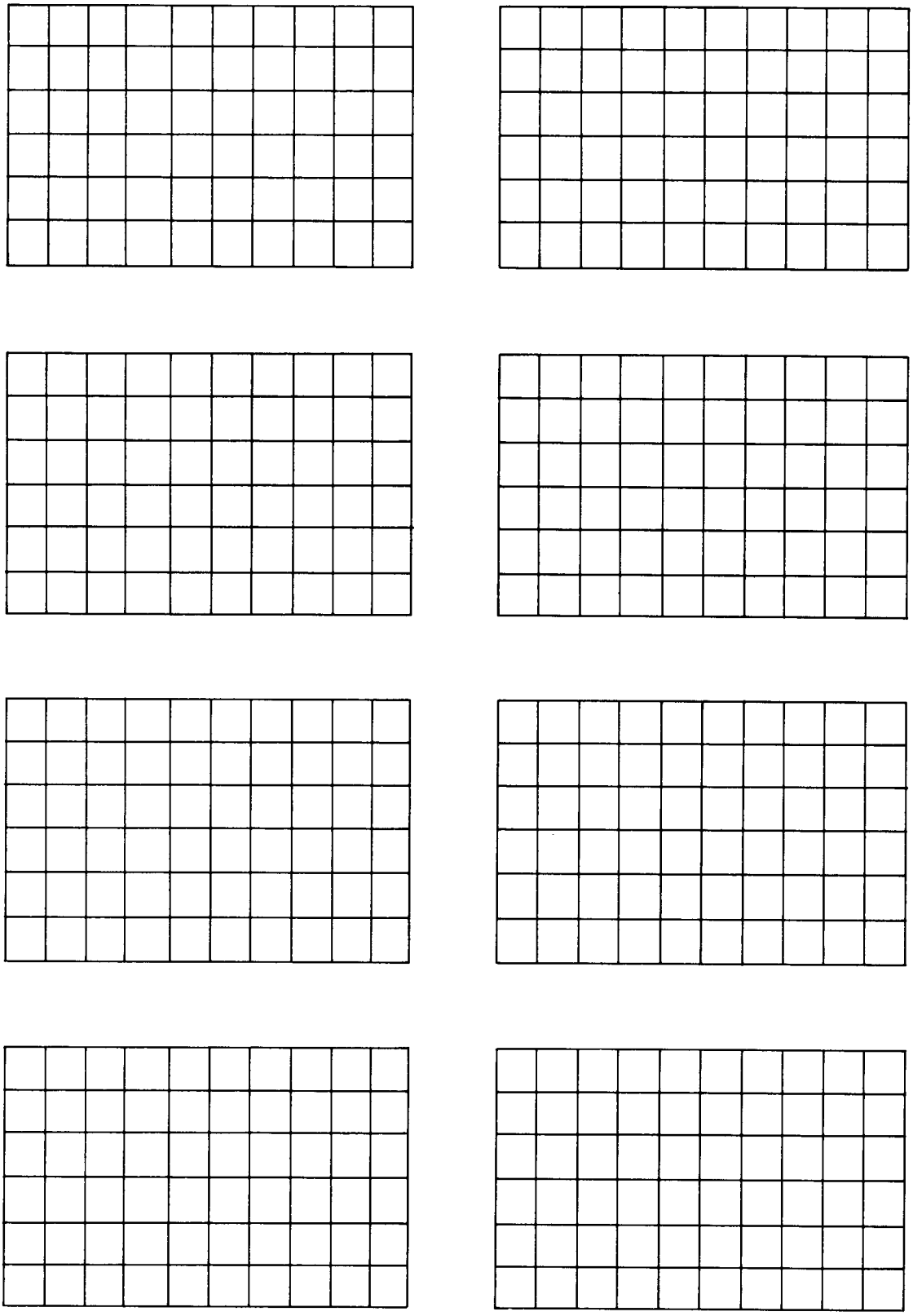


FIGURE C48H. FINAL AMPLIFIER (LOGIC BLOCKS)

NOTES



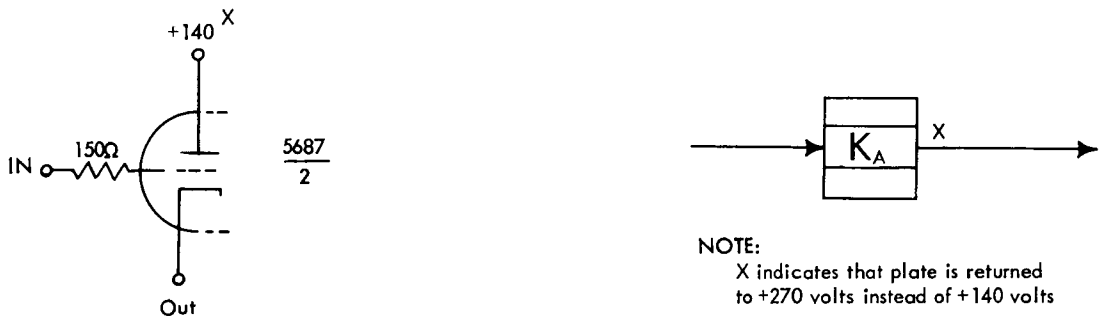


FIGURE C49. POWER CATHODE FOLLOWER -- K_A

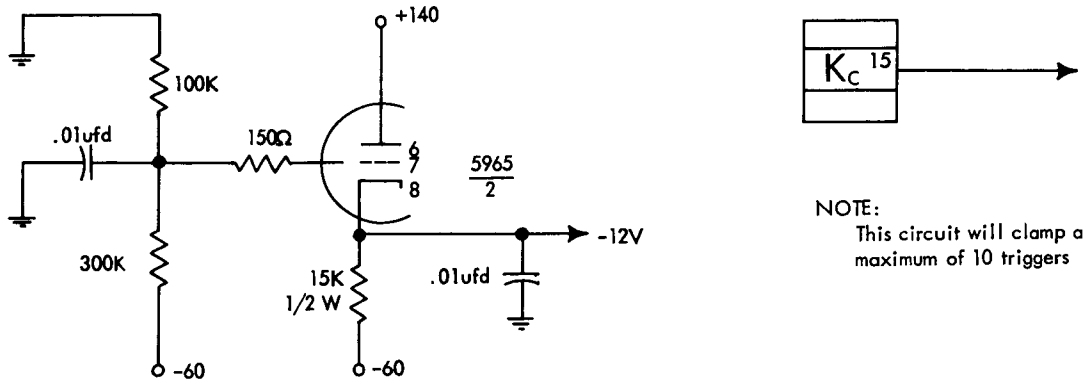


FIGURE C50. CATHODE FOLLOWER CLAMP -- K_C

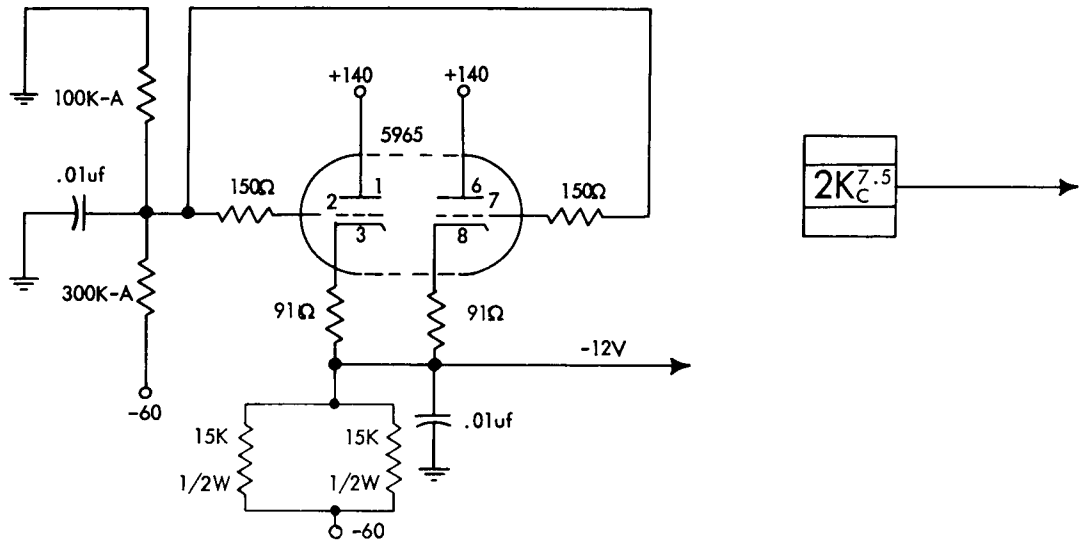


FIGURE C51. CATHODE FOLLOWER CLAMP -- $2K_C$

2.05.00 CATHODE FOLLOWERS

2.05.01 Standard Cathode Follower (K)

The standard cathode follower (K) is described in "Standard Circuits," section 2.09.00, Book A.

2.05.02 Power Cathode Follower (K_B)

The power cathode follower (K_B) is similar to the K_A except that it uses one half of a 5965 instead of one half of a 5687. It can also be returned to +270 volts.

2.05.03 Power Cathode Follower (K_A, K_{A1})

The power cathode follower (K_A) (Figure C49) is a one-half 5687 tube with a plate tied to +140 or +270 volts; the cathode goes to some external load. The load resistor of the K_A is to be shown external to the block, because the block symbol does not imply any load in the pluggable unit position in the block. If the value of the resistor is not shown on the output line of the K_A (indicating that the resistor is in the same pluggable unit position as the K_A), an infinity symbol is to be shown in the K_A block. The value of the cathode resistor is then indicated when the actual location of its cathode resistor appears. The K_A is used in the moving coil circuit in the magnetic tape unit. In this case, the load of the K_A is the moving coil itself and the inverters I_M. A K_{A1} uses a 6350 tube.

2.05.04 Cathode Follower Clamp (K_C)

The cathode follower clamp (K_C) (Figure C50) is used to produce the regulated -12 volts used for clamping trigger grids, and at other points where -12 volts is desired. The divider on the grid input holds the right grid at -15 volts. With this grid voltage, the tube draws 3.2 ma and the drop across the cathode resistor is 48 volts. The output voltage is -12 volts.

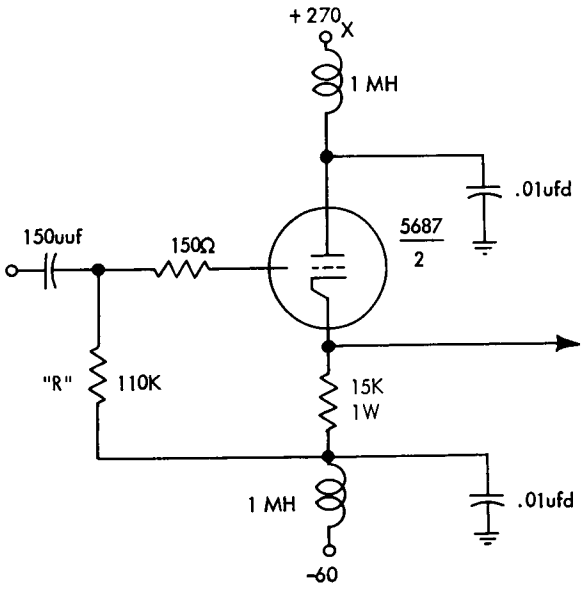
One K_C is designed to clamp a maximum of ten triggers. The clamp voltage changes approximately one volt from no load to full load.

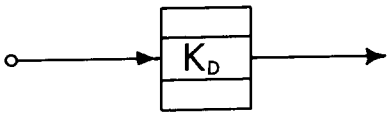
2.05.05 Cathode-Follower Clamp ($2K_C$)

The cathode-follower clamp ($2K_C$) (Figure C51) is used where the load is too great for a K_C (Figure C50). Two half-tubes are used in parallel with 91-ohm load-balancing resistors which insure that both tubes share the load. In this case, each tube draws approximately 3 ma to give the 48v drop across the load resistor, and the output is again a regulated -12 volts. The clamp voltage changes about one volt from no load to full load.

2.05.06 Cathode Follower, Drum (K_D)

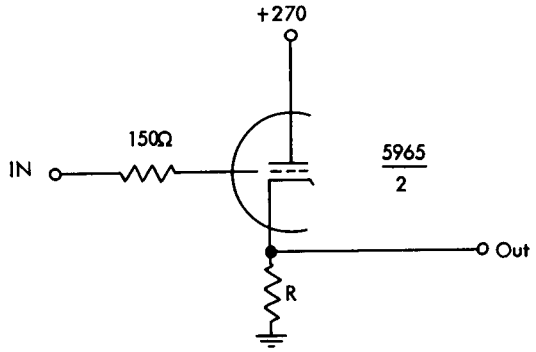
The cathode follower (K_D) (Figure C52) appears in the drum where it is driven either by the peaker PKR_A or the peaker PKR_V. When driven by the PKR_A, the K_D has a +140v plate supply and the grid input resistor R is 33K. In this case an X is shown in the lower right-hand corner of the K_D block on the system and pluggable unit diagrams. The output swings from -50 to +120 volts as the PKR_A pulse is applied to the grid. The grid is initially at -60 volts and the tube is not cut off.





NOTE:
X Plate Supply +140 And
"R" Is 33K

FIGURE C52. CATHODE FOLLOWER (DRUM) -- K_D



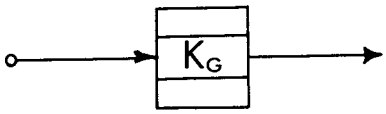
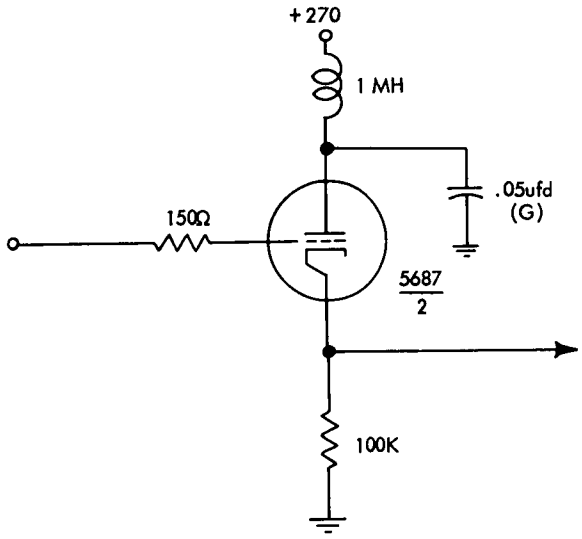


FIGURE C53. PLATE-LEVEL CATHODE FOLLOWER -- K_G



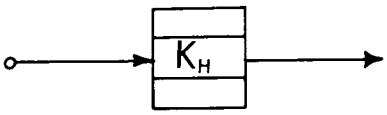


FIGURE C54. CATHODE FOLLOWER (DRUM HEAD) -- K_H

When driven by a PKR_V, the K_D will be as shown in Figure C52, with a +270v plate supply and a 110K grid input resistor. The output swings from -40 to +140 volts as the PKR_V pulse is applied to the grid. There is a slight negative overshoot on the output line as the input goes negative. The grid is also initially at -60 volts and the tube is not cut off.

2.05.07 Deflection Power Cathode Follower (K_E)

This component was assigned to 702 electrostatic memory and is not used now.

2.05.08 Plate-Level Cathode Follower (K_G)

The plate-level cathode follower (K_G) (Figure C53) is us d to power plate or tap level signals. The minimum value of cathode resistor R is 12K-3W. This is the value necessary to insure that the maximum-allowable plate dissipation of one-half of a 5965 (1.67 watts) is not exceeded. The operation of the circuit is the same as that of the standard cathode follower K with the exception that the voltage swing is larger. When K_G's are paralleled, 91-ohm resistors will be placed in the cathode circuits to insure equal sharing of the load between tubes.

2.05.09 Cathode Follower, Drum Head (K_H)

The cathode follower (K_H) (Figure C54) is used in the drum write circuit. The input pulses to the K_H are peaked pulses from cathode follower K_D. These pulses have an amplitude of about +180 volts, and are about 1.2 microseconds in duration. The output of the K_H varies from +40 volts to +125 volts as the input varies from around -40 volts toward +140 volts.

The one-millihenry choke and the .05-uf capacitor in the plate circuit of the K_H are for decoupling purposes. These tend to keep variations in the K_H out of the power supply. The output of the K_H goes directly to the plates of the inverter I_A through the read-write coil. Because the inverter I_A draws its plate current through the cathode follower K_H, the currents in this cathode follower are heavy. This, however, is not detrimental because the duty cycle is relatively short. The K_H uses one-half of a 5687 tube. The half-5687 can draw as much as 20 milliamps steady DC current.

2.05.10 Unassigned

2.05.11 Unassigned

2.05.12 Power Cathode Follower (K_P)

The power cathode follower (K_P) (Figure C55) is a cathode follower employing a 5687 tube rather than a 5965. The purpose of this change is to obtain greater power output without going to parallel cathode followers with the danger of parasitic oscillations. The cathode follower K_{PO} is the use of cathode follower K_P with a common cathode resistor for OR circuit operations.

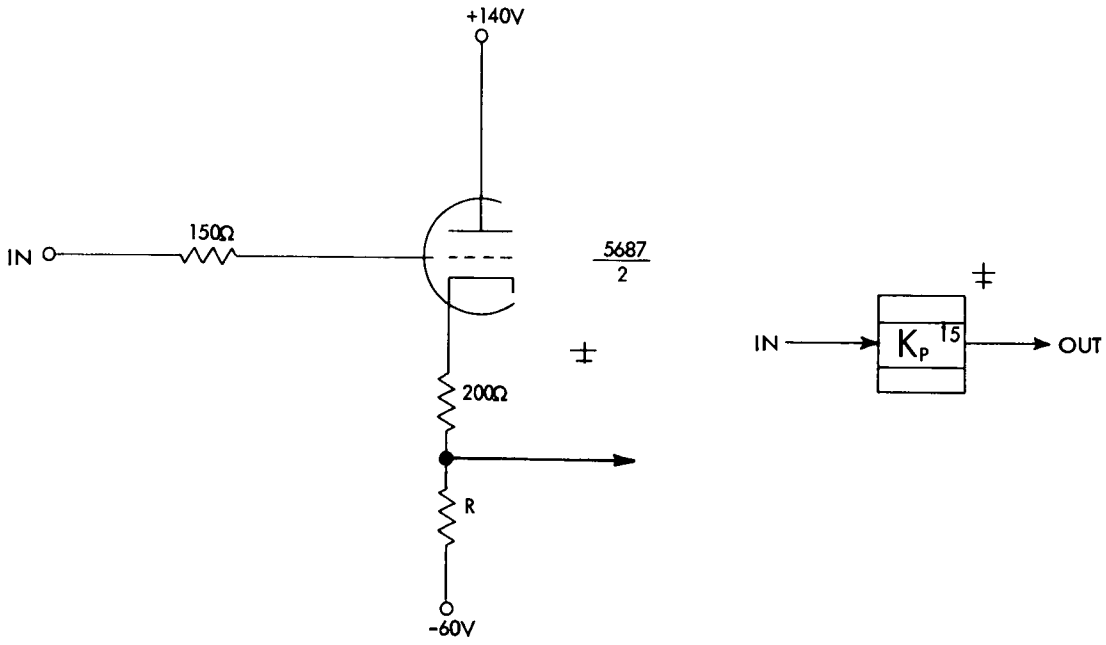
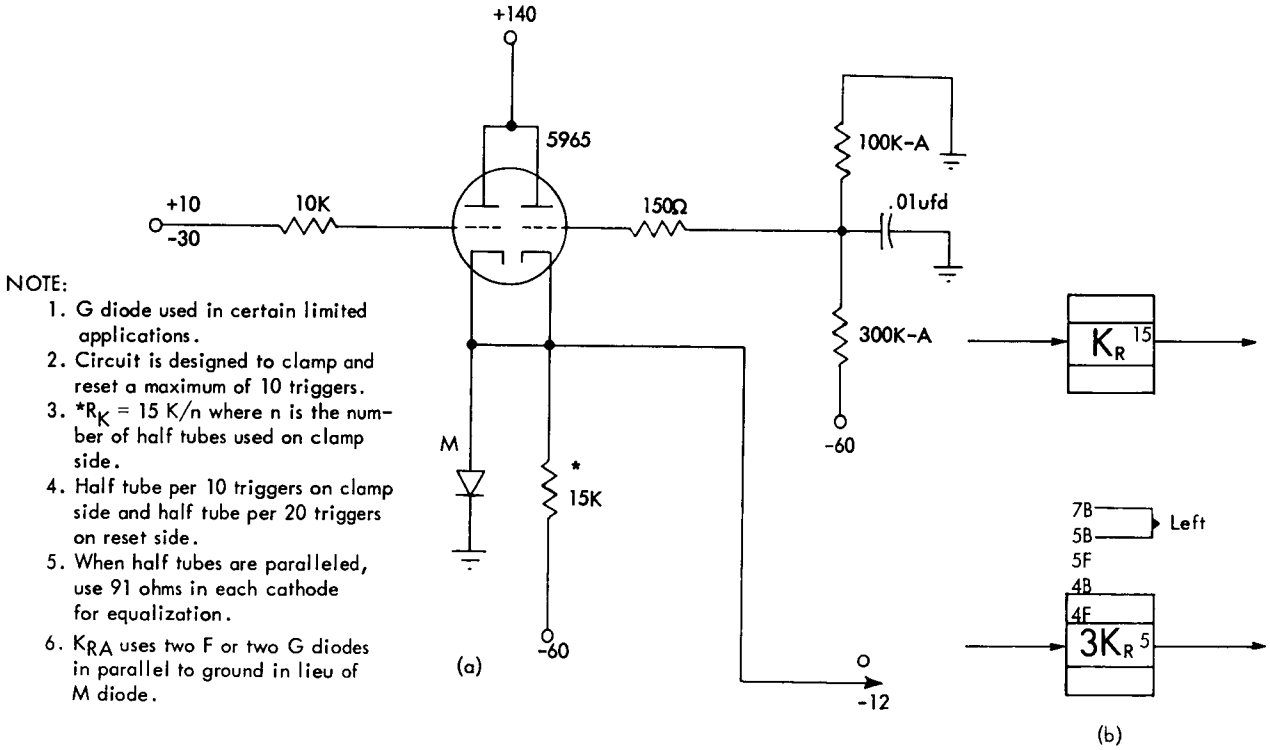


FIGURE C55. POWER CATHODE FOLLOWER -- K_P



NOTE:

1. G diode used in certain limited applications.
2. Circuit is designed to clamp and reset a maximum of 10 triggers.
3. *R_K = 15 K/n where n is the number of half tubes used on clamp side.
4. Half tube per 10 triggers on clamp side and half tube per 20 triggers on reset side.
5. When half tubes are paralleled, use 91 ohms in each cathode for equalization.
6. K_{RA} uses two F or two G diodes in parallel to ground in lieu of M diode.

FIGURE C56. CATHODE FOLLOWER RESET -- K_R

2.05.13 Cathode Follower Reset (K_R)

The cathode follower reset (K_R) (Figure C56) is used to reset triggers on or off. It also serves as a -12v clamp. The output of the K_R is connected to the clamp diode at the on-side grid to reset the trigger on. It is connected to the clamp diode on the off-side grid to reset the trigger off.

The right grid of the K_R is at -15 volts because of the divider on this grid. When the input is down to -30 volts, the left tube is cut off because the right tube is drawing 3.2 ma and the 48v drop across the 15K load resistor brings the cathode up to -12 volts. The left grid, therefore, is 18 volts negative with respect to the cathode. The -12v output serves as a clamping voltage at the trigger to insure that the grid, to which it is connected, drops no lower than -12 volts. When the input is brought up to +10 volts, the cathode comes up as far as ground where it is clamped by the diode to ground. With the cathode at ground, the right tube is cut off because the grid is 15 volts negative with respect to the cathode. The ground potential at the output of the K_R, tied to a grid of a trigger, causes the tube associated with this grid to conduct. The trigger is set on or off as the case may be.

This circuit is designed to clamp and reset a maximum of ten triggers with a change of less than one volt in clamp voltage from no load to full load. The K_R is actually two circuits in one: a clamp circuit, and a reset circuit. Each half has its own load limitations. The right tube (clamp side) can clamp up to ten triggers. This means that the K_R can be tied to 20 trigger grids for clamping purposes because only half that number of grids are at -12 volts at one time. For additional loading, additional half-tubes are paralleled with the right tube.

The left tube (reset side) can reset up to 20 triggers. For additional loading, additional half tubes are paralleled with the left tube. When half-tubes are paralled, either on clamp or reset side, 91-ohm resistors are used in the cathodes for load equalization.

The block symbol used is nK_R where n is the number of half-tubes used for the clamp (right) side as above. Thus the $3K_R$ uses four half-tubes one half for the reset side and three halves for the clamp side. The value of the cathode resistor is determined by the formula $\frac{15K}{n}$ where n has the same meaning as above. For multiple numbers of clamps and resets in the same logic block (Figure C56b), the n states the number of half-tubes used for clamps and the value of R in the logic block is $\frac{15K}{n}$. The reset tubes are identified by a bracket and the word "left."

The duration of the reset condition (up level) should be between 0.5 and 100 usec. The minimum lower level of input should be -20 volts in order to keep the left side cut off.

2.05.14 Resistance Gated Diode Driver (K_S)

The resistance gated diode driver (K_S) (Figure C57) is used to drive one or more diode gates (D_G) directly, or to drive cathode followers (K), which in turn drive diode gates. The value of the resistor R in the right grid bias circuit is determined by the output voltage desired. This value is chosen so that the right grid bias is slightly negative with respect to the desired low-level output voltage. When the incoming signal is +10 volts, the left tube conducts and the right tube is cut off. The output is

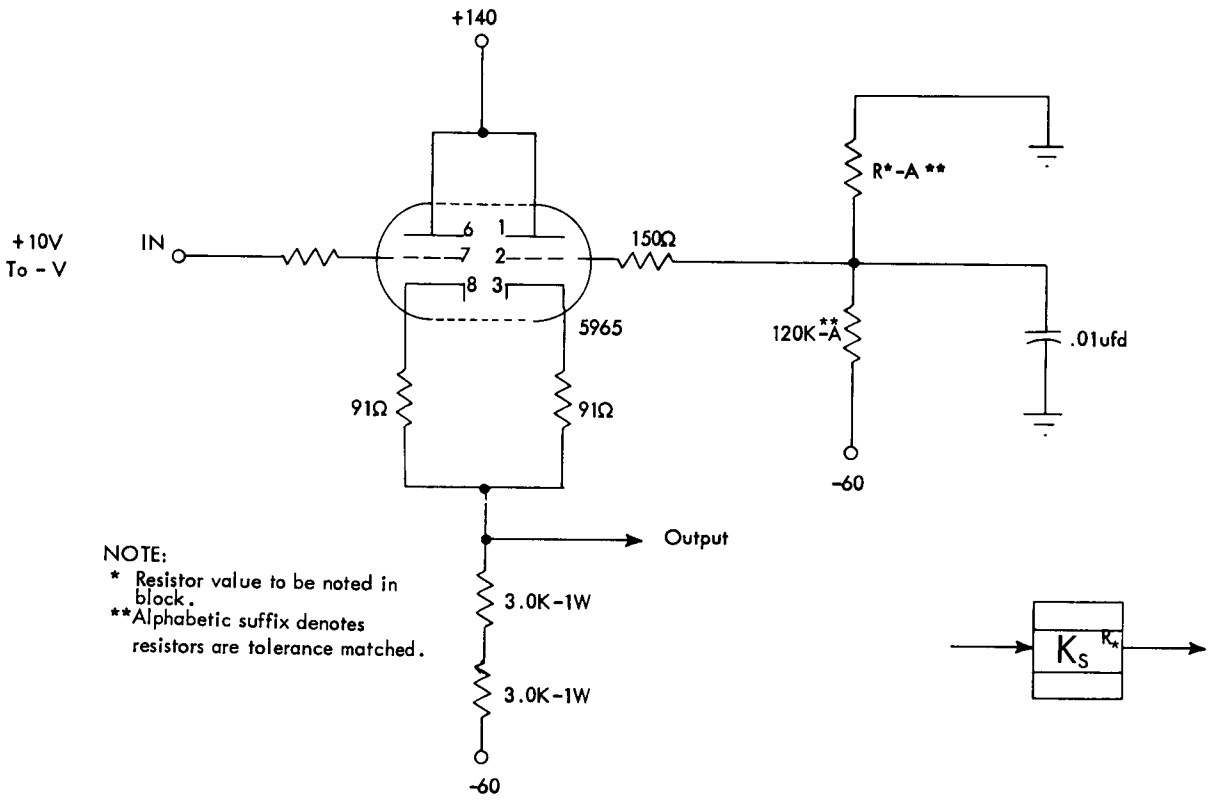


FIGURE C57. RESISTANCE GATED DIODE DRIVER -- K_S

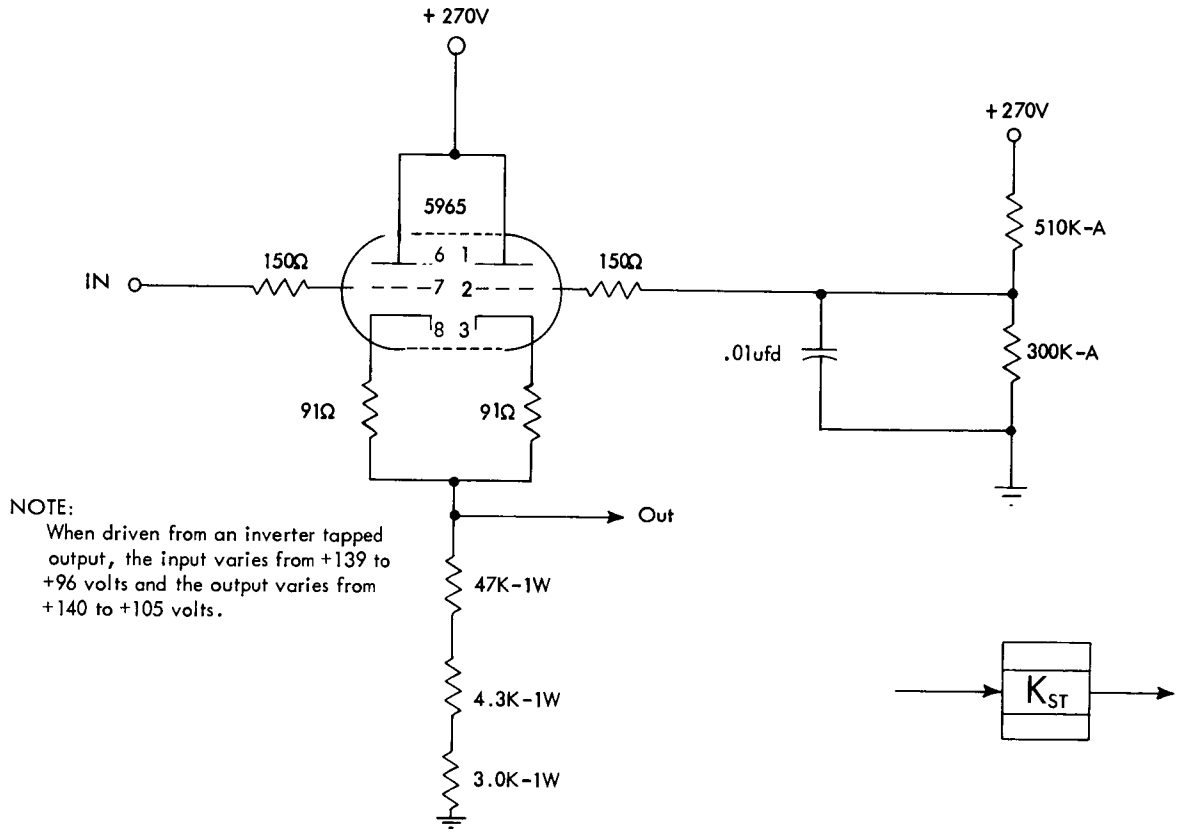


FIGURE C58. RESISTANCE GATED DIODE DRIVER -- K_{ST}

about +10 volts, because the bias on the right side is sufficiently negative to cause cut-off. If, however, the input level drops to at least two volts below the desired lower output level, the left side loses control and the right side conducts to give the desired output value.

The K_S circuit may be driven from a trigger or another cathode follower. The K_S drives five triggers located reasonably close together.

The resistance gated diode driver may have any of the following output levels, depending on the value of resistor R:

R	Lower Output Level
43K (If driving diode gates directly.)	-14 volts
56K (If driving standard K which drives resistance-gated diodes.)	-16.5 volts
62K	-18 volts
75K	-20.5 volts

2.05.15 Resistance Gated Diode Driver, Tap Level (K_{ST})

The resistance gated diode driver (K_{ST}) (Figure C58) operates like the resistance gated diode driver K_S. The principal difference in the two circuits is the level of operation. When the input of the K_{ST} varies from +139 to +96 volts, the output varies from +140 to +105 volts. The K_{ST} is used mainly in the drum where the input is the DC output of a diode gate D_G.

2.05.16 Cathode Follower (K_X) (K_{XO})

The cathode follower (K_X) (Figure C59) is merely a cathode follower employing a 6211 tube rather than the 5965 with a resultant saving in power. The filament current is substantially smaller, and the tube also draws a smaller plate current. The cathode follower K_{XO} is simply the use of cathode followers K_X that have a common cathode resistor for OR circuit operation.

2.05.17 Power Cathode Follower (K_Z), (K_{Z1})

The power cathode follower (K_Z) (Figure C60) is used to power the output of the peakers PKR_Z in the memory wave form generator. The voltage divider at the grid input to the K_Z sets the input at -30 volts in the quiescent state. The input pulses are AC-coupled and drive the cathode follower into conduction. The amplitude of the incoming pulses to the K_Z is 90 volts and better. The output of the K_Z is 40v pulses. The currents in the K_Z may be as high as 100 milliamps per half-tube. These currents are not detrimental to the tube because the duty cycle is very short, considerably less than 10 percent. A K_{Z1} uses a 6350 tube in place of the normal 5687 tube.

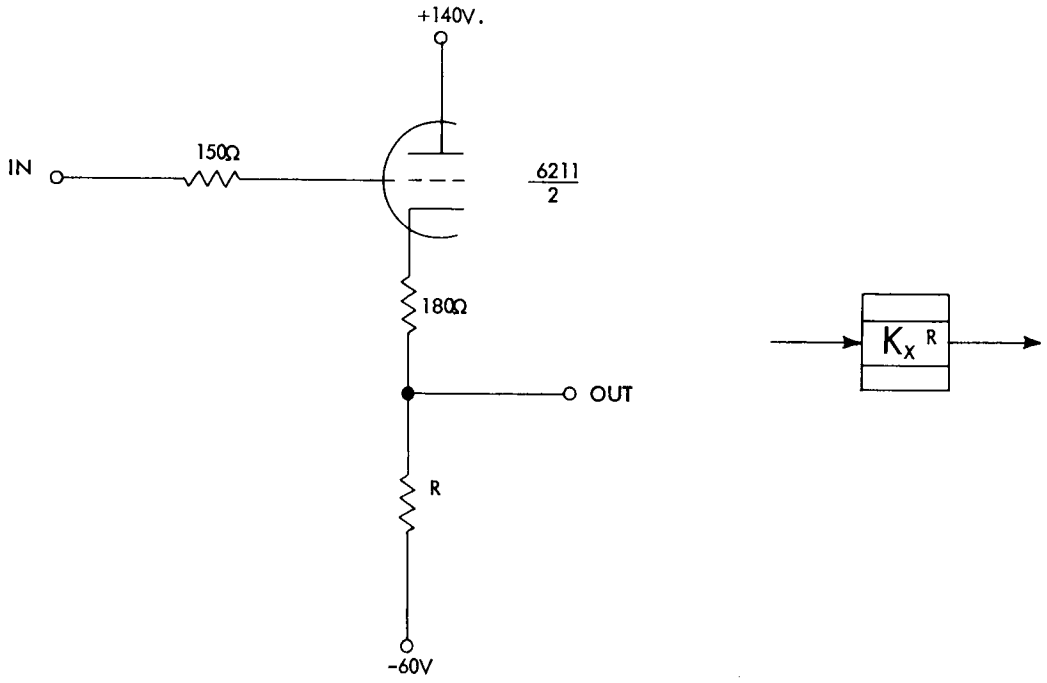


FIGURE C59. CATHODE FOLLOWER -- K_X, K_{XO}

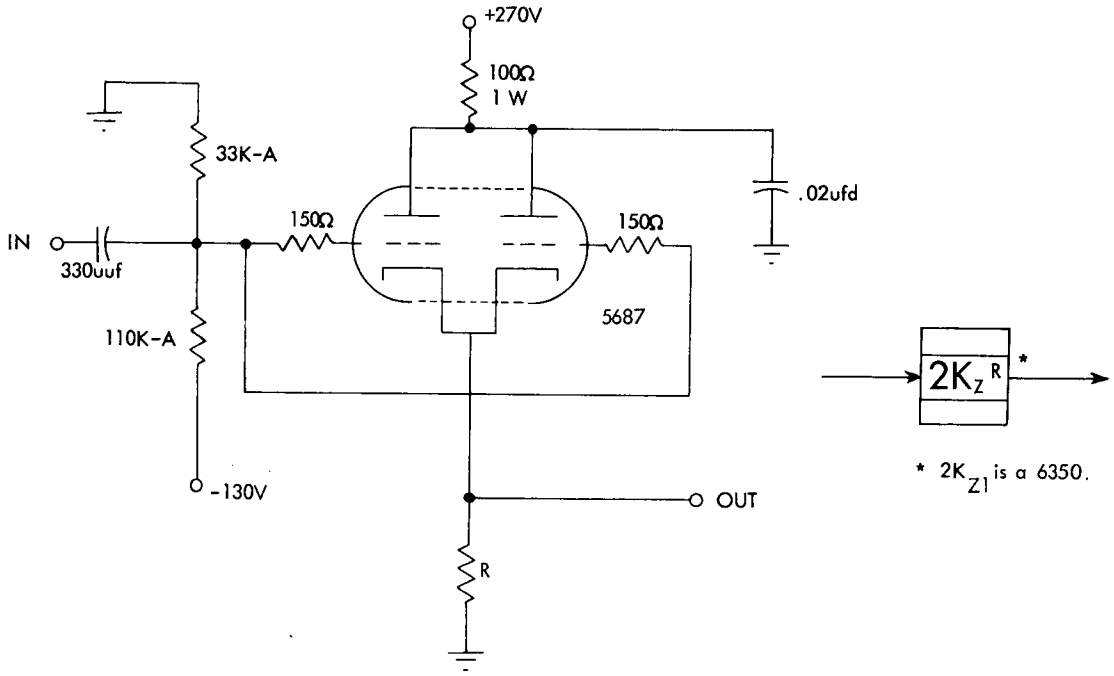


FIGURE C60. POWER CATHODE FOLLOWER -- $2K_Z$

2.05.18 Power Cathode Follower (K_J)

The K_J (Figure C60A) circuit is the same as the KP but uses a 6350 tube in place of the 5687. The 6350 permits driving heavier loads without paralleling the cathode followers. A K_{JO} is one section of a K_J OR circuit.

2.05.19 Pulse-Driving Cathode-Follower (K_{PD})

The K_{PD} (Figure C60B) is a low-impedance high-current source for driving a bank of parallel AND circuits with a sharp, short-duration pulse. In its static condition, the grid of the K_{PD} is biased at -50 volts while the load circuit maintains the cathode at -30 volts. When the input of the driving grounded grid amplifier rises to +10 volts, the tapped output of the GA rises about 75 volts. This causes heavy conduction in the K_{PD} and heavy grid current. The output drives the bank of AND circuits to about +10 volts rapidly and stabilizes at this voltage. When the input voltage drops, the low cathode impedance drops the output voltage rapidly.

Because of the heavy current, the 1000 uuf capacitor differentiates pulses of greater than six usec in duration to protect the 5687 from damage.

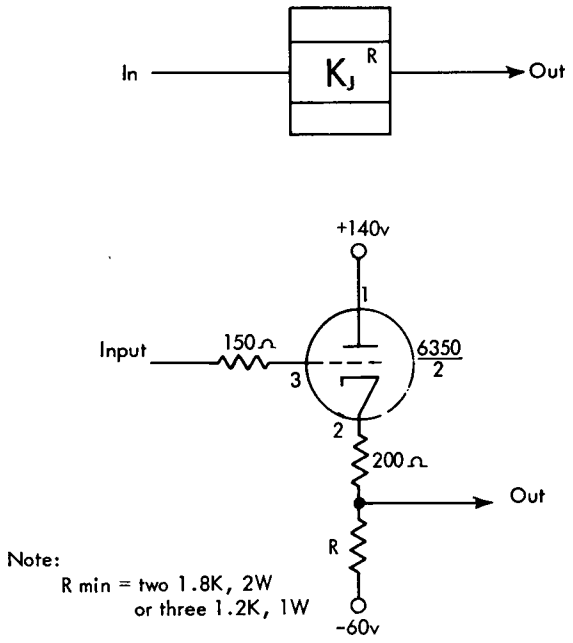
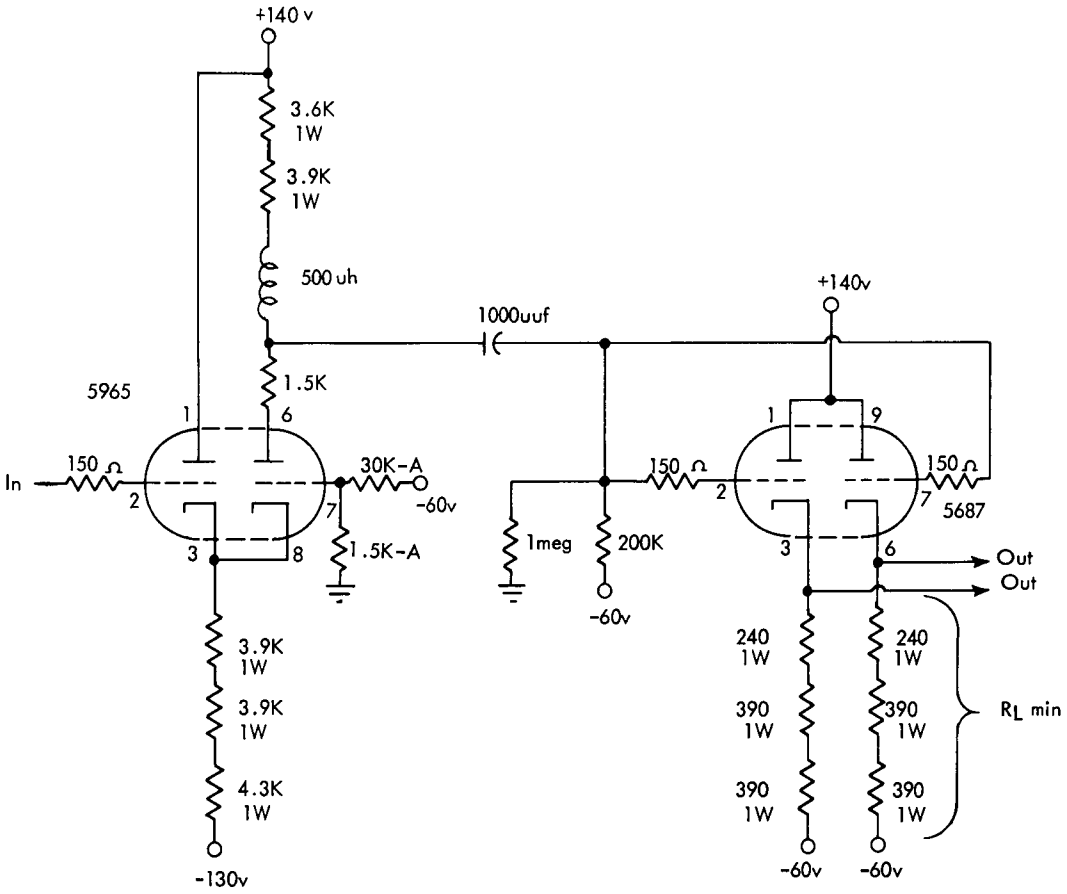
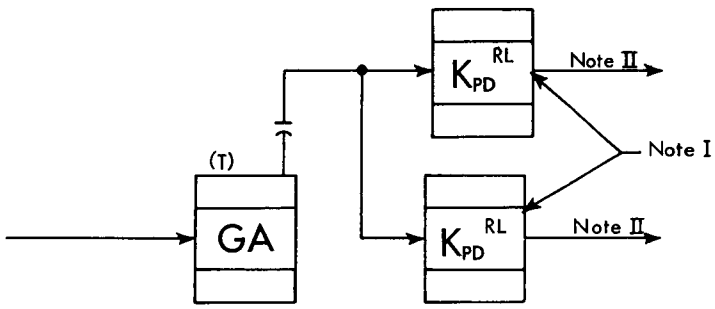


FIGURE C60A. POWER CATHODE FOLLOWER -- K_J





Notes:

I $R_L = \frac{18,360}{N}$

Where N = No. of 100K and ckts to be driven

N max = 18

II With min R_L = 1.02K, each K_{PD} drives eighteen, 100K and ckts

Max pulse width = 6 us

Max duty cycle = 25 %

K_{PD} may not be paralleled

FIGURE C60B. PULSE-DRIVING CATHODE FOLLOWER -- K_{PD}

2.06.00 DIODE CIRCUITS

2.06.01 Plus AND (Minus OR) Circuit

The +AND (-OR) circuit* is described under "Standard Circuits" (section 2.01.00, Book A).

2.06.02 Diode Gate (D_G)

The diode gate (D_G) is described under "Standard Circuits" (section 2.07.00, Book A).

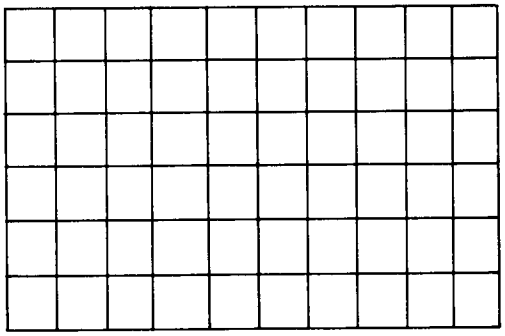
2.06.03 Diode Gate (G_J)

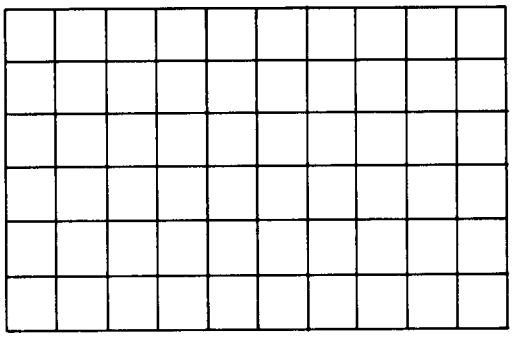
The diode gate (G_J) is described under "Standard Circuits" (section 2.08.00, Book A).

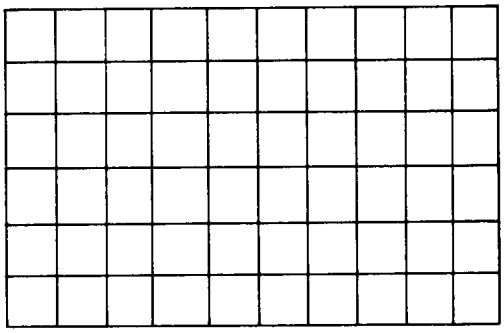
2.06.04 Plus OR (Minus AND) Circuit

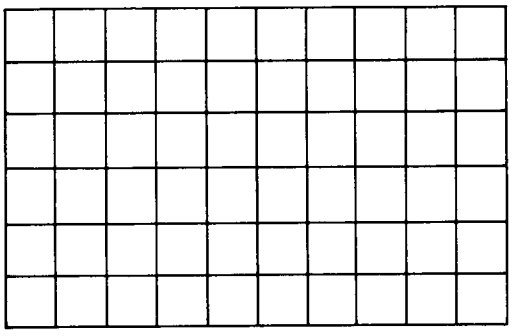
The +OR (-AND) circuit* is described under "Standard Circuits" (section 2.02.00, Book A).

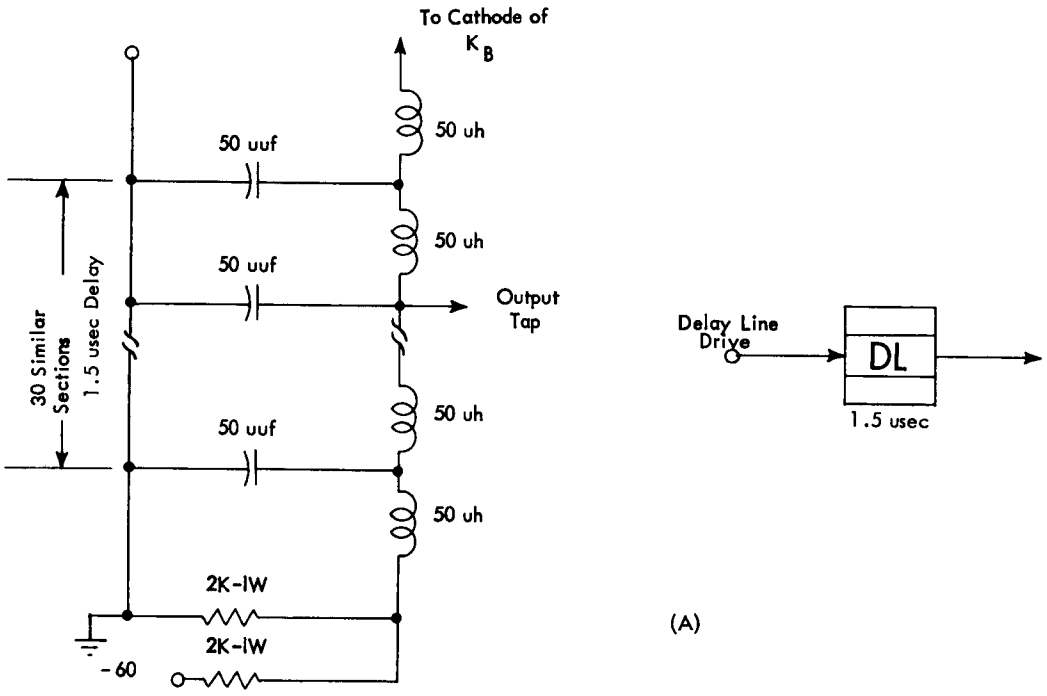
*Cascaded AND/OR circuits are covered under "Standard Circuits" (section 2.04.00, Book A).











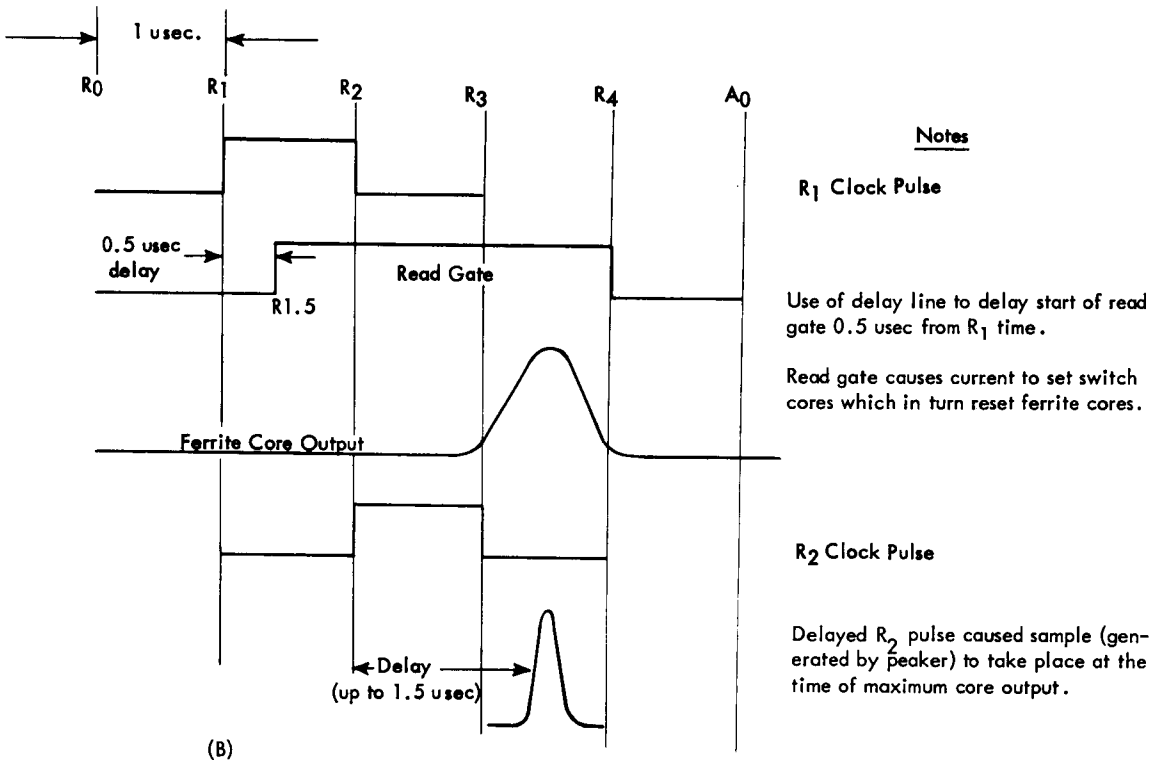


FIGURE C61. 1.5 MICROSECOND DELAY LINE -- DL

2.07.00 DELAY CIRCUITS

A delay circuit can delay a pulse a specified length of time with a minimum of distortion. This type of circuit is useful in computer design to produce precisely-timed sample pulses.

2.07.01 Delay Line (DL)

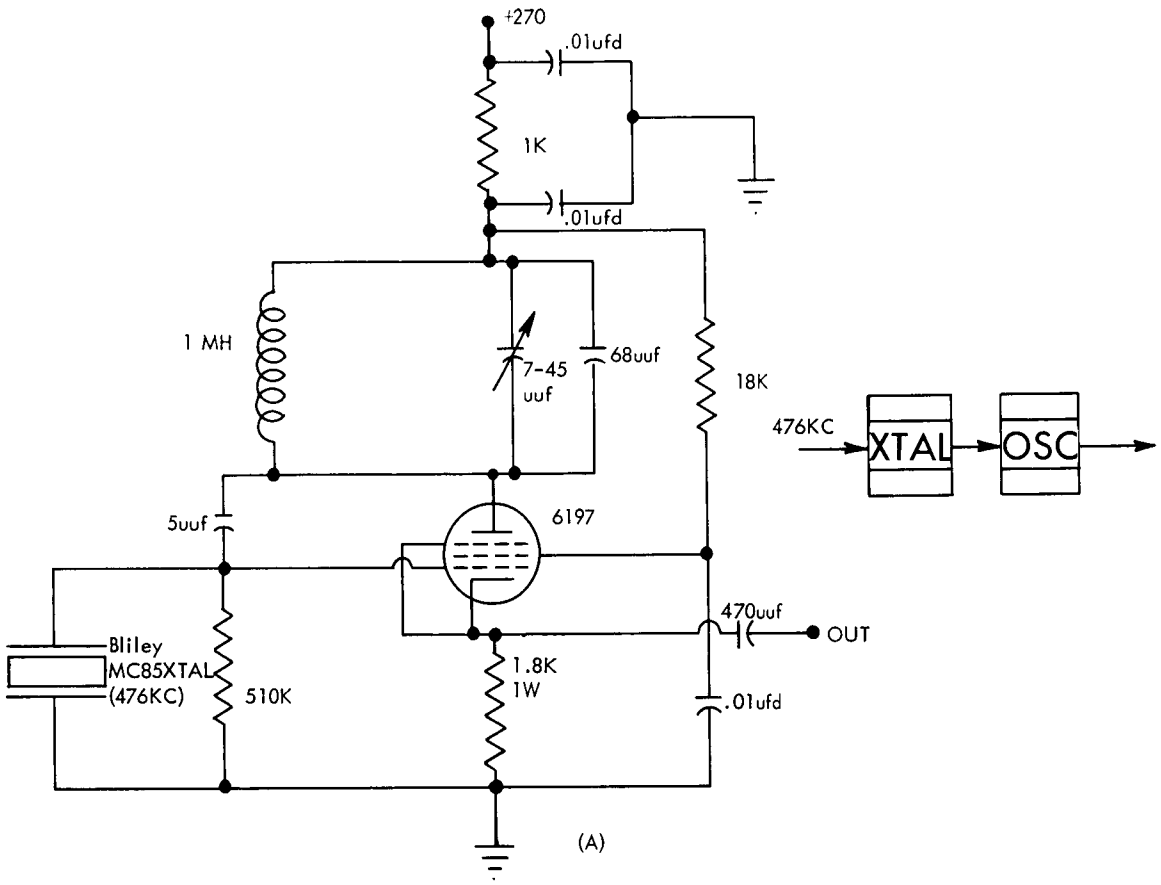
The delay line (DL) (Figure C61) is used in the wave-form generator circuits to delay clock pulses a specified length of time. The delay line contains up to 30 individual sections with each section capable of 0.05-usec delay (square root of LC) for a total of 1.5 usec for the complete circuit. The output can be taken from any section representing the desired amount of delay.

Circuit Description. The input to the delay line is a cathode follower. The delay line circuit is the cathode load for the tube. The LC networks are terminated with their characteristic impedances (the value of impedance that makes the line look infinitely long to prevent pulse "echo") and returned to an effective -30 volts. Characteristic impedance of a delay line is computed as the square root of L over C. In operation, the delay lines make use of the characteristics of coils and capacitors to shift the phase of signals applied to them. Consider the following: A change in voltage is applied at the input terminal to the delay line. Because the charging current to the first capacitor in the delay line must be drawn through the coil, the current will lag the applied voltage because current through the coil lags the voltage across the coil. The voltage developed across the capacitor lags the charging current by a similar amount. This voltage is now applied to the next coil, and so on down the line as the signal is delayed in passing from one section of the network to the next. Signals delayed any desired amount may be tapped off at various places on the delay line.

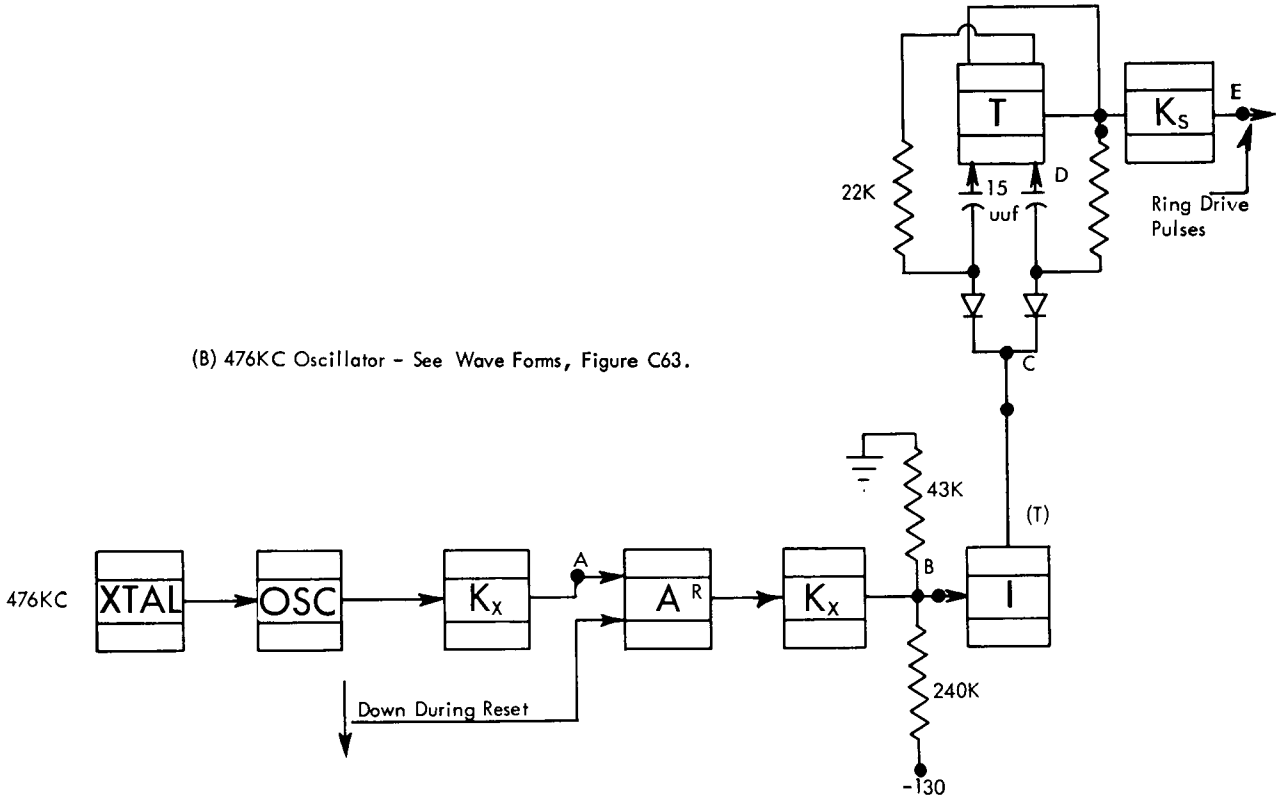
Figure C61b shows a sample usage of delay lines. The sequence shown is a simplified version of core-memory read sampling. The amount of delay varies with each machine: it is adjusted to coincide with maximum core output.

2.07.02 Character Gate Delay Line (DL_A)

The DL_A is used in the 767 DS to time the character gate interval for the 729 III tape operation. It has 54 sections, each having 0.105 usec delay. It uses 500 uh chokes and 22 uuf silver mica capacitors.



NOTE:
This same circuit is used with a 1 MC crystal, a 500uh coil and a 15 uuf capacitor. The load resistor will then be 2.0K - 1W.



(B) 476KC Oscillator - See Wave Forms, Figure C63.

FIGURE C62. OSCILLATOR (CLOCK) -- OSC

2.08.00 PULSE GENERATORS

Pulse generators are self-contained circuits that produce pulses or voltage variations of a fixed frequency. The most commonly used pulse generator is the oscillator.

2.08.01 Bit Sweep Generator (B_G)

This component was assigned to 702 electrostatic memory and is not used now.

2.08.02 476 KC Oscillator for Clock (OSC)

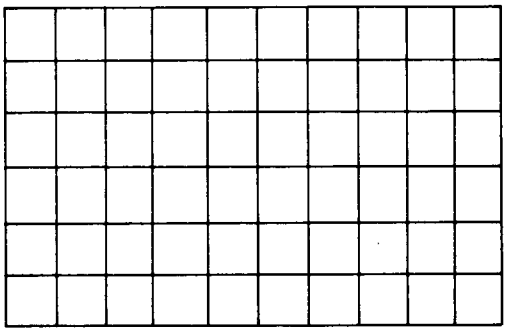
The oscillator (OSC) is described in "Standard Circuits," section 2.13.00, Book A.

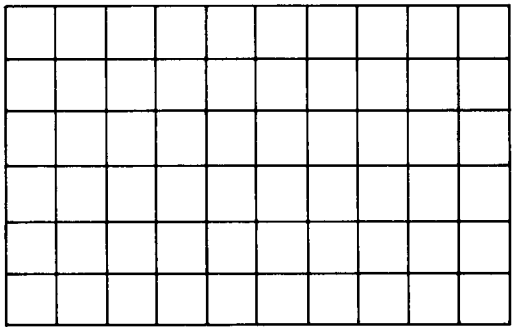
Figure C63 shows typical wave forms taken from a 476KC oscillator shown in Figure C62b. The grid wave form is a nominal 550v peak-to-peak sine wave. The plate wave form is a slightly distorted sine wave with an amplitude of about 550 volts, peak-to-peak. The cathode wave form is a positive peak about 80 volts in amplitude. The negative portions are clipped as the tube is cut off. The cathode voltage drops slightly even after the tube is cut off. This drop is caused by the interelectrode capacitive coupling between grid and cathode. The output of the oscillator consists of positive-going pulses of 0-80 volts occurring once every 2.1 microseconds. The magnitude of the feedback voltage in combination with the cathode bias is such that the tube is overdriven. The result is that the output is not a pure sine wave, but it is distorted on the positive excursion and clipped by the cut-off action of the tube (the negative excursion). The output is taken from the 1.8K cathode resistor which serves both as bias and as part of the load for the circuit. Figure C62b shows the development of ring-drive pulses that drive all control unit clocks. The labeled points refer to Figure C63.

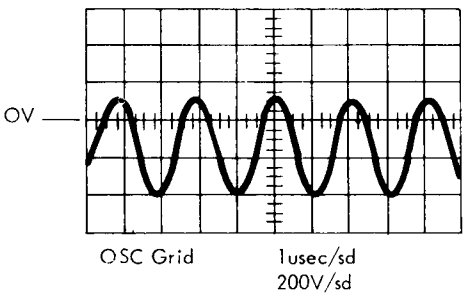
2.08.03 Unassigned

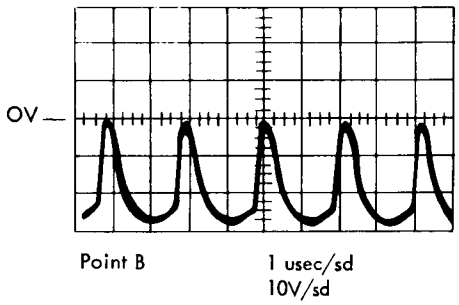
2.08.04 Two-MC Oscillator for Clock (OSC_A)

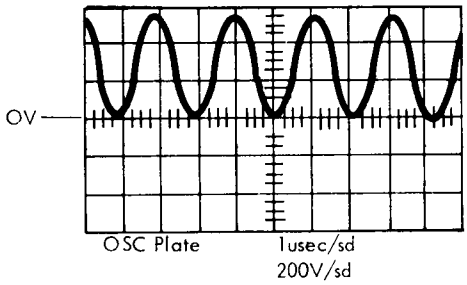
This component is assigned to the 777 Tape Record Coordinator (section 5.02.01, Book D).

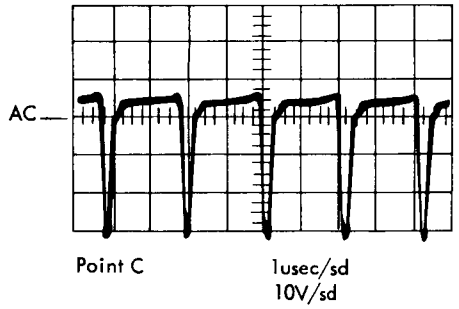


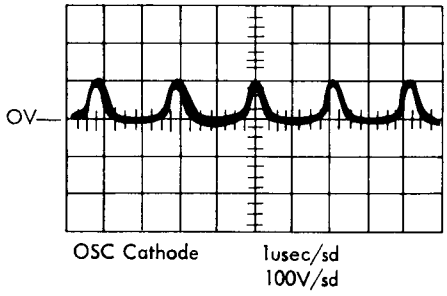


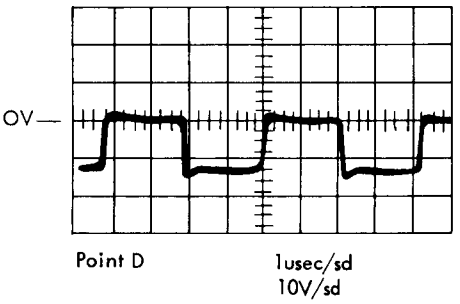


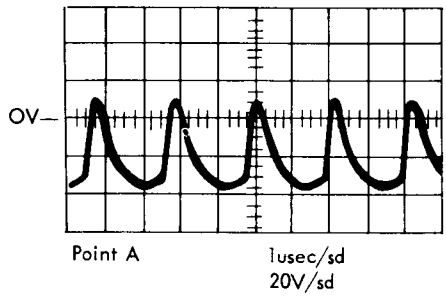












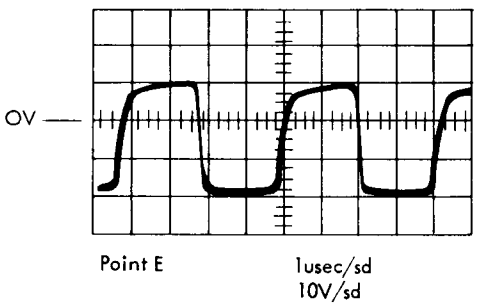
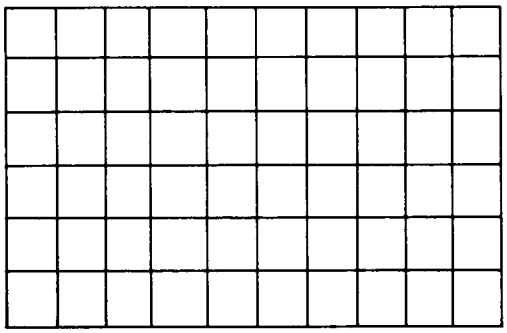
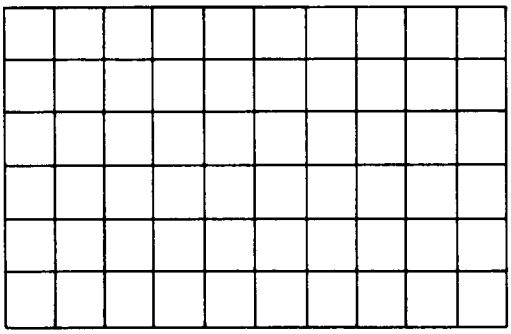
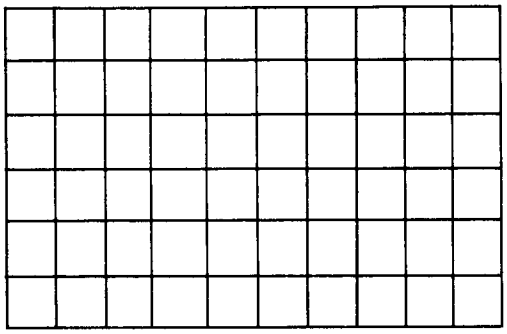


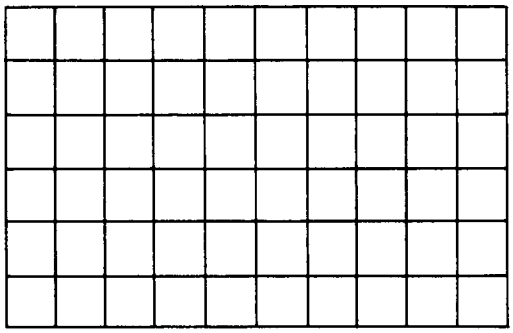
FIGURE C63. WAVE FORMS FOR 476KC OSCILLATOR AND CLOCK

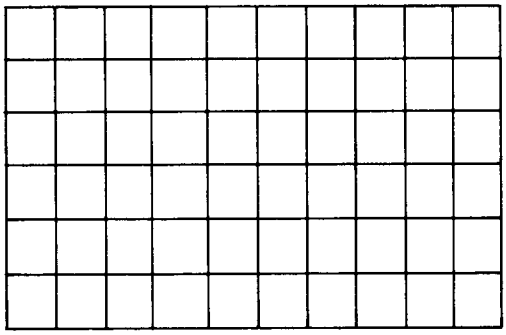
NOTES

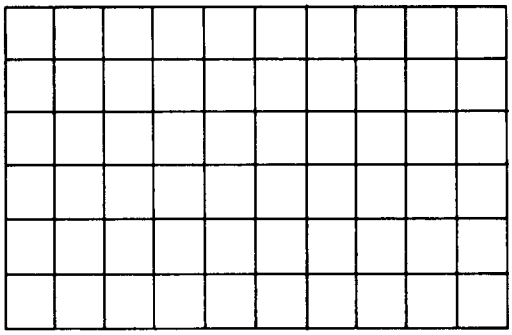


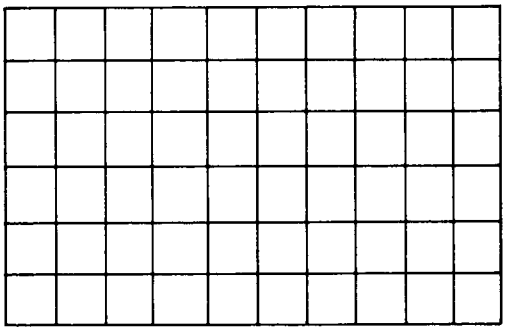


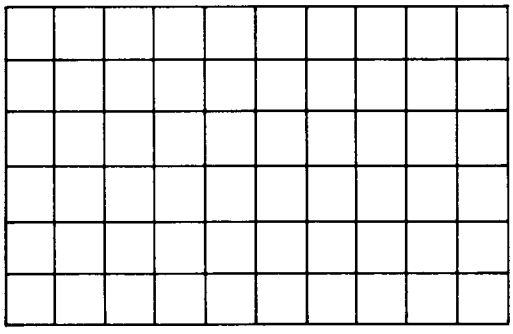












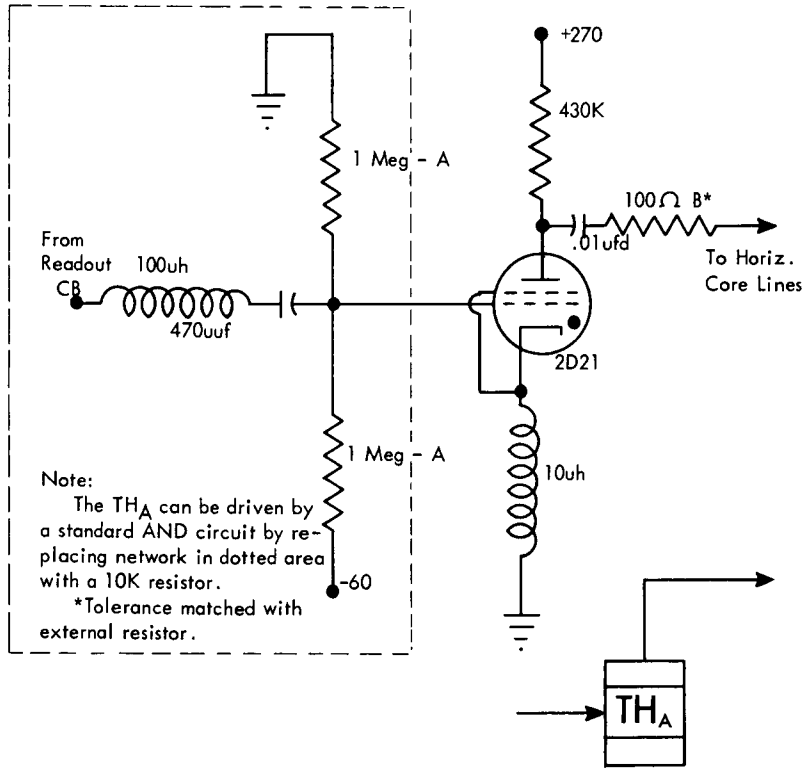


FIGURE C64. READ-OUT THYRATRON --TH_A

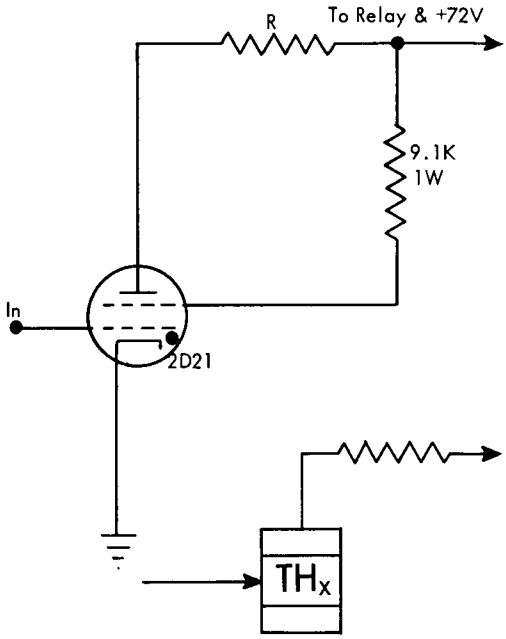


FIGURE C65. THYRATRON RELAY DRIVER -- TH_X

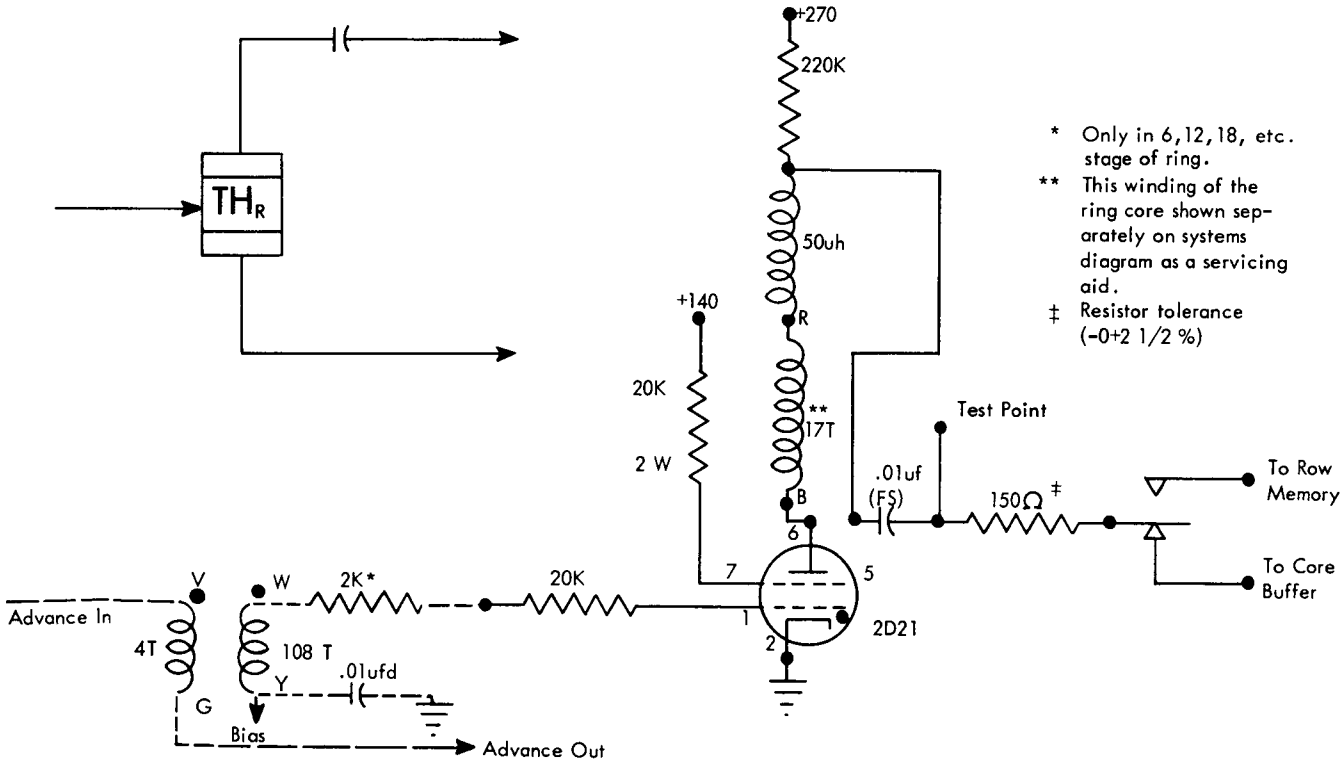


FIGURE C66. READER RING CIRCUIT THYRATRON -- TH_R

2.09.00 THYRATRON CIRCUITS

Thyratron operation is described in "Standard Circuits," section 2.14.00, Book A.

2.09.01 Printer/Punch Magnet Thyratron (TH)

The thyratron (TH) is described in "Standard Circuits," section 2.14.01, Book A.

2.09.02 Read-Out Thyratron (TH_A)

The read-out thyratron (TH_A) (Figure C64) is used in the printer and punch to read out of the core matrices. Circuit breakers are used to provide the input pulse and the input contains a 100-uh coil to smooth out the fluctuations caused by contact bounce. The tube is initially held cut-off by the input divider network. A positive pulse causes the TH_A to fire with a resultant drop of about 200 volts at the plate. The coupling capacitor to the core line discharges and the discharge current represents full current to read-out (reset) the cores (about 700 ma). The coil in the cathode circuit limits the current build-up through the tube (a design specification). The thyratron is self-extinguishing because the effective plate voltage drops too low to sustain ionization. When the tube cuts off, the coupling capacitor recharges to +270 volts.

2.09.03 Reader Ring Circuit Thyratron (TH_R)

The TH_R (Figure C66) is used to read out of the cores of the core buffer matrix or row memory in the reader. Where the read-out takes place is conditioned by the status of relay contacts. The TH_R, when fired, sets the ring core in the plate circuit to allow stepping of the ring circuit. The next advance-current pulse hitting the set ring core allows this core to reset and the resultant positive output is fed to the grid of the next TH_R, firing it and setting its ring core. Thus, the TH_R's firing sets up the conditions necessary to fire the next position in the ring.

As each thyratron fires, its plate voltage falls sharply. The coupling capacitor at the plate now discharges. The discharge current is drawn through the cores in the buffer matrix or row memory to reset these cores. Brushes reading the holes in the card set the cores selectively in the buffer matrix or row memory previous to the ring circuit operation. Thus, the TH_R, as part of the ring circuit, controls the unloading of all information stored in the matrices in a serial manner (one character at a time).

The TH_R is initially held cut off by the bias level (a -DC voltage level). It is selectively fired by the action of the ring cores. A 50-uh coil in the plate circuit tends to slow the rise of current through the tube as the thyratron fires. The tube is self-extinguishing because the plate voltage falls too far to sustain ionization.

2.09.04 Thyratron Relay Driver (TH_X)

The TH_X (Figure C65) is used in the card punch and printer to pick relays. The plate of the TH_X is returned through the relay coil to +72 volts. In the quiescent state, the TH_X is cut off. When the input voltage rises, the TH_X fires and conducts current through the relay. The plate supply voltage is broken through the operation of circuit breakers to extinguish the thyratron.

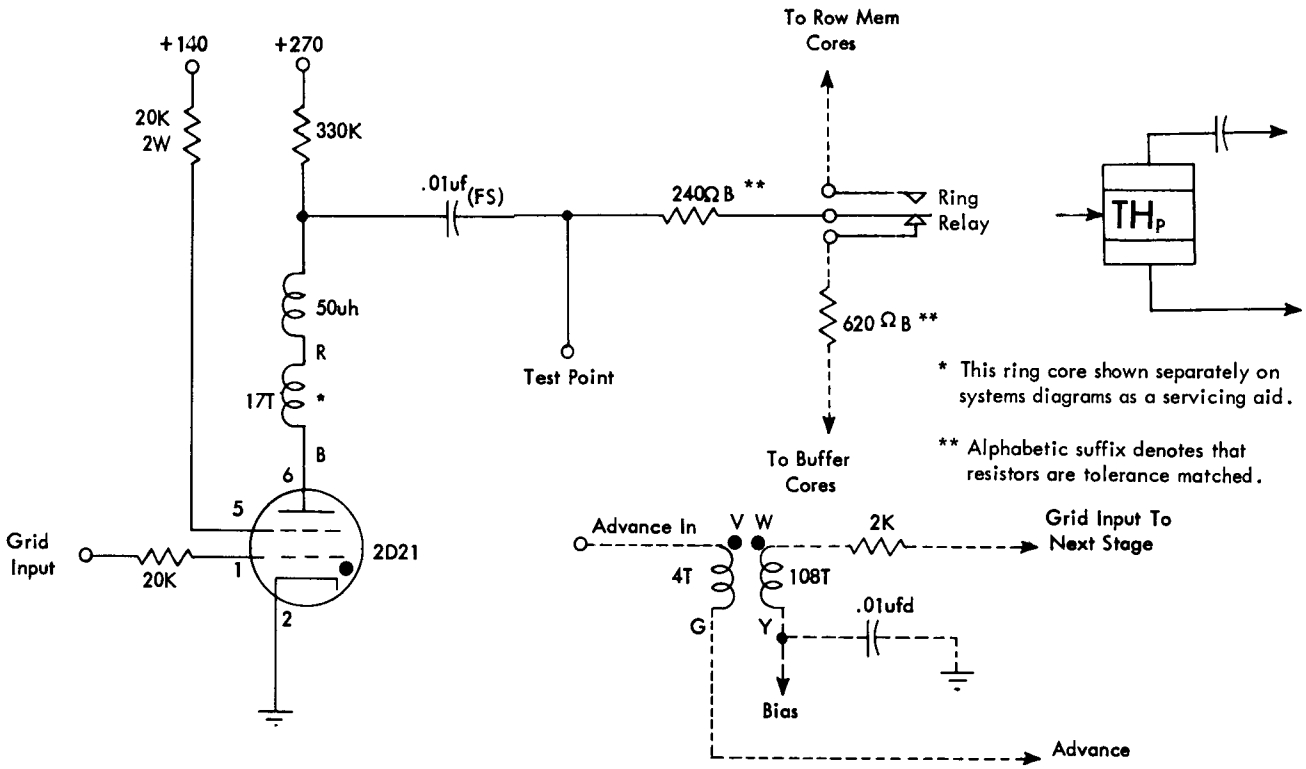


FIGURE C67. PRINTER/PUNCH RING CIRCUIT -- TH_P

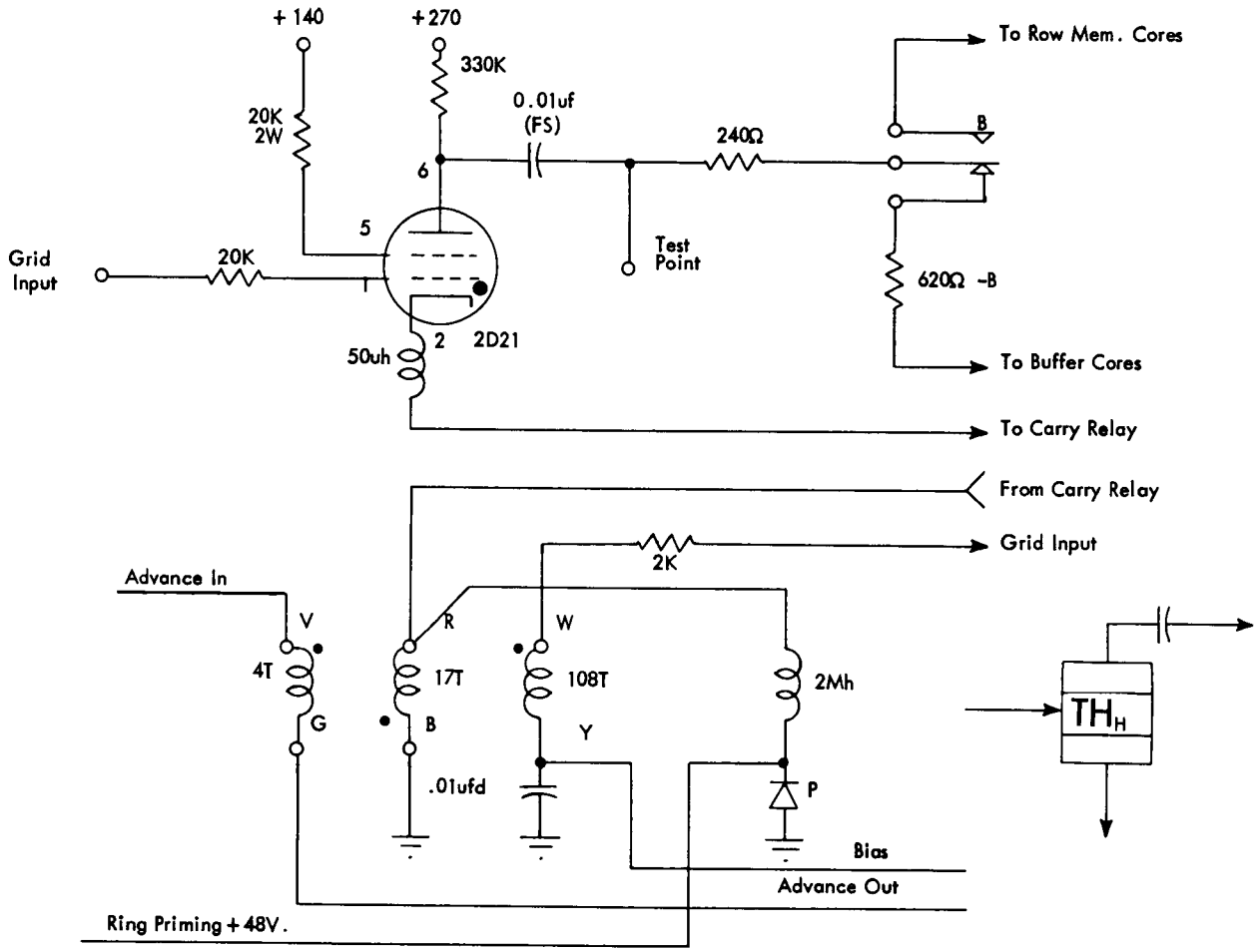


FIGURE C68. PRINTER/PUNCH HOME POSITION RING CIRCUIT -- TH_H

2.09.05 Printer/Punch Ring Circuit Thyratron (TH_P)

The TH_P (Figure C67) is used in the printer/punch ring circuits to control the ring, and also to supply half of the necessary writing current for writing in the printer/punch core buffer matrix. It also supplies the non-coincident (full) current necessary to read out of the row memory cores.

As in the reader ring circuit thyratron TH_R (section 2.09.03, Book C), the ring cores control the selective firing of the ring thyratrons. In this case the ring core is in the plate circuit, although the operation is the same. Firing of the thyratron sets its ring core so that the next advance current pulse can reset the ring core and allow the next thyratron to be fired. When the thyratron fires, the plate of the capacitor in the line going to the buffer cores shifts about 200 volts. The capacitor draws current to discharge to the new voltage, and the cores in the buffer have half of the necessary current to set them. If the other half of the necessary current to set the cores is supplied by the current drivers from the horizontal line, then these cores will be set.

The TH_P is a self-extinguishing thyratron. When it is fired, the plate voltage drops to a level too low to sustain ionization.

2.09.06 Printer/Punch Home Position Ring Thyratron (TH_H)

The thyratron TH_H (Figure C68) is used in the home position of the thyratron ring circuit in the printer and punch. The TH_H differs from the TH_P only in the fact that the ring core is located in the cathode circuit rather than the plate circuit of the TH_H. The extra input in the ring circuit of the TH_H is used to prime the ring core through CB's in order to start the thyratron ring. In all other respects, the TH_H operates the same as the TH_P.

2.10.05 Read Pre-Amplifier (AT_3)

(This arbitrarily-assigned number follows section 2.09.06.)

The AT_3 is used on the 729 I Magnetic Tape Unit. Is is similar to the AT used with the 727 Magnetic Tape Unit. The third stage tube is now a 6350 instead of a 6211; the separation of the read and write heads in the 729 make the tube diode gate of the AT unnecessary.

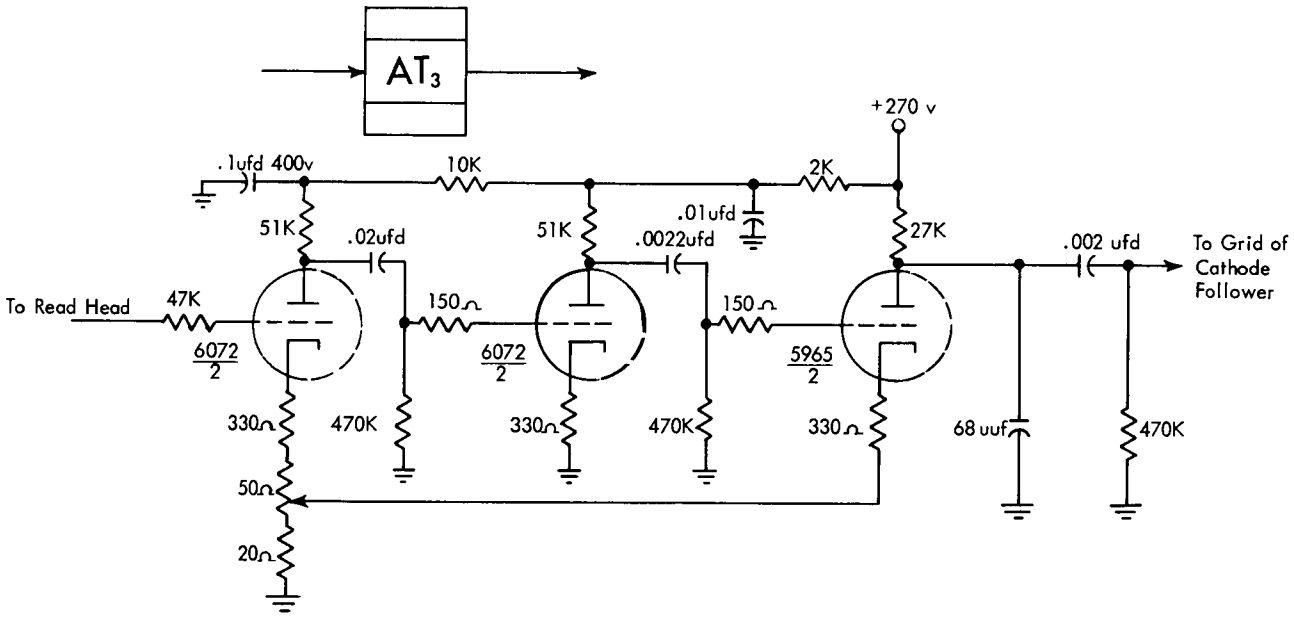


FIGURE C69. READ PRE-AMPLIFIER -- AT_3

Component Circuits

Book D. Auxiliary Equipment

CONTENTS

CONTENTS (continued)

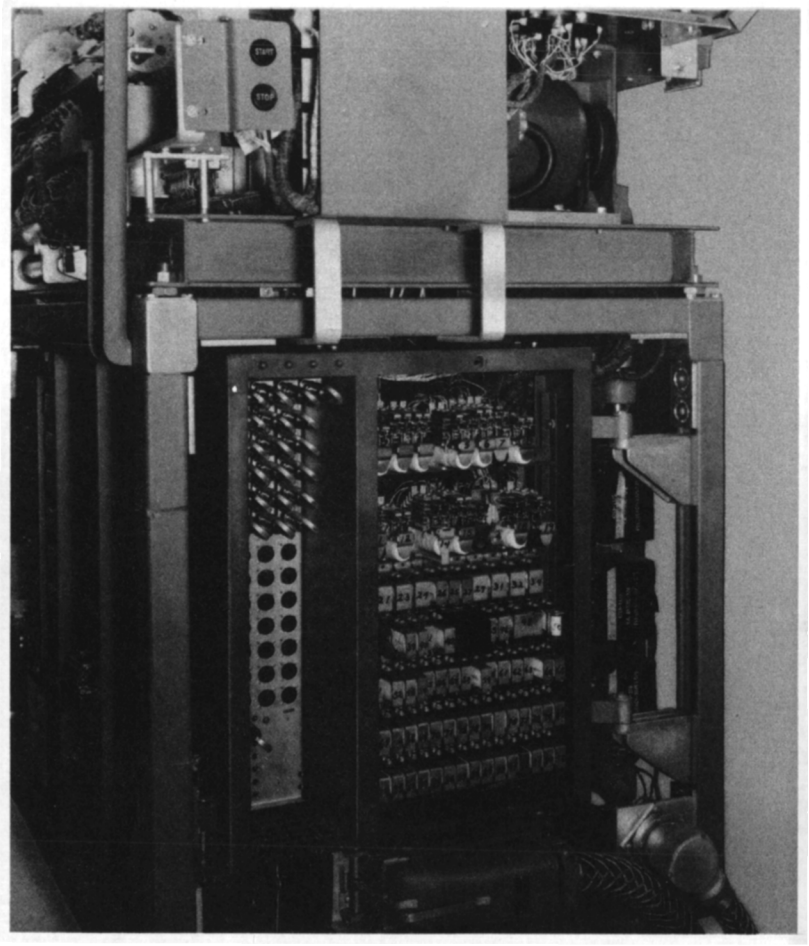


FIGURE D1. 720 PRINTER RELAY GATE 1

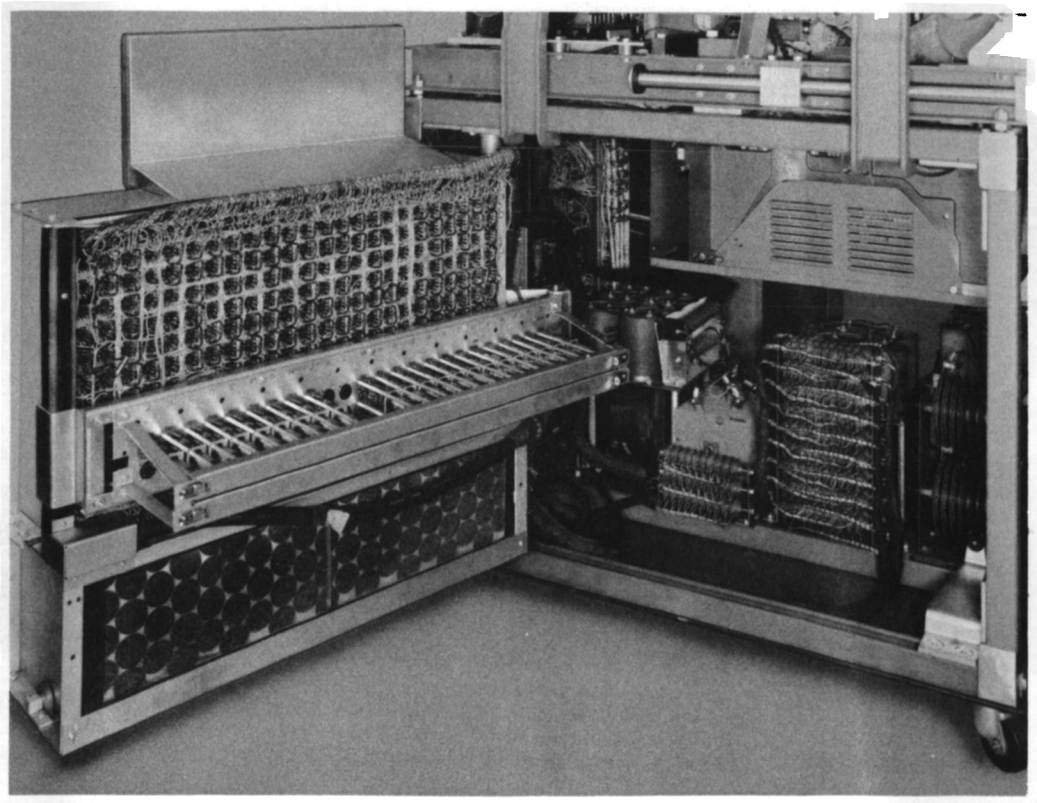


FIGURE D2. 720 BACK AND PIGGY BACK

1.00.00 IBM 720 PRINTER

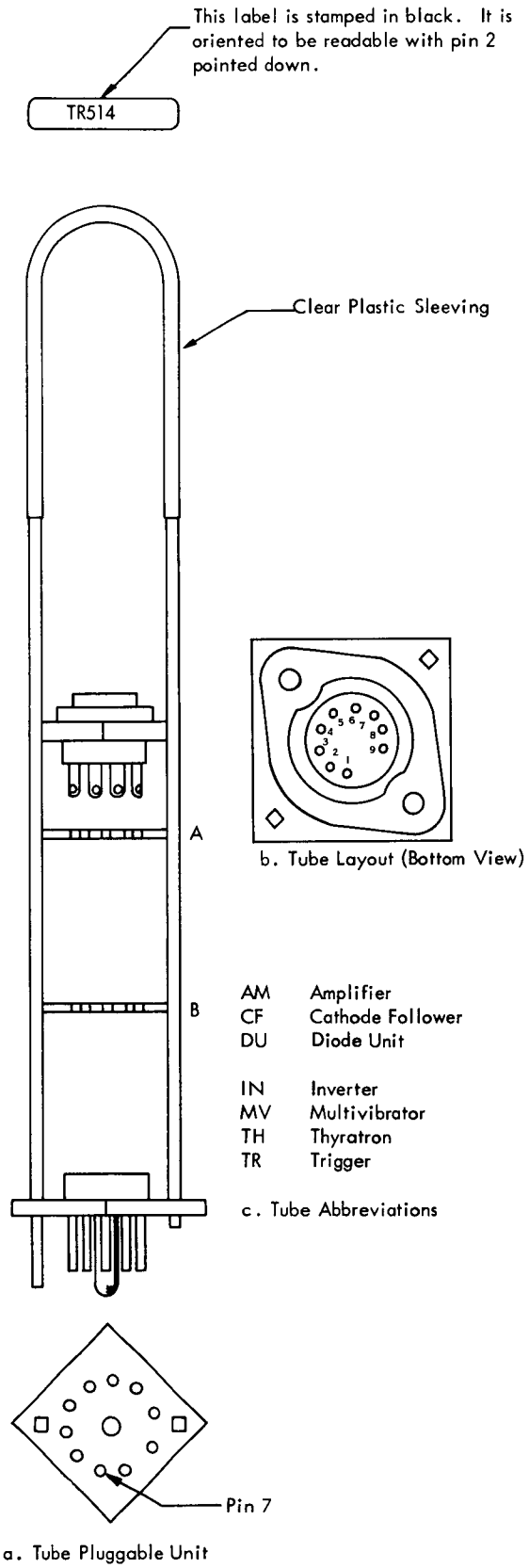
1.00.01 General Information

The component circuits used in the 720 Printer are presented in this book. If voltage levels are the same throughout the machine for a particular circuit, the voltages are shown on the pluggable unit diagram. For some circuits, the voltages are varied by special voltage dividers external to the logic block. In these instances, the voltages are omitted from the diagrams to avoid any possible confusion.

Whenever possible, the reader is referred to another part of this manual where a similar circuit is discussed in great detail. Those circuits that have no counterpart are presented with sufficient information to make the circuit understandable. In every case, space is provided below each description so that pertinent notes may be made.

1.00.02 Pluggable Units

Each circuit is mounted on a separate pluggable unit (Figure D3a) designed to accommodate one tube and its associated components. The unit is labeled on the handle so that it is readily identifiable while in place in the machine. The identification is made up of two letters and three numbers. The letters designate the type of circuit and the number further specifies the specific design.



a. Tube Pluggable Unit

b. Tube Layout (Bottom View)

c. Tube Abbreviations

FIGURE D3. 720 PRINTER PLUGGABLE UNIT

1.01.00 AMPLIFIERS

The basic grounded-grid amplifier is discussed in section 2.10.00, Book A.

1.01.01 AM510

This circuit is no longer used.

1.01.02 AM516

The AM516 is the basic amplifier for the printer ring-check circuit. The unit is used to amplify signal levels at the input with the full plate output of +35 to +135 volts and a tapped plate output of +85 to +135 volts. The amplifier does not invert the signals.

The left half of the tube acts as a cathode follower and the right half operates as a grounded-grid amplifier. The output is taken from a divider off the tapped plate load. The input is applied to the left grid of the tube. The right grid is returned to -3v from a resistor divider.

When the input voltage rises to +10 volts, the cathode voltage rises, causing an effective -1 volt bias on the left grid. Thus, the left side conducts. The effective bias on the right grid is now -14 volts (-3 and 11); the right side is completely cut off. The plate is now at +135 volts.

As the input shifts 40 volts negative, the cathode voltage drops only to -6 volts because of grid current. This leaves an effective bias of -24 volts (-30 and +6) on the left grid and cuts off the left side. The effective bias on the right grid is now +3 volts (-3 and +6) and the tube conducts on the right side.

The grid current is about 1.5 ma. The output can be fed to any divider network to obtain desired input levels. In this application, the divider network used is one for thyratron levels.

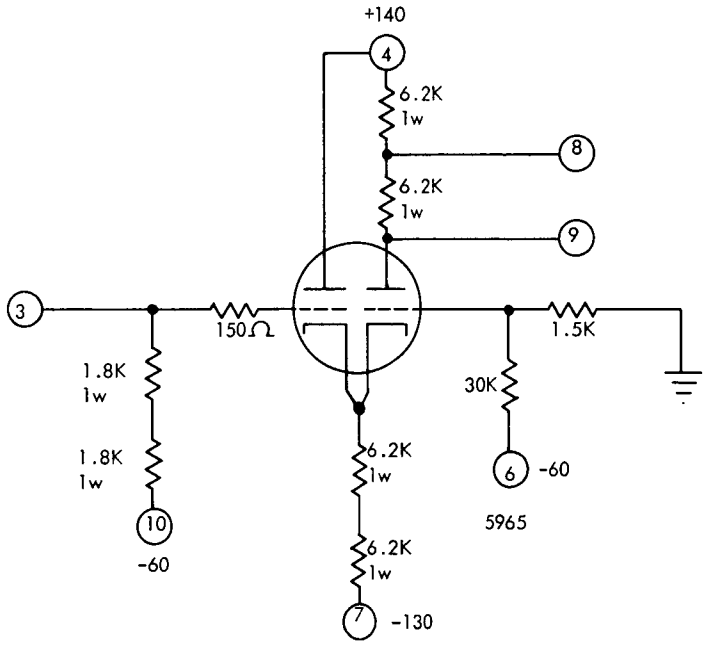


FIGURE D4. AMPLIFIER (AM516)

1.02.00 CATHODE FOLLOWERS

The operation of the standard cathode follower is discussed under "Basic Theory," section 2.09.00, Book A.

1.02.01 CF530

The CF530 is the basic cathode follower for signal level pulses (-30 volts and +10 volts). If used to drive cable lines between units, the cathode follower load resistors are not returned to -60 volts (pins 4 and 9) and load is supplied externally at the other end of the cable line.

Description and components are identical to K as used in Books A, C, and E.

1.02.02 CF531

The CF531 is the basic cathode follower for thyratron levels (-40 volts and +25 volts).

It is similar to the CF530 except that when a CF531 is driven by another CF at the opposite end of a cable line, the driving CF load resistor is connected internally across the input to the CF531 to -60 volts. Otherwise, pins 9 and 10 are not used.

The 91-ohm cathode resistor, present in the CF530, is eliminated, causing the output levels to be slightly higher than the input levels.

The grid resistor is larger to limit grid current.

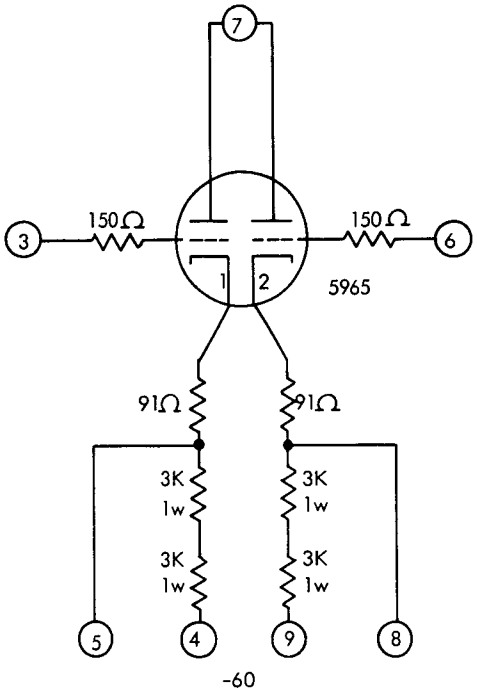


FIGURE D5. CATHODE FOLLOWER (CF530)

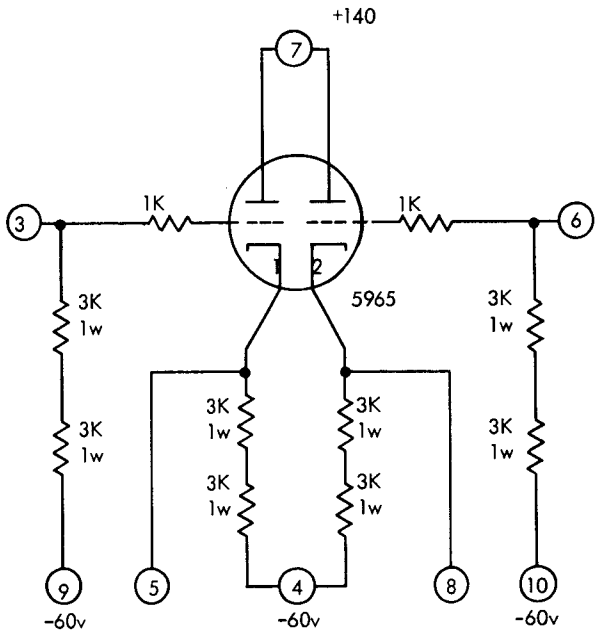


FIGURE D6. CATHODE FOLLOWER (CF531)

1.02.03 CF539A

The CF539A is the basic cathode follower for thyratron levels (-15 volts and +25 volts). The output from pins 9 and 10 are used as part of a column pulse OR circuit in the printer ring check.

The output is a basic thyratron level (-15 volts and +25 volts). Direct output (pins 5 and 8) is fed to the grids of column TH506's (seven per column), so that each cathode follower drives seven TH506's.

The output from pins 9 and 10 are part of a positive OR circuit controlling odd or even column pulses in the printer ring check. The diodes are used as the logic diodes for the OR circuit.

1.02.04 CF549

The CF549 is the basic cathode follower for thyratron output levels (-27 volts and +25 volts). It is used as an AND circuit driver.

The output of the CF549 drives one line of a two-way positive AND circuit.

The 15-uuf compensating capacitor on the input divider network improves rise and fall time.

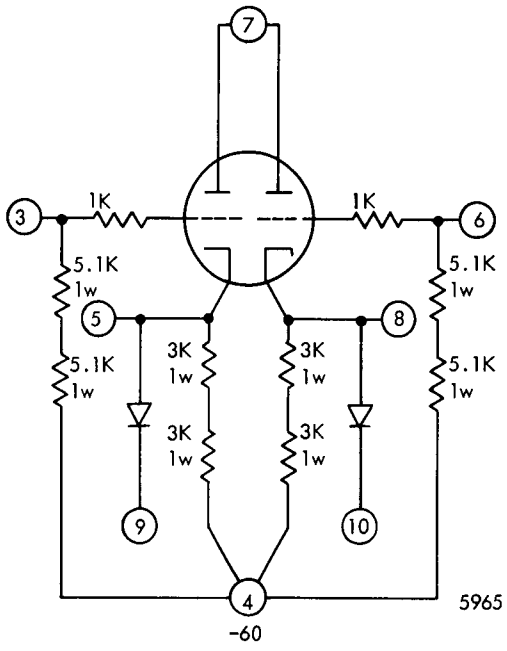


FIGURE D7. CATHODE FOLLOWER (CF539A)

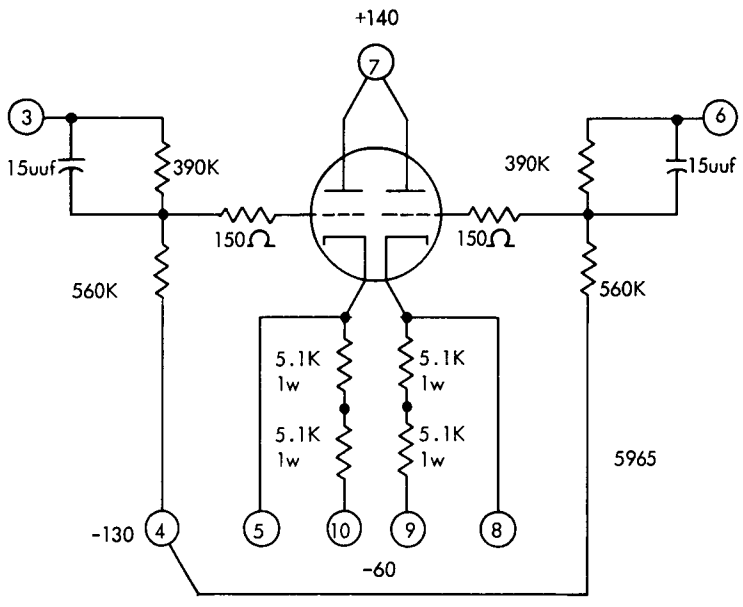


FIGURE D8. CATHODE FOLLOWER (CF549)

1.02.05 CF550

The CF550 is the cathode follower for signal levels (-30 volts and +15 volts). It is used as an AND driver and as an OR input. It is designed to operate as the load into which the plate output of a trigger or amplifier work. The input divider network sets the input levels at -30 volts and =15 volts. The output down level is slightly higher than the input down level (-27 volts).

To operate as a cathode follower OR circuit, the outputs are tied together with either pin 9 or pin 10 tied to -60 volts.

1.03.00 DIODE CIRCUITS

A discussion on crystal diodes appears in the appendix of this manual, Book E.

1.03.01 Diode Unit, DU 1

The DU1 is a general purpose pluggable unit for AND and OR circuit combinations. The AND and OR circuits depend upon the direction in which the clip-in diodes are connected in the unit, and also upon the voltage to which they are returned, either positive or negative. The diode load resistors determine the value of the wave-form rise and fall time.

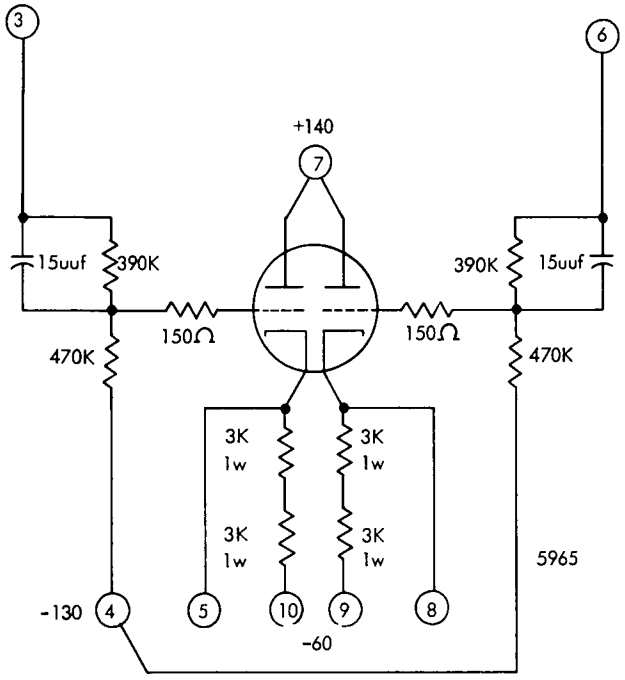
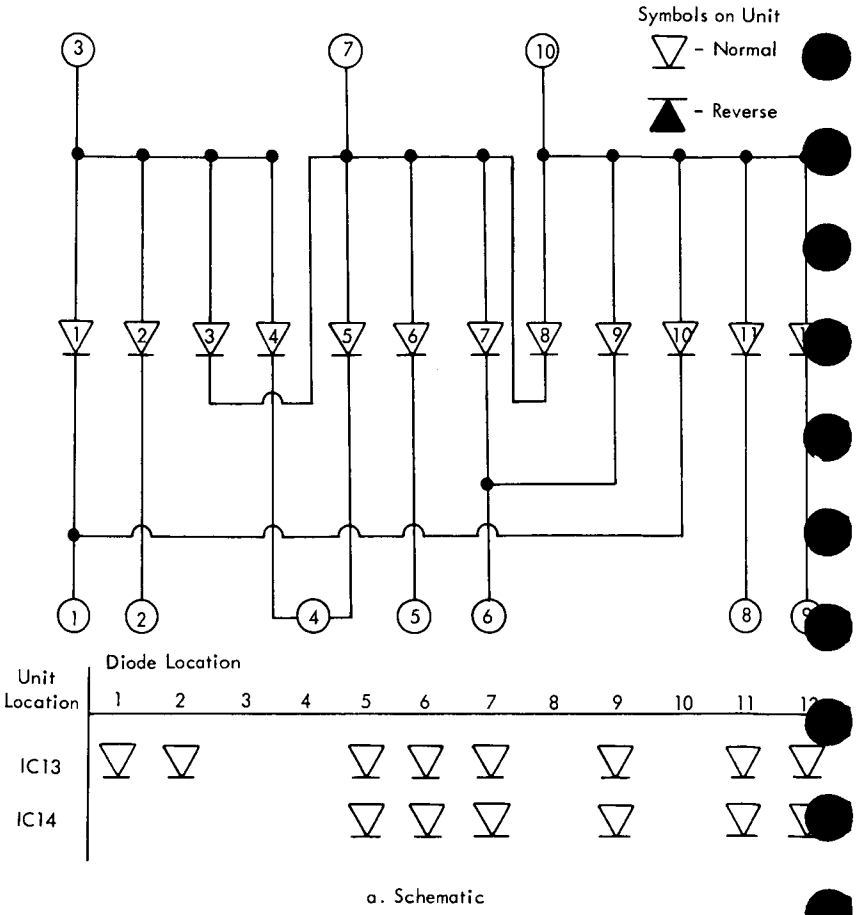


FIGURE D9. CATHODE FOLLOWER (CF550)



a. Schematic

FIGURE D10. DIODE UNIT (DU1)

1.04.00 INVERTERS

The operation of the standard inverter is discussed under "Basic Theory," section 2.05.00, Book A.

1.04.01 IN503

Input levels are both signal (-30 volts and +10 volts) and thyratron (-27 volts and +25 volts). Output levels are (+40 volts and +140 volts) from full plate and (+90 volts and +140 volts) from tapped plate. The IN503 uses only the full plate output in the printer ring check circuit. In one case, this is fed to a CF550 resulting in a signal level input of (-20 volts and +10 volts). In the other case, the full plate output is tied to +140 volts through an 8.2K resistor in the plate circuit of a TR514. When the inverter conducts, it pulls the plate of the TR514 down, causing it to change its state if that side of the TR514 is not conducting at the time.

1.04.02 IN509

The IN509 has a signal level input (-30 volts and +10 volts); the output drives a relay, the output down-level picking the relay, and the up-level dropping it.

With an input of -30 volts, the grid is biased beyond cut-off and no plate current flows. In this application, the plate is connected through a resistance in series with a hold and a pick coil returned to +140 volts. The output, with no plate current flow, is at a +140v level. This operation is identical for either half of the tube.

As the input goes 40 volts positive (+10) the grid bias is zero volts or slightly positive, and the tube conducts. With the relay load, the output level drops to +93 volts. The current through the load provides enough ampere turns to pick and hold the relay.

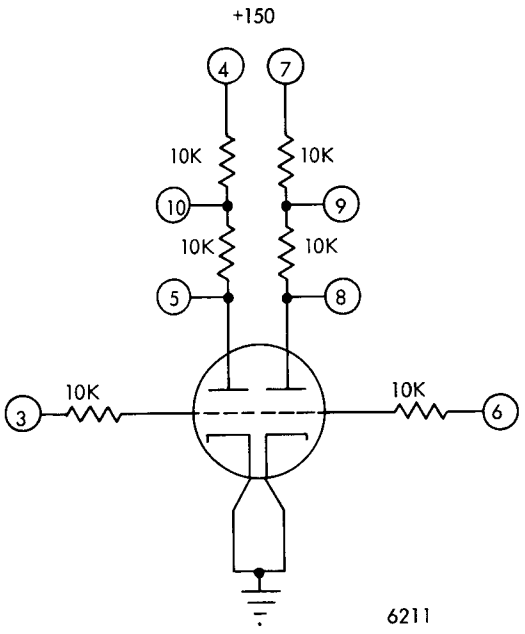


FIGURE D11. INVERTER (IN503)

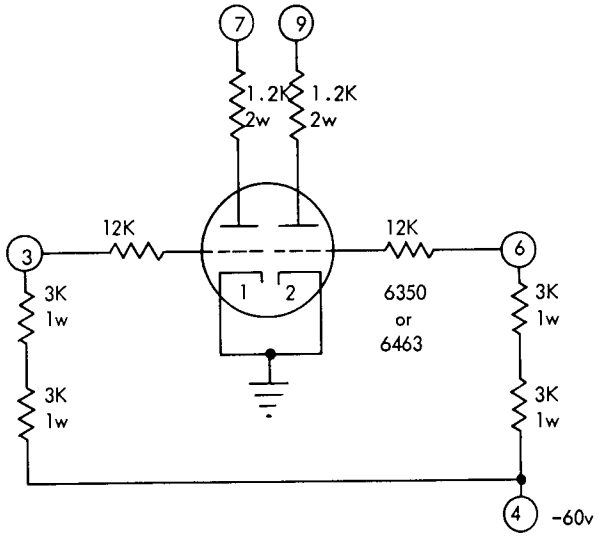


FIGURE D12. INVERTER (IN509)

1.04.03 IN536

The IN536 has a tapped plate output available for use as the driver for a gated trigger.

Signal level input (-30 volts and +10 volts) to the left grid causes conduction on that side of the tube when the input shifts to positive. This drops the bias on the right grid to -20 volts and cuts off the right side and results in a tapped output of +140 volts.

On a negative input shift, the left side cuts off, raising the effective bias on the right grid above ground. The right side begins to conduct and the tapped output falls to +90 volts.

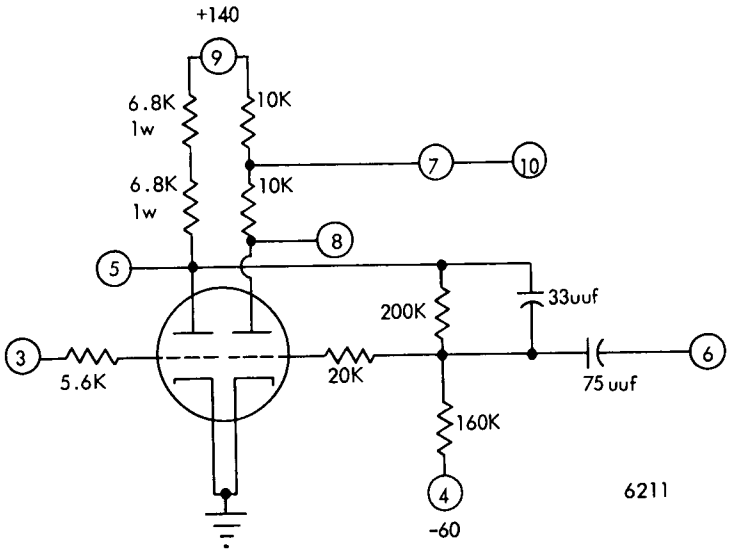


FIGURE D13. INVERTER(IN536)

1.05.00 SINGLE SHOT MULTIVIBRATORS

1.05.01 MV501

The MV501 provides a 400-usec positive pulse (-30 volts and +10 volts). The basic principle is similar to the operation of the single shot (SS_E). At quiescent state, the right triode conducts because of positive bias on its grid. Voltage at the grid is zero or slightly positive; at the plate, +40 volts; at the output divider, -30 volts. With the plate at +40 volts, the grid of the left triode rests at -15 volts, keeping the left side cut off.

Upon application of a 37v positive shift to the left grid through a .001-mfd capacitor, the left triode is driven into conduction, lowering its plate voltage. This downward shift is applied to the grid of the right triode through the 1000-uuf capacitor, cutting the right triode off. This raises the voltage at the output divider to +10 volts and keeps +25 volts at the grid divider of the left triode, keeping it in conduction. As the 1000-uuf capacitor charges positively by way of the 820K resistor, it reaches -7 volts in about 400 usec at which time the right triode conducts again bringing the output pulse down to -30 volts and keeping the grid of the first triode below cut-off.

The main timing is caused by the RC charge time of the 1000-uuf condenser through the 820K resistor.

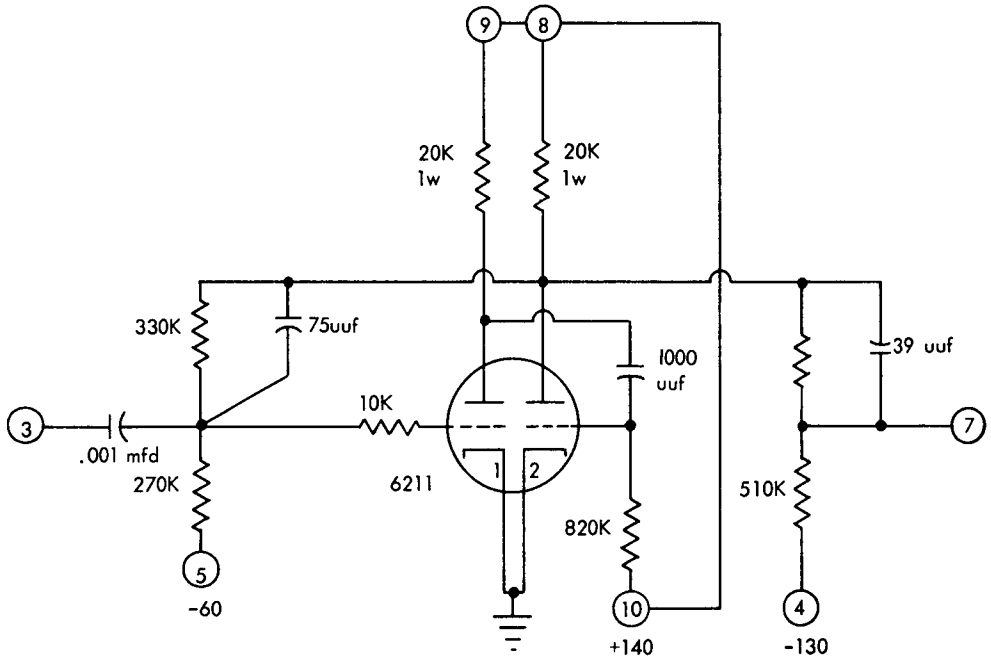


FIGURE D14. SINGLE-SHOT MULTIVIBRATOR (MV501)

1.06.00 THYRATRONS

The operation of thyratrons is discussed under "Basic Theory" in section 2.14.00, Book A.

1.06.01 TH506

The TH506 is a thyratron AND circuit to pick relay and magnet coils. In 720 application, the thyratron 506's are prefired through 4K resistors, giving each 16 ma of plate current at a plate voltage of 80 volts. This is done to insure simultaneous firing of the thyratrons.

The thyratron 506 can operate at a plate voltage of either +80 volts or +150 volts. At +80 plate volts, the input to the 47K grid resistor must be a minimum of +20 volts. At +150 plate volts, the minimum input to the 47K resistor must be +5 volts.

Both the plate circuit and the precheck circuit must be opened to de-ionize the tube. This is usually controlled by cam-operated circuit breakers.

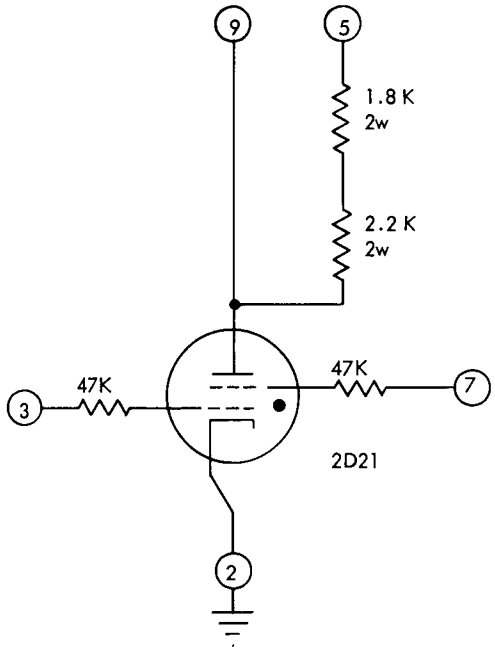


FIGURE D15. THYRATRON (TH506)

1.06.02 TH507

The TH507 is a thyratron memory device and relay driver, and also a magnet driver.

The TH507 has a +80v input level either directly to its grid or capacitively coupled to the grid to obtain an AC spiked input.

Certain TH507's have blowout capacitors between their plates preventing both thyratrons from being on at the same time. When one TH507 is on and the TH507 whose plate is capacitively coupled to it fires, the drop in plate voltage of the newly fired thyratron is momentarily applied to the coupling capacitor, causing a negative shift across it. This shift drives the plate of the first TH507 negative, and causes de-ionization in the tube, stopping conduction. However, if the charge time of the coupling capacitor is faster than the input drop-out time to the first TH507, that TH507 will fire again. To prevent this condition, the above-mentioned AC spiked input is used.

TH507 relay drivers are prefired through a 2K resistor. Upon completion of their plate circuits, they fire to pick relays in the carriage circuit. In this way, they serve as memory devices.

The TH507 can operate at +80 volts or +150 volts. The screen grid is tied to the grounded cathode.

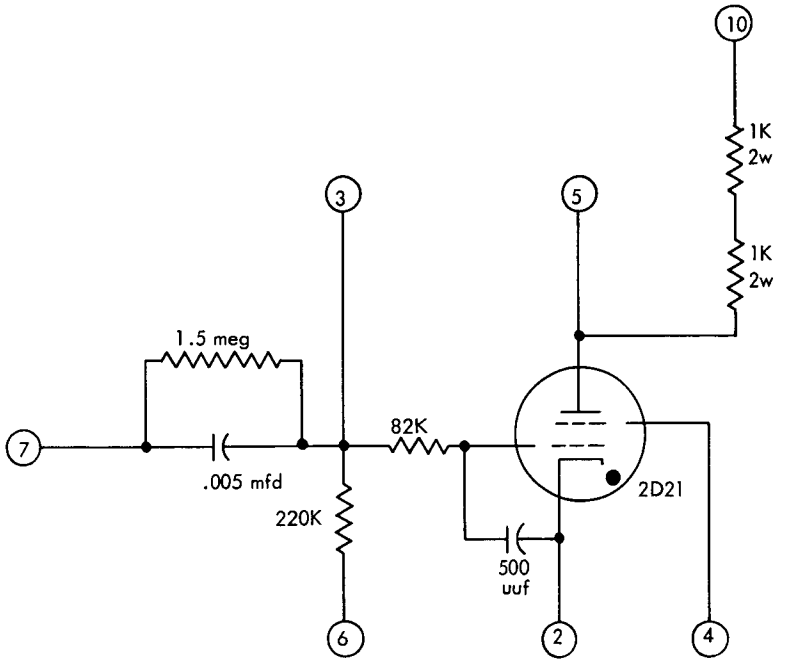


FIGURE D16. THYRATRON (TH507)

1.06.03 TH508

The TH508 is a relay driver for 720 carriage and printer controls. It is also a storage device. The TH508 can operate at +80 plate volts or +150 plate volts. To insure proper operation, the minimum positive input to the 47K grid resistors must be +20 volts for a +80v plate, and +5 volts for a +150v plate.

Certain TH508's have cathode load resistors. The outputs from these are fed to controlling cams in series with the grids of other TH508's. When a cathode loaded TH508 fires, its cathode level shifts to +70 volts, and when the controlling cam in the grid circuit of the second TH508 makes, this positive voltage is applied to its grid, and causes the thyratron to fire. The first thyratron acts as a storage medium; the second one drives a relay. Each screen grid is either biased at +80 volts or returned to its own plate through a resistor.

1.06.04 TH523

The TH523 is a relay driver. Basic signal level input is (-30 volts and +10 volts) to both grids. Coincident positive pulses to its grids cause the TH523 to fire and pick and hold a relay. The pulses are coincident at check time. They are also coincident for a ring check edit. This causes the thyratron to fire and checks its operation.

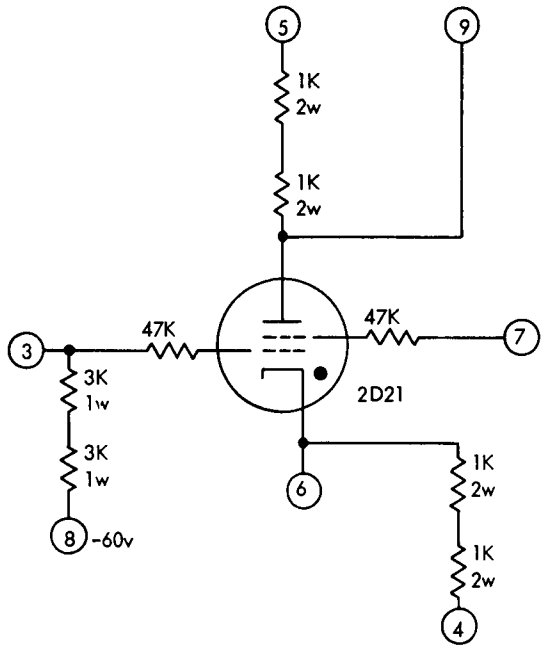


FIGURE D17. THYRATRON (TH508)

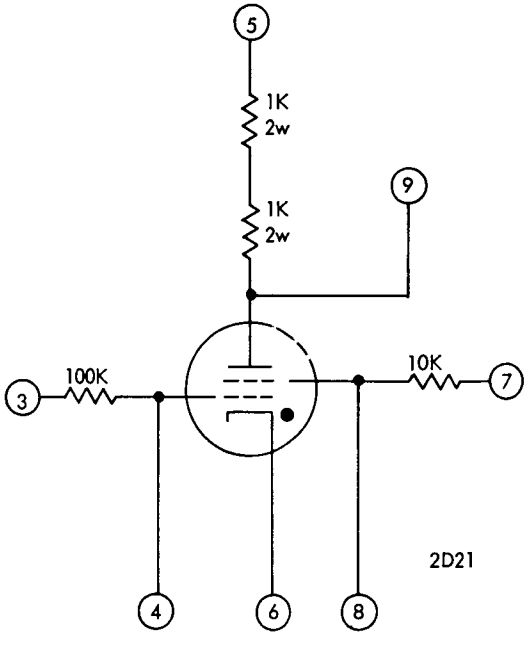


FIGURE D18. THYRATRON (TH523)

1.07.00 TRIGGERS

The operation of the standard trigger is discussed under "Basic Theory," section 2.06.00, Book A.

1.07.01 TR501

Description and components are identical with those for a T_C (section 2.02.01, Book C).

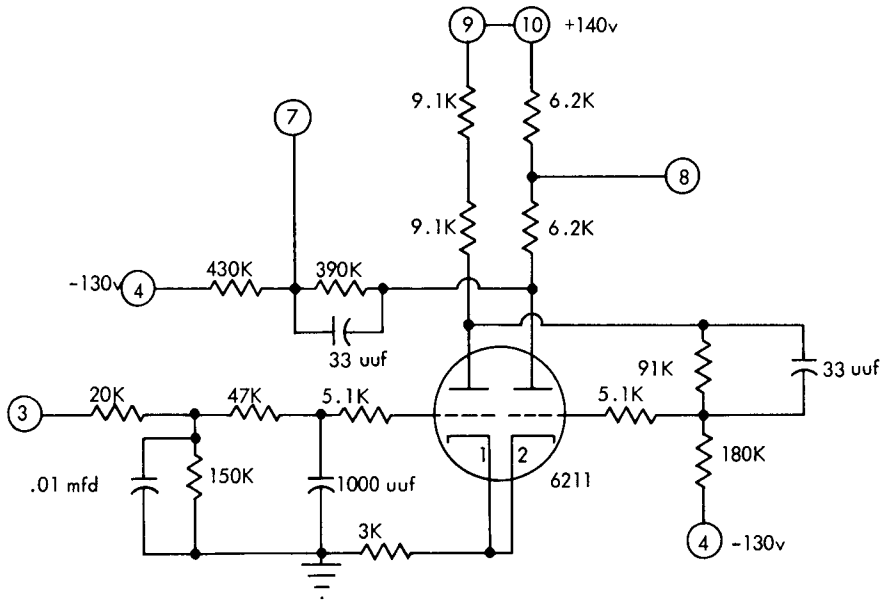


FIGURE D19. TRIGGER (TR501)

1.07.02 TR514

The TR514 is used in the 720A printer as a negative-shift input binary trigger. It also functions as a self-gated input trigger.

For negative shift application, the input (+85 volts and +135 volts) is fed from the tapped plate output of an AM516, through two F diodes and two 33-uuf capacitors, to the grids of the TR514. As the input voltage changes from +85 volts to +135 volts, the cathodes of the input diodes become positive with respect to their anodes and look like a high resistance (400K) to the input capacitors. This causes a gradual change in voltage on the positive sides of the capacitors and keeps the grids at their previous potential. With a 50v negative shift (+85 volts and +135 volts), however, the diodes now look like 200 ohms to the input capacitors. This results in an almost immediate change in voltage on the positive sides of the capacitors; because the voltage across a capacitor cannot change instantly, a negative pulse is applied to both grids. This causes the conducting side of the trigger to cut off and its plate voltage to rise. Because its plate voltage is coupled to the grid of the other side, that grid is pulled up to a positive bias and that side of the trigger begins to conduct.

When used as a self gated trigger, only one input to the trigger is used; there are no input diodes, and the trigger changes its state on both positive and negative input shift.

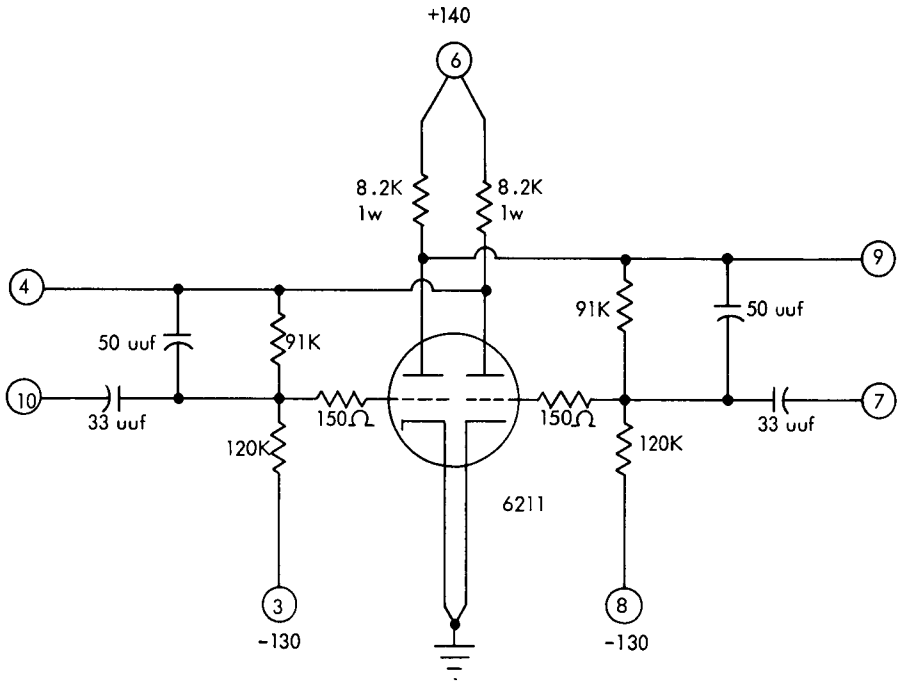


FIGURE D20. TRIGGER (TR514)

2.00.00 730A AND 735 COMPONENT CIRCUITS

2.01.00 LATCHES

A latch is a circuit composed of inverters and of cathode followers. It has two stable states. The circuit utilizes feedback to maintain either stable state. Latches used in the IBM 730A are of two types--single latches and double latches.

2.01.01 Single Latch

The single latch consists of a double inverter and a cathode follower. The plate of the second inverter is coupled to the grid of the cathode follower. The cathode follower output is coupled to the grid of the first inverter, through switching or directly, to provide a latch-back.

In systems diagrams the two blocks are drawn side by side. The plate-to-grid connection between the second inverter and the cathode follower is understood but not shown. The latch-back is shown. The blocks are identified as an AM unit and a CF unit.

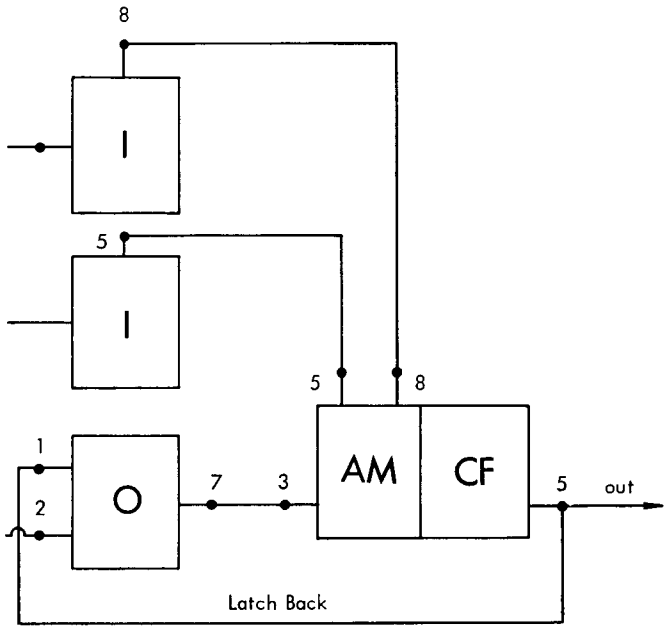


FIGURE D 21. SINGLE LATCH (OR LATCH - BACK)

Figure D21 is a schematic of a single latch with an "OR" circuit latch-back. This corresponds to the ring-drive-last-latch on Systems 735: 1.1.0.0.

ON State

1. The output from the cathode follower is up.
2. The first inverter is conducting.
3. The second inverter is not conducting.

OFF State

1. The output from the cathode follower is down.
2. The first inverter is not conducting.
3. The second inverter is conducting.

Type of Latch-Back

1. Direct latch-back--output from the cathode follower is fed directly to the grid of the first inverter.
2. AND circuit latch-back--output from the cathode follower is fed to the grid of the first inverter through an AND circuit.
3. OR circuit latch-back--output from the cathode follower is fed to the grid of the first inverter through an OR circuit.

Methods of Turning On

1. Plate pullover of first inverter.
2. Negative shift to grid of second inverter (using tapped output from another unit).
3. Plus signal to grid of first inverter.

Methods of Turning Off

1. Plate pullover of second inverter.
2. Plus shift to grid of second inverter (using full output from another unit).
3. Break AND circuit latch-back.

Outputs from a single latch can be taken from the plate circuits of either of the two inverters or from the cathode circuit of the cathode follower.

Examples of Latch-Back

1. Direct--Check Sample latch (735: 1.1.1.0)
2. OR circuit--ring drive last latch (735: 1.1.0.0).
3. AND circuit--ring position 1 latch (735: 1.2.0.0).

Examples of Turning On

1. Pull over first inverter--Check sample latch (735: 1.1.1.0).
2. Negative shift to grid of second inverter--ring position 1 latch (735: 1.2.0.0).
3. Plus signal to grid of first inverter--ring drive last latch (735: 1.1.0.0).

Examples of Turning Off

1. Plate pull over second inverter--information sample last latch (735: 1.1.0.0).
2. Plus shift to grid of second inverter--check sample latch (735: 1.1.1.0).
3. Break AND circuit latch-back--ring position 1 latch (735: 1.2.0.0).

2.01.02 Latch Ring

Figure D22 shows three positions of an open ring composed of single latches. If the first position of the ring is on, it will turn off when "ring advance" goes negative and breaks the AND circuit latch-back.

The second position will turn on as the first position is turned off. The negative shift at the plate of the second inverter (of the first position) is coupled to the grid of the second inverter (of the second position). The time constant of the coupling circuit is long enough to keep the second inverter (of the second position) cut off until the AND circuit latch-back comes up, and the latch is turned on. It will stay on until another ring advance pulse causes it to turn off. Then the third position of the latch ring will turn on.

Because the ring is an open ring, it will stop advancing when the last ring position is turned off. The ring was started when the home position was turned off after it had been turned on.

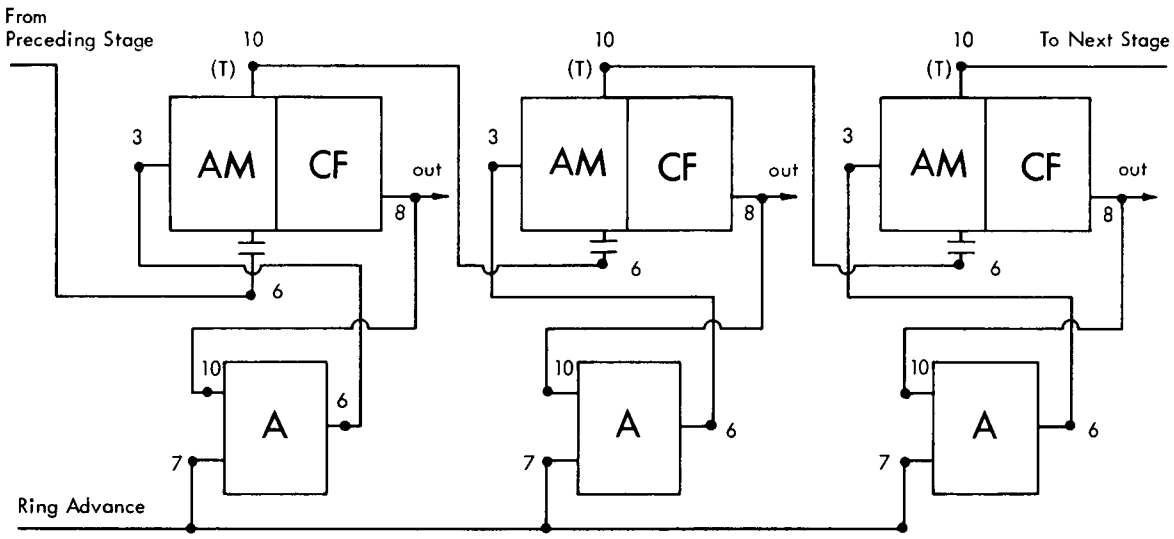


FIGURE D22. LATCH RING (3 STAGES)

2.01.03 Double Latch

A double latch consists of four tube halves. To form one-half of the latch, an inverter has its plate coupled to the grid of a cathode follower. The other half of the latch is identical to the first half.

The output from each cathode follower is fed to the grid of the inverter in the other half of the latch. This output may be coupled through switching, or it may be direct.

The double latches in the 730A use direct latch-back. An example is the ring drive information sample latch (Systems 735: 1.1.0.0). On the systems diagram, the two halves of the latch are shown separately. Each half consists of two blocks side by side. The blocks are identified by an I unit and a CF unit. The connection between the plate of the inverter and the grid of the cathode follower is understood but not shown. The latch-back is shown.

Figure D23 shows the schematic of a double latch. The double latch is useful in that it provides a plus cathode follower output when the latch is in either state. Either state of the latch can be chosen as the ON state, but thereafter any discussion concerning a particular latch must be consistent with the choice.

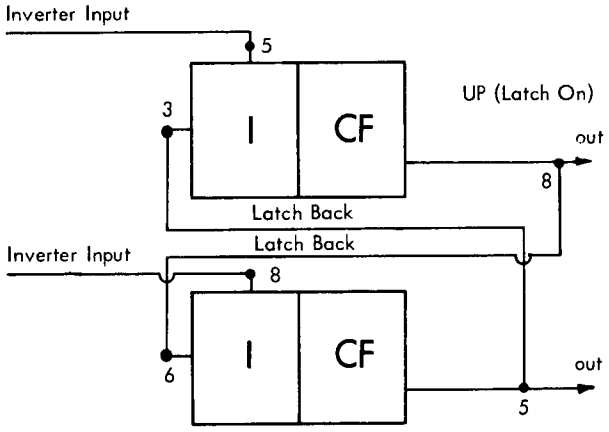


FIGURE D23. DOUBLE LATCH

2.02.00 CATHODE FOLLOWERS

The basic cathode follower is described in section 2.09.00, Book A.

2.02.01 CF 501

The CF 501 does not have the 91Ω dropping resistor in the cathode circuit, causing the output to be slightly higher than the input. It uses a 1K resistor in the grid in place of the normal 150Ω, to limit grid current.

2.02.02 CF 502

The CF 502 is similar to CF 501, except that the cathode load is 3.6K in place of 5.4K of the CF 502. A 6350 tube is used to handle heavier loads.

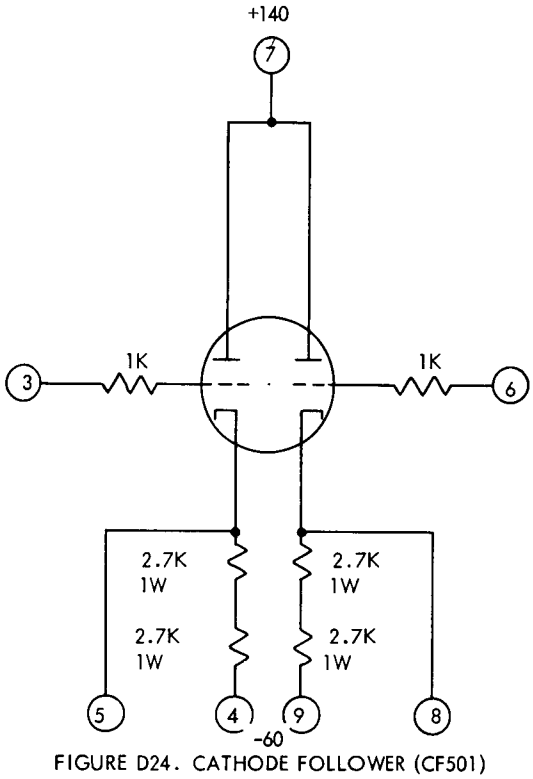


FIGURE D24. CATHODE FOLLOWER (CF501)

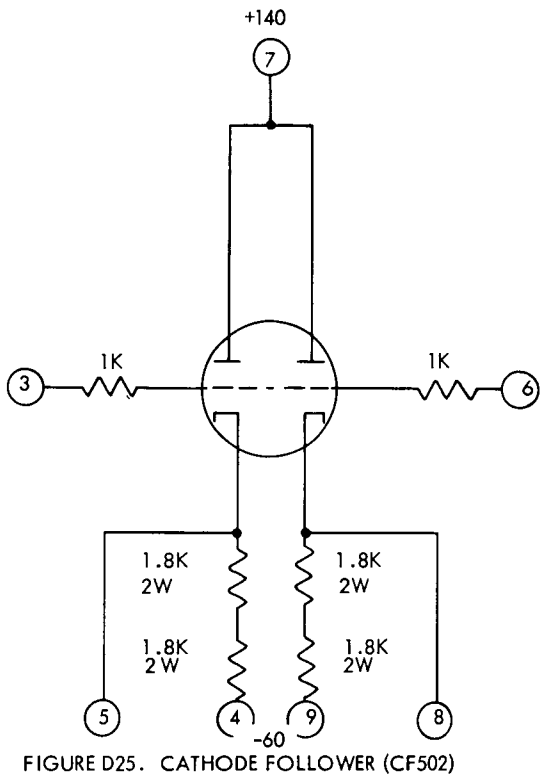


FIGURE D25. CATHODE FOLLOWER (CF502)

2.02.03 CF540

The CF540 is similar to the CF549. The compensating capacitor in the DC input circuit aids rise and fall time. The grid divider is tied to -270 volts instead of -130 volts. The cathode load resistor is 4.8K. No dropping resistor is used. A 6350 tube is used for driving heavier loads. The circuit is widely used in latches.

2.03.00 INVERTERS

The basic inverter is described in section 2.05.00, Book A.

2.03.01 IN551

The IN551 does not actually function as an inverter. Here, the input is fed through a 560 uuf capacitance to the cathode. A positive shift at the input (cathode) causes the tube to cut off, thus causing the output to rise. The reverse holds true for a negative shift at the input.

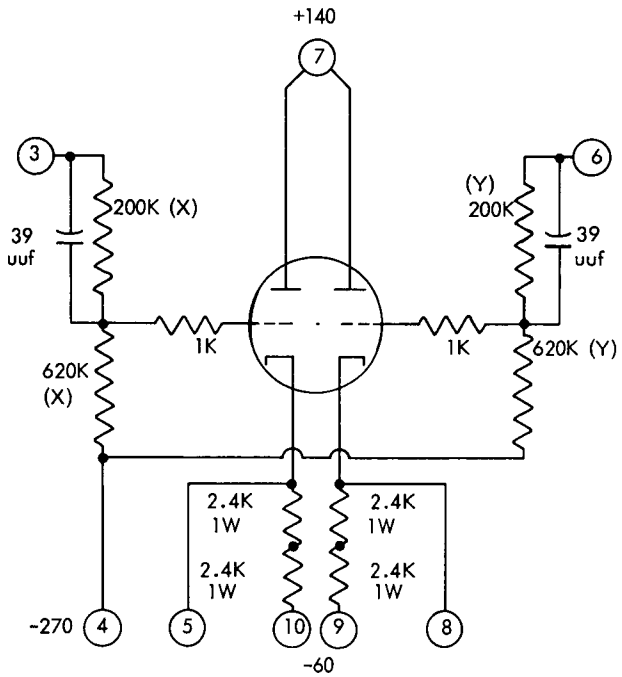


FIGURE D26. CATHODE FOLLOWER (CF540)

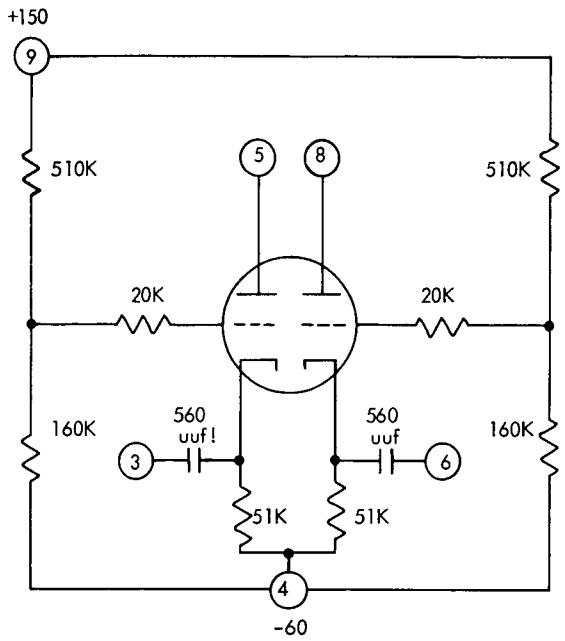


FIGURE D27. INVERTER (IN551)

2.03.02 IN553

The IN553 has a full plate output. The grid circuit is tied to -130 volts and uses a DC input with a 39 uuf compensating capacitor. The grid current is limited by a 1K resistor. A 5965 tube is used.

2.03.03 IN554

The IN554 is the same as the IN536 (section 1.04.03), except that the right grid is overcompensated and gives a better fall time. The left plate load resistor has less resistance to make a better driver than the IN 536. The capacitance at the input on pin 6 is reduced, for greater sensitivity.

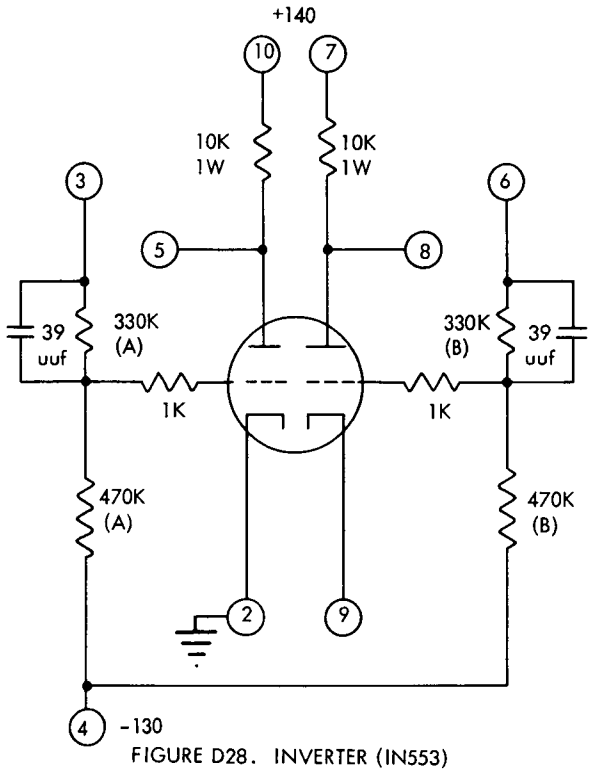


FIGURE D28. INVERTER (IN553)

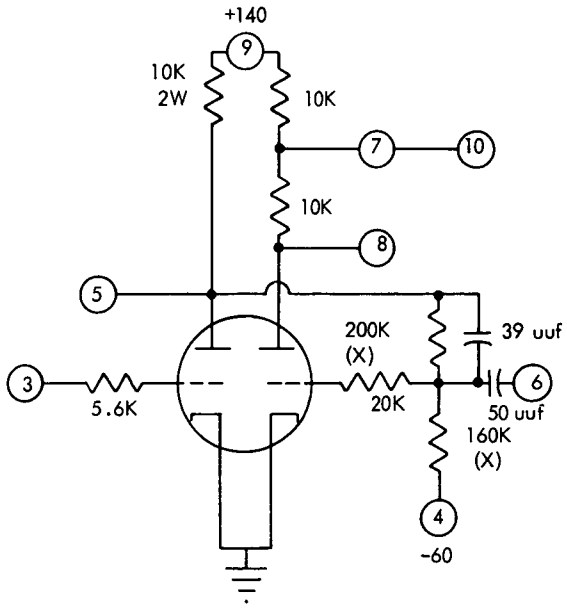


FIGURE D29. INVERTER (IN554)

2.04.00 MULTIVIBRATORS

2.04.01 MV502

The MV502 is a free-running multivibrator. The left plate is up for 3 usec and the right plate is up for 27 usec. The action is determined by the two cross-coupling RC circuits. The left grid uses 25 uuf and 470K; the right grid uses 68 uuf and one megohm. A negative shift to pin 3 causes the three-microsecond output to come up. This provides a means of synchronizing the multivibrator to external circuitry.

2.05.00 THYRATRONS

The operation of thyratrons is discussed under "Basic Theory" in Section 2.14.00, Book A.

2.05.01 TH509

The TH509 is used as a magnet driver. The plate is returned to +80 volts through a magnet coil. A neon is driven from the plate through a 4K resistance. A cathode output may be used. Both grids may be used as control.

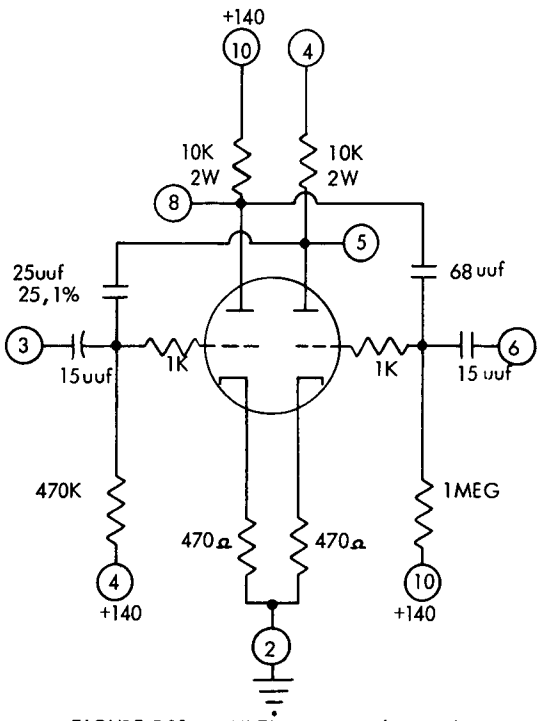


FIGURE D30. MULTIVIBRATOR (MV502)

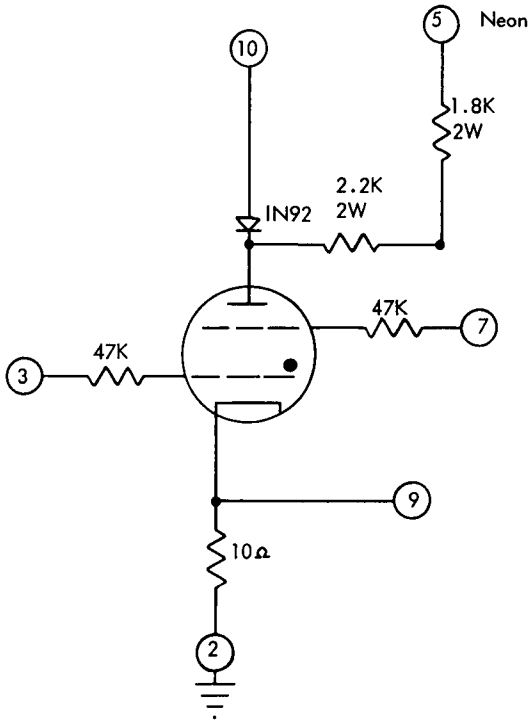


FIGURE D31. THYRATRON (TH509)

2.05.02 TH515

The TH515 is supplied +150 volts through a CB to the plate circuit. The input is to grid one at pin 8. The circuit may be used as an ATH if both grids are controlled. Pin 4 can be controlled by a clamping tube. The cathode is supplied by a divider between ground and +150 volts. Two neon outputs are provided. The output is a sharp negative shift through the capacitor and diode in pin 7.

2.05.03 TH524

Output of the TH524 is full plate through a .01 mfd capacitor. The tube can be fired by coincident pulses on both grids, or it may be used as an ATH if both grids are controlled.

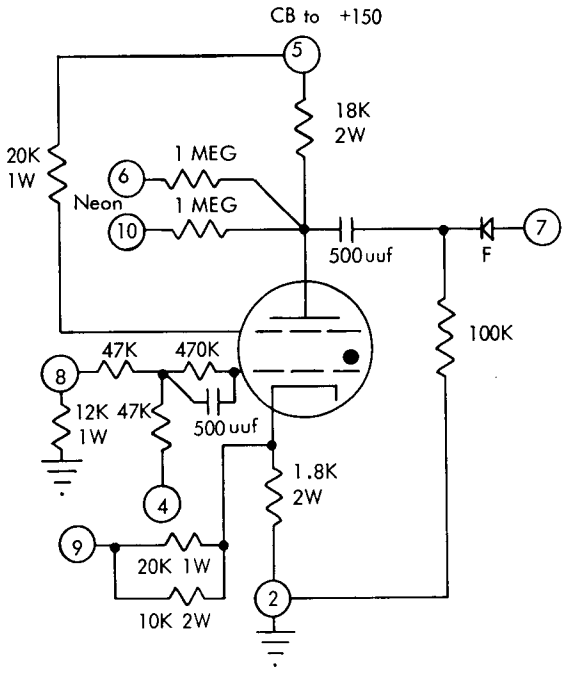


FIGURE D32. THYRATRON (TH515)

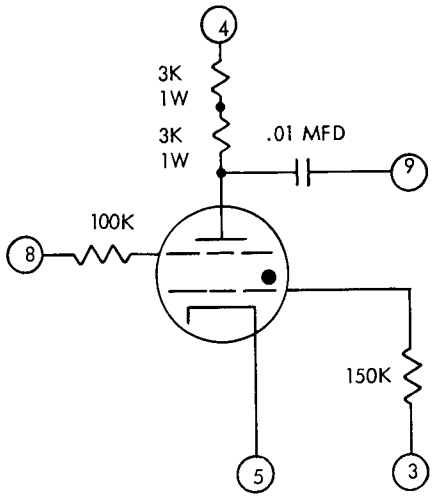


FIGURE D33. THYRATRON (TH524)

2.05.04 TH525

The TH525 plate is supplied +150 volts through a CB. The cathode is returned to about +30 volts by a divider. Plate divider output is used. Divider inputs are used at both grids.

2.06.00 TRIGGERS

The basic trigger is described in section 2.06.00, Book A.

2.06.01 TR506

The TR506 is similar in operation to the T_C or T_K of Book C. The TR506 uses a negative shift input through the 33 uuf capacitor in the grid circuit. A plate divider output is used.

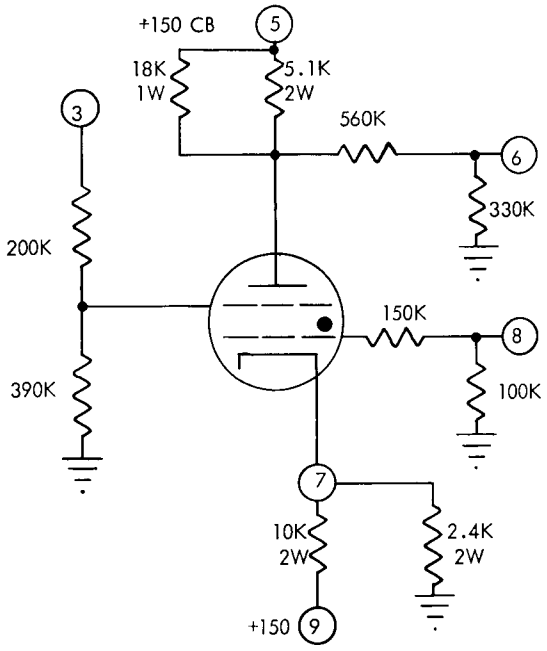


FIGURE D34. THYRATRON (TH525)

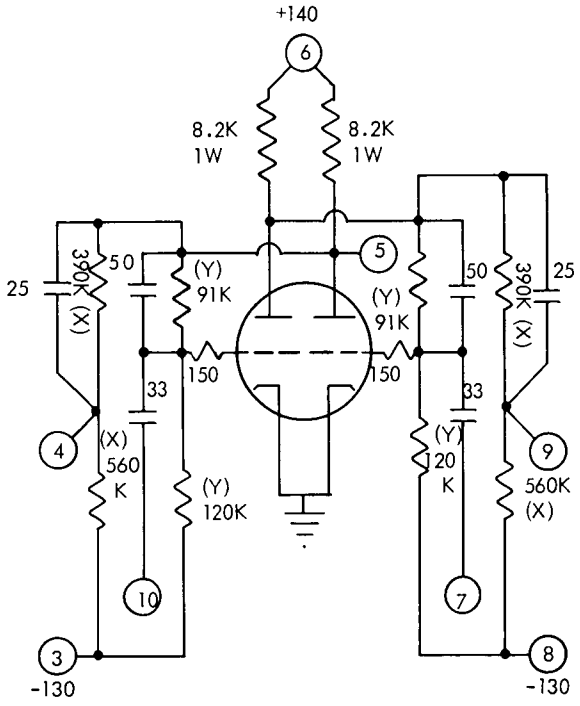


FIGURE D35. TRIGGER (TR506)

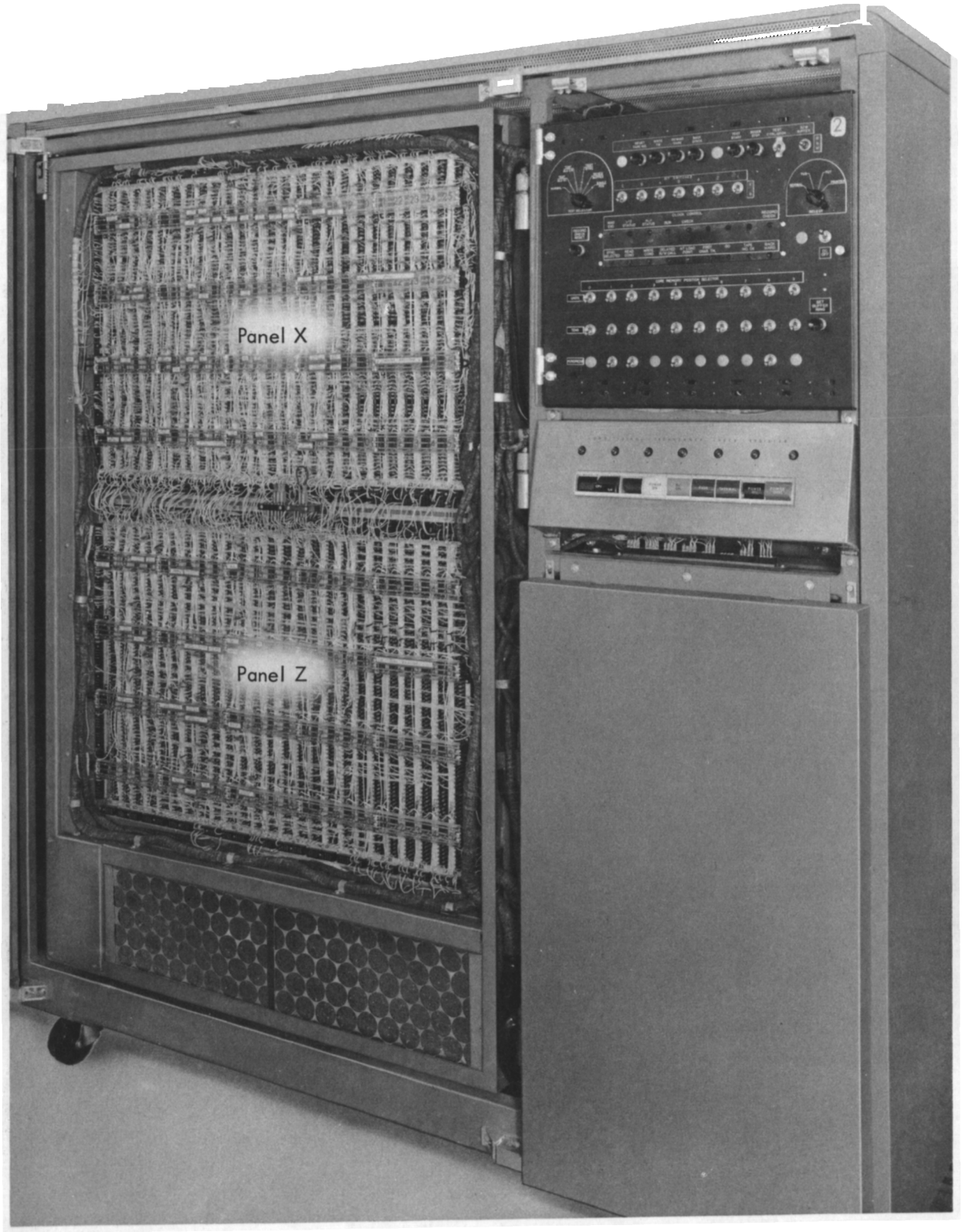


FIGURE D36. 760 CONTROL AND STORAGE UNIT, FRONT VIEW

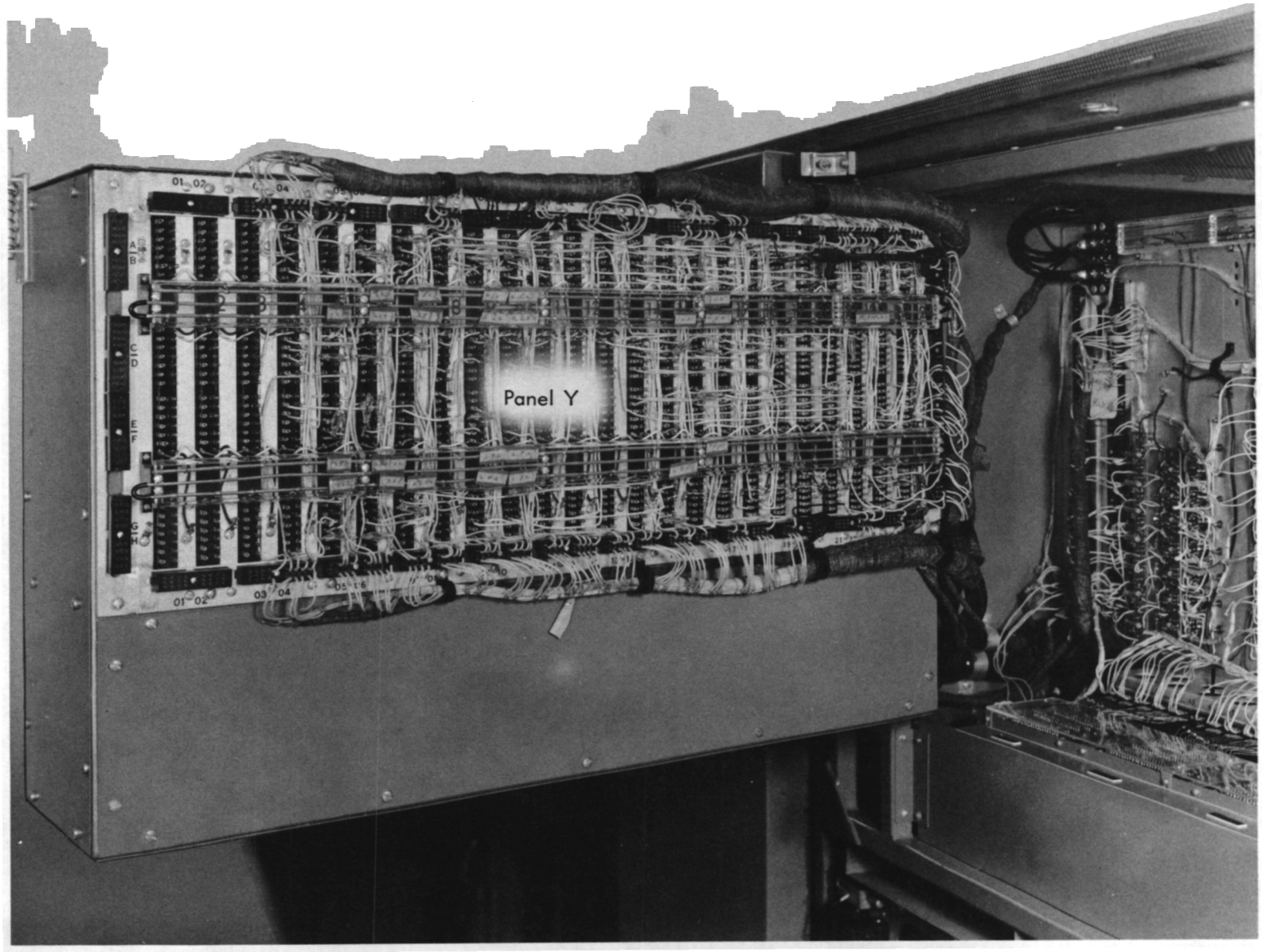


FIGURE D37. 760, Y PANEL

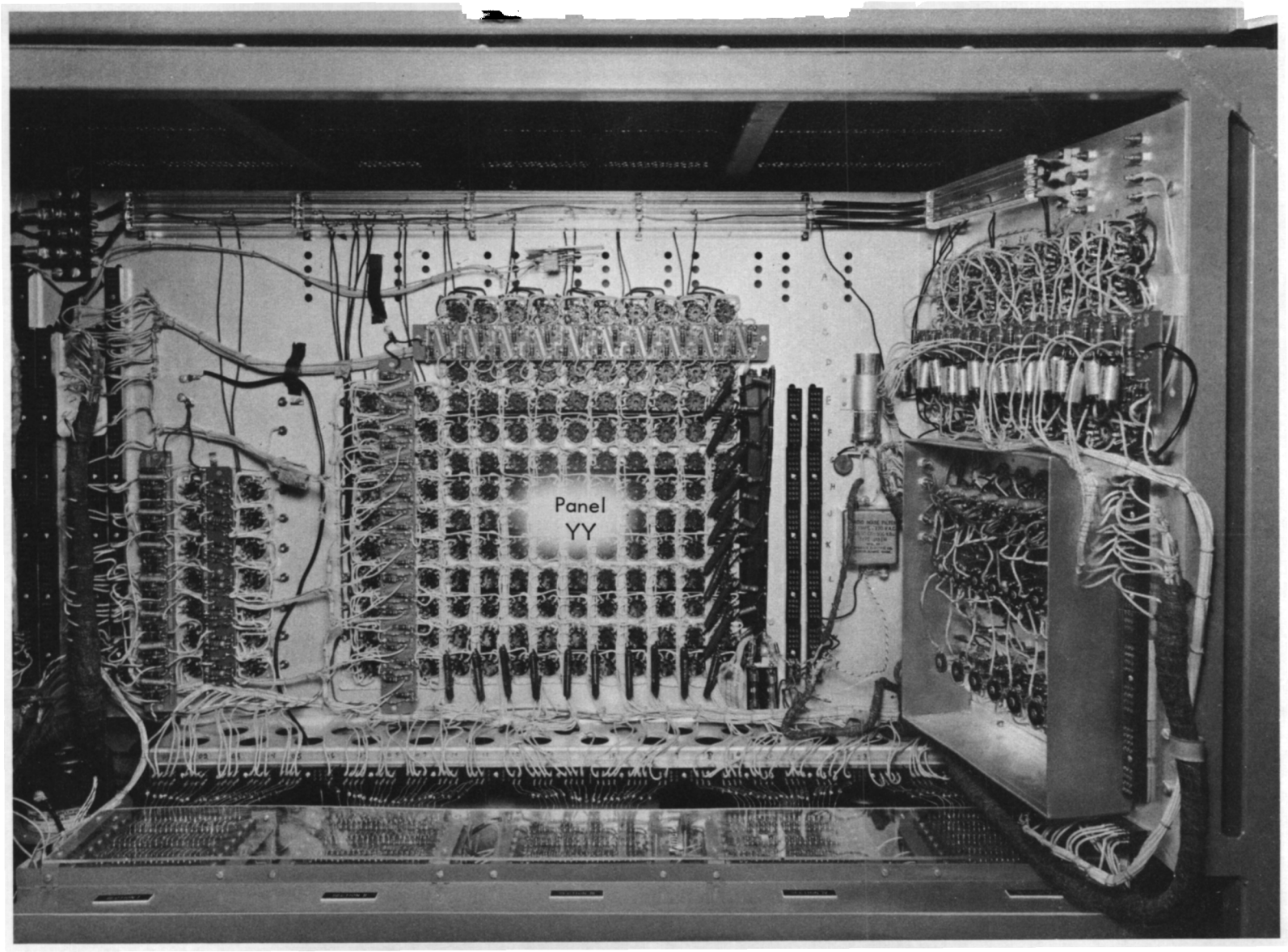


FIGURE D38. 760, YY PANEL

3.00.00 760 CONTROL AND STORAGE UNIT

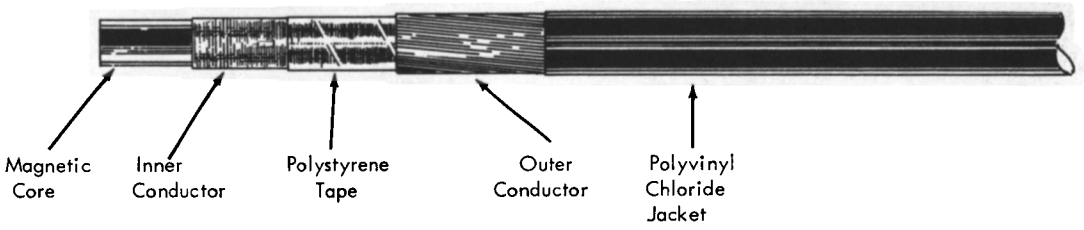
3.01.00 PLUGGABLE UNIT LOCATION

The pluggable unit panels in the 760 are designated panel X, panel Z, panel Y, and panel YY. Panels X and Z are located on the front gate of the 760. They are composed of standard 700-series pluggable units and include the control circuits, registers and timing circuits. The Y and YY panels are on the back of the machine in the upper right hand section (facing the back of the machine). These panels contain circuits necessary for putting information into the record storage unit. The 3X section of the 760 Systems Manual shows the composition of the four pluggable unit panels.

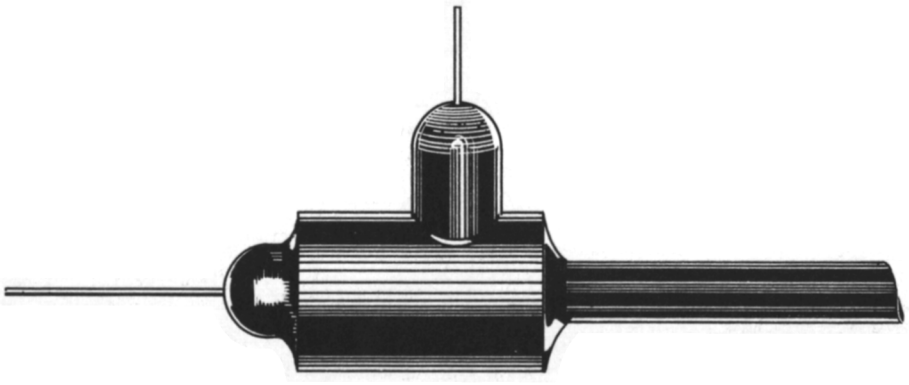
3.02.00 DELAY CIRCUITS

3.02.01 Delay Line (DL_D)

The delay line used in the 760 is a Columbia Technical Corporation type HH1600 or equivalent. It consists of a flexible magnetic core around which the inner conductor is closely wound. Covering the inner conductor is a dielectric made up of four overlapping layers of polystyrene tape. The outer conductor consists of spirally-wound wires covered by a polyvinyl chloride jacket to protect the assembly against moisture and abrasion. The ends of the line are capped and the conductors are brought out with No. 18 tinned leads.



Cut-away section HH-4000 Delay Cable



End cap with inner and outer winding connections

FIGURE D39. DELAY LINE, DL_D

3.03.00 CURRENT DRIVERS

3.03.01 Current Driver Matrix (CD_M)

The current drivers CD_M, (Figure D40) are used to supply the current to set switch cores in the buffer memory of the 760. The circuit uses a full 6350 twin triode. For a complete understanding of how the CD_M sets the switch cores consult the systems diagrams of the circuits involved. The CD_M merely acts as a current switch to supply current to the cores when the grid potential is brought to a level where the tube conducts.

When the CD_M is used for the direct drive (X lines), a 200-uuf condenser is tied from grid to ground to improve the shape of the output current pulse by slowing the rise of the grid. Where this is done, the condenser is shown outside of the block symbol.

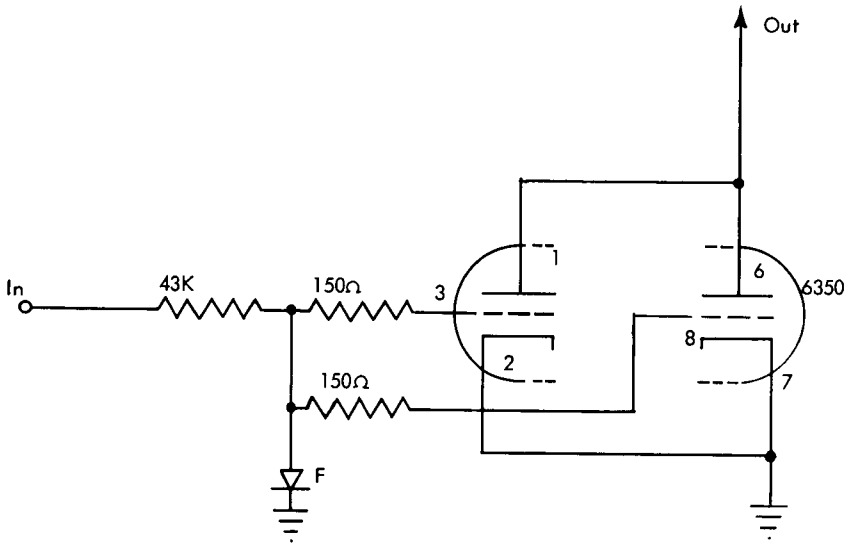
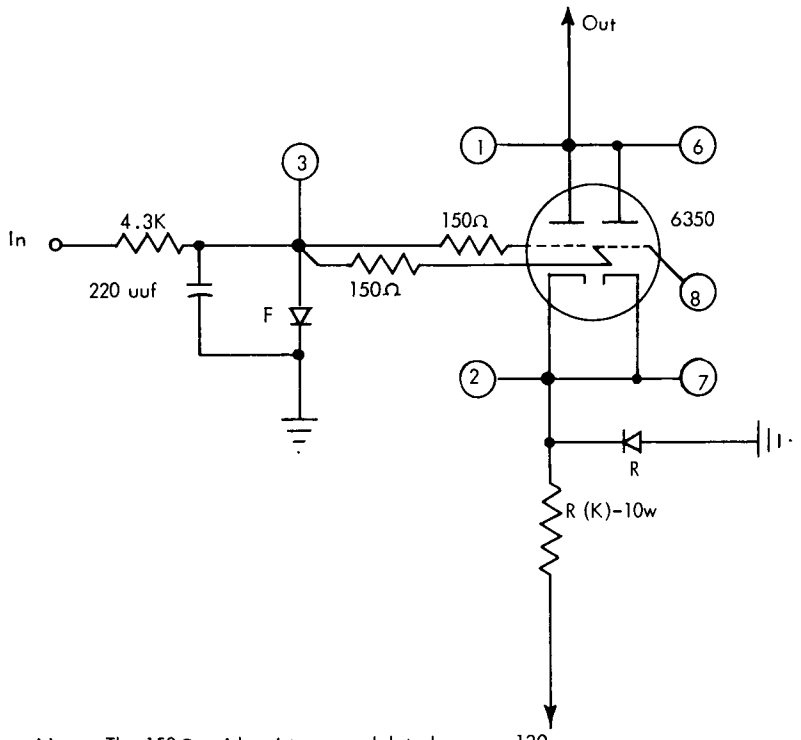


FIGURE D40. CURRENT DRIVER, MATRIX (CD_M)

3.03.02 Current Driver, Core (CD_C)

The current driver (core), CD_C, (Figure D41) is used to supply inhibit current to switch cores. The function of such a current driver is to supply a current which is constant, and reasonably independent of tube variations. Circuit operation is as follows.

When the input voltage is down, the cathode potential is maintained near ground by the ground-clamping diode. The clamping diode used is a type R diode. This diode is a gold-bonded transistor with low forward resistance and good recovery characteristics. When the input voltage is brought up to ground, it is diode-clamped to keep it from going above this potential; the current through the cathode load resistor switches from the diode to the tube. The current switch is affected by the cathode's going more positive than ground as the tube operates under a few volts bias. The 220-uuf condenser at the input slows the rise of the input voltage, and decreases any tendency to overshoot. The two half-tubes in parallel draw approximately 54 ma when conducting.



Note: The 150Ω grid resistors are deleted in the 775 and 760 because of printed circuit space limitations.

FIGURE D41. CURRENT DRIVER, CORE (CD_C)

3.04.00 AMPLIFIERS

3.04.01 Read Amplifier, Core (AR_C)

The read amplifier (core), AR_C, (Figure D42) is used to sense the output of the buffer memory in the 760. The AR_C is composed of a pentode driving a triode which in turn is AC-coupled to a standard cathode follower (K). The input of the AR_C is the rectified output of a pulse transformer. The rectifier is composed of the secondary of the pulse transformer and two type F diodes. The rectified signal is applied to the grid of the class-A-operated triode-connected pentode. The bias for this stage is obtained by a by-passed cathode resistor.

The first stage of the amplifier has a gain of about 15 while the second stage has a gain of approximately 8 for an overall gain of approximately 120. Thus the 500mv signal at the grid of the first stage is amplified to a 60v signal at the output of the amplifier. These figures are only approximate, of course, since different core and pulse transformer combinations can be expected to produce larger or smaller input signals to the amplifier.

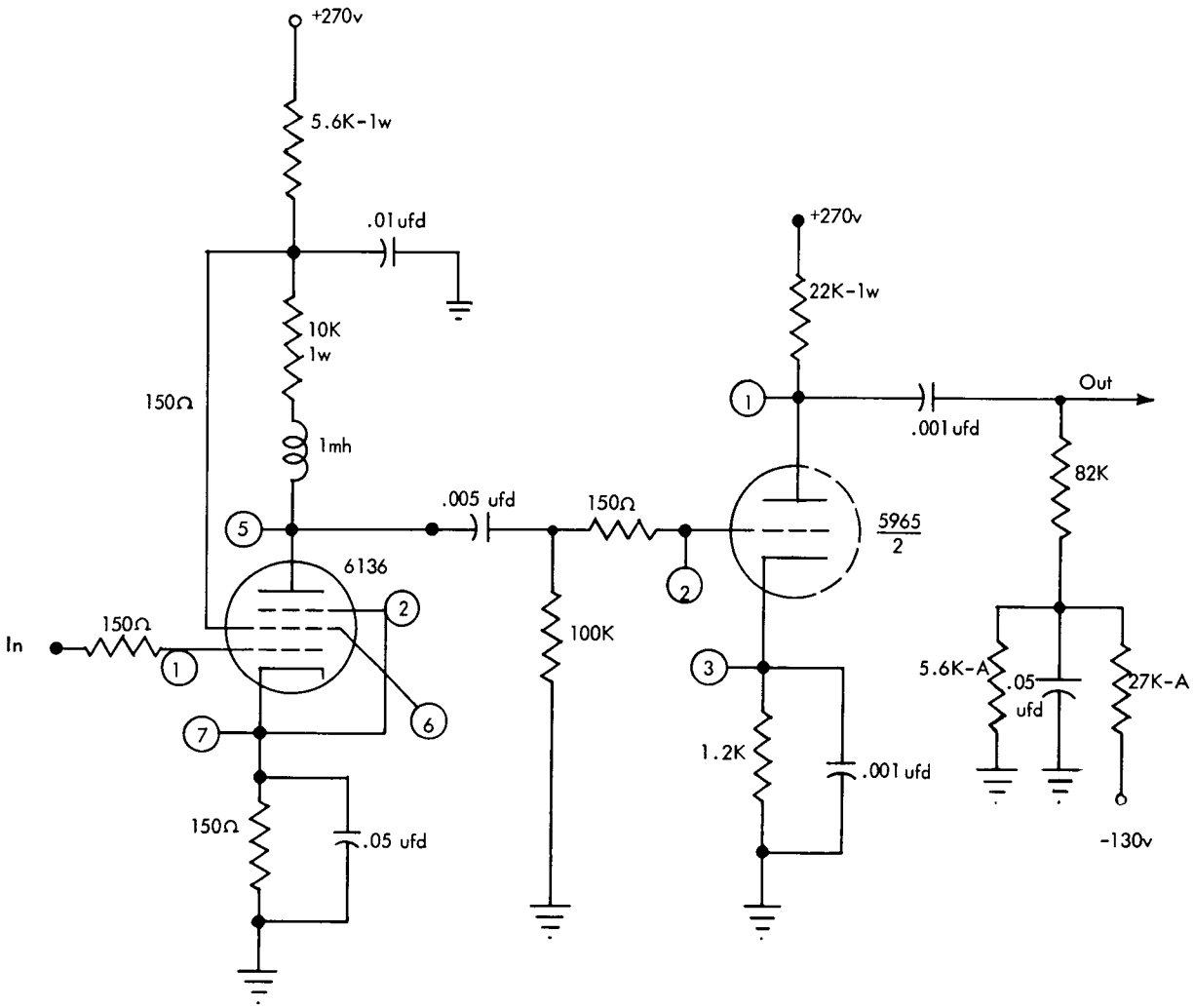


FIGURE D42. READ AMPLIFIER, CORE - AR_C

3.05.00 INVERTER, PULL-OVER BUFFER (I_{PB})

The I_{PB} is the pull-over inverter for the 760 Control and Storage.

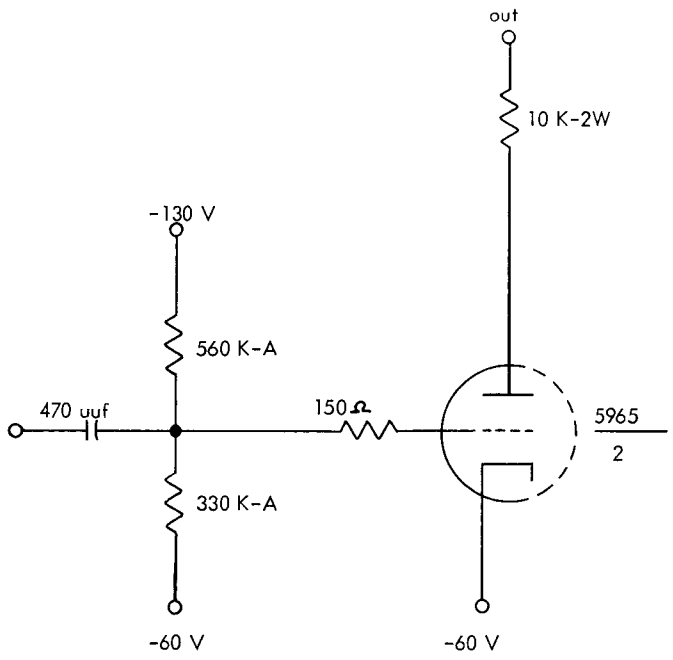


FIGURE D43. PULL-OVER INVERTER--I_{PB}

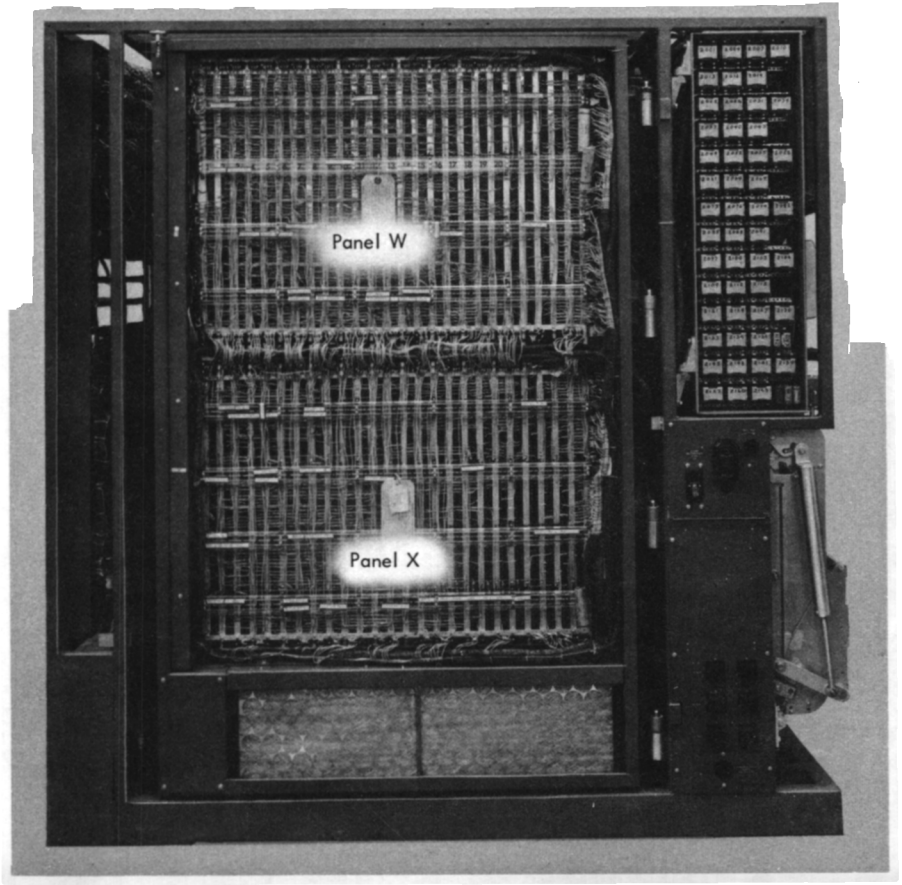


FIGURE D44. 774 PLUGGABLE UNIT PANEL
(Left Side View)

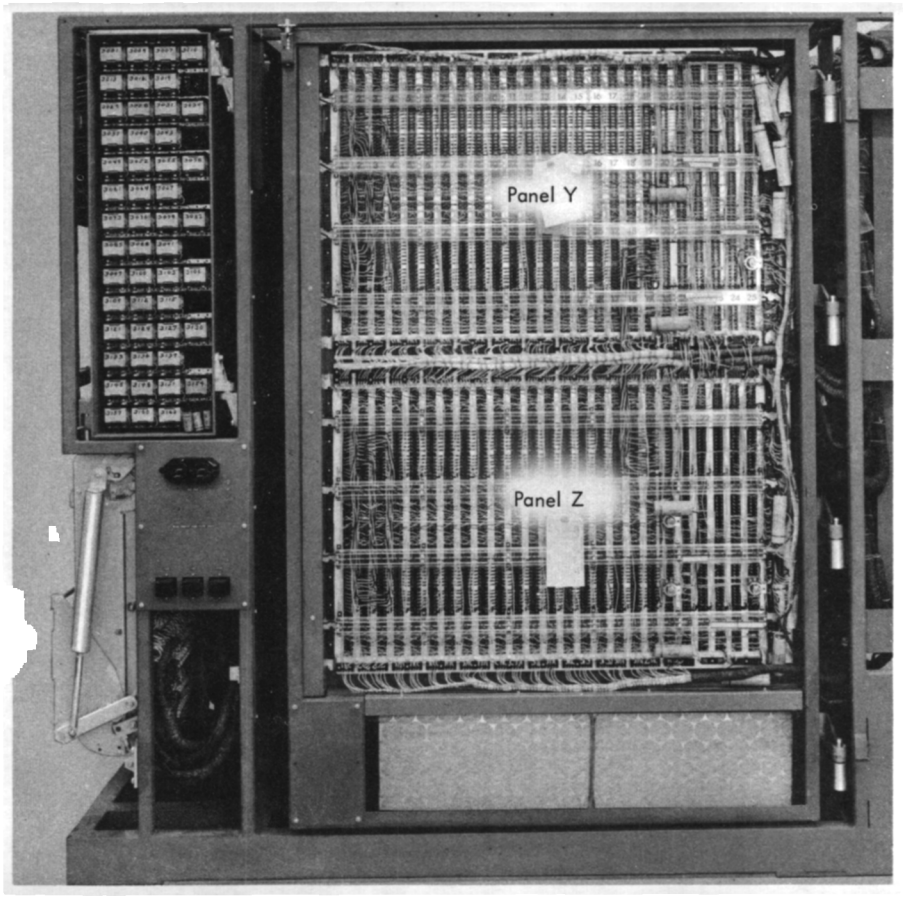
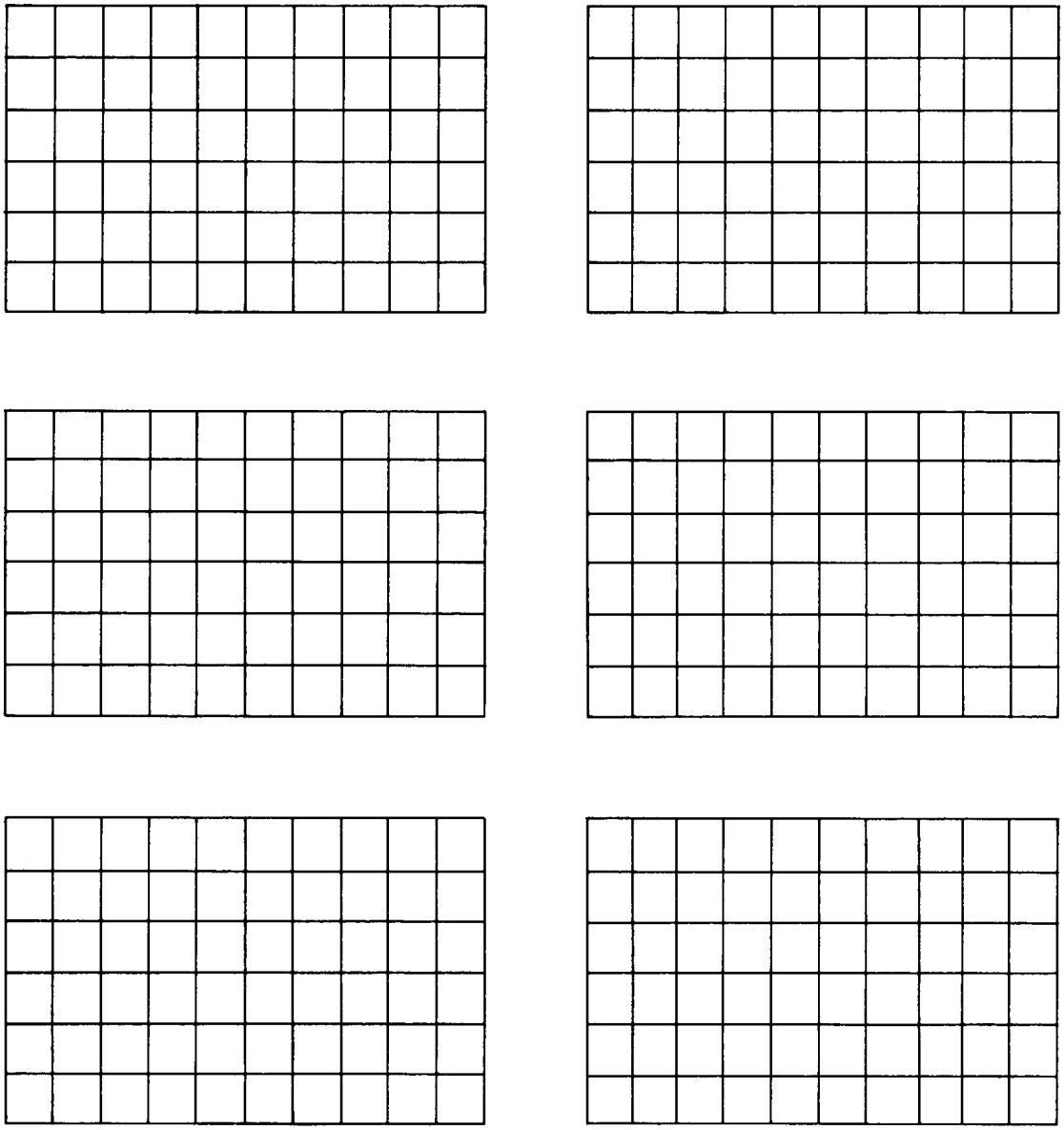


FIGURE D45. 774 PLUGGABLE UNIT PANEL
(Right Side View)

4.00.00 TAPE DATA SELECTOR (774)

The 774 has two gates housing the pluggable units. The left pluggable unit gate (facing the front of the machine) contains all 12v filament tubes and is divided into two sections: the W panel (top section), and the X panel (bottom section). This gate is referred to as the control gate. The memory gate (right gate facing the front of the machine) has six-volt filament tubes. The two sections of this gate are panel Y (top section) and panel Z (bottom section).

Component circuits used in the 774 are standard circuits explained in other sections of this volume (with the exception of those circuits included in this section).



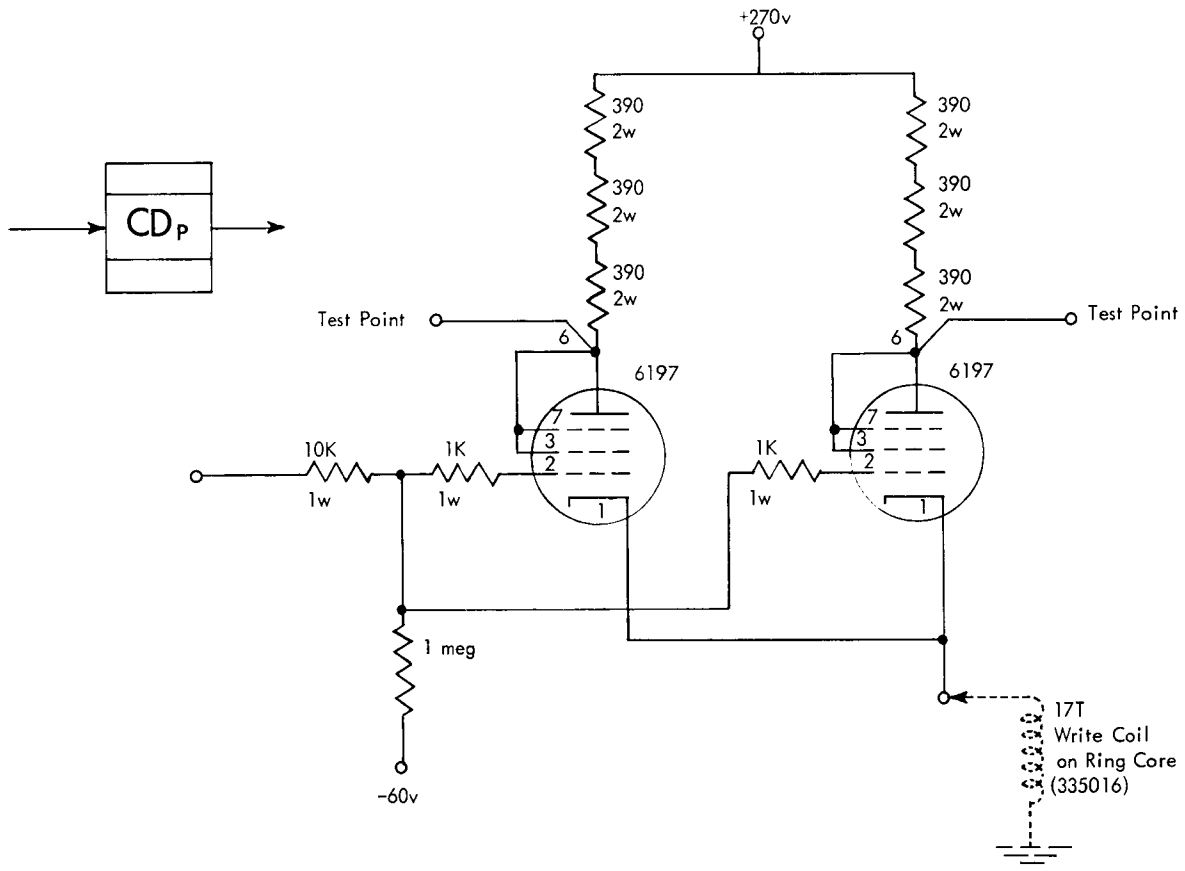
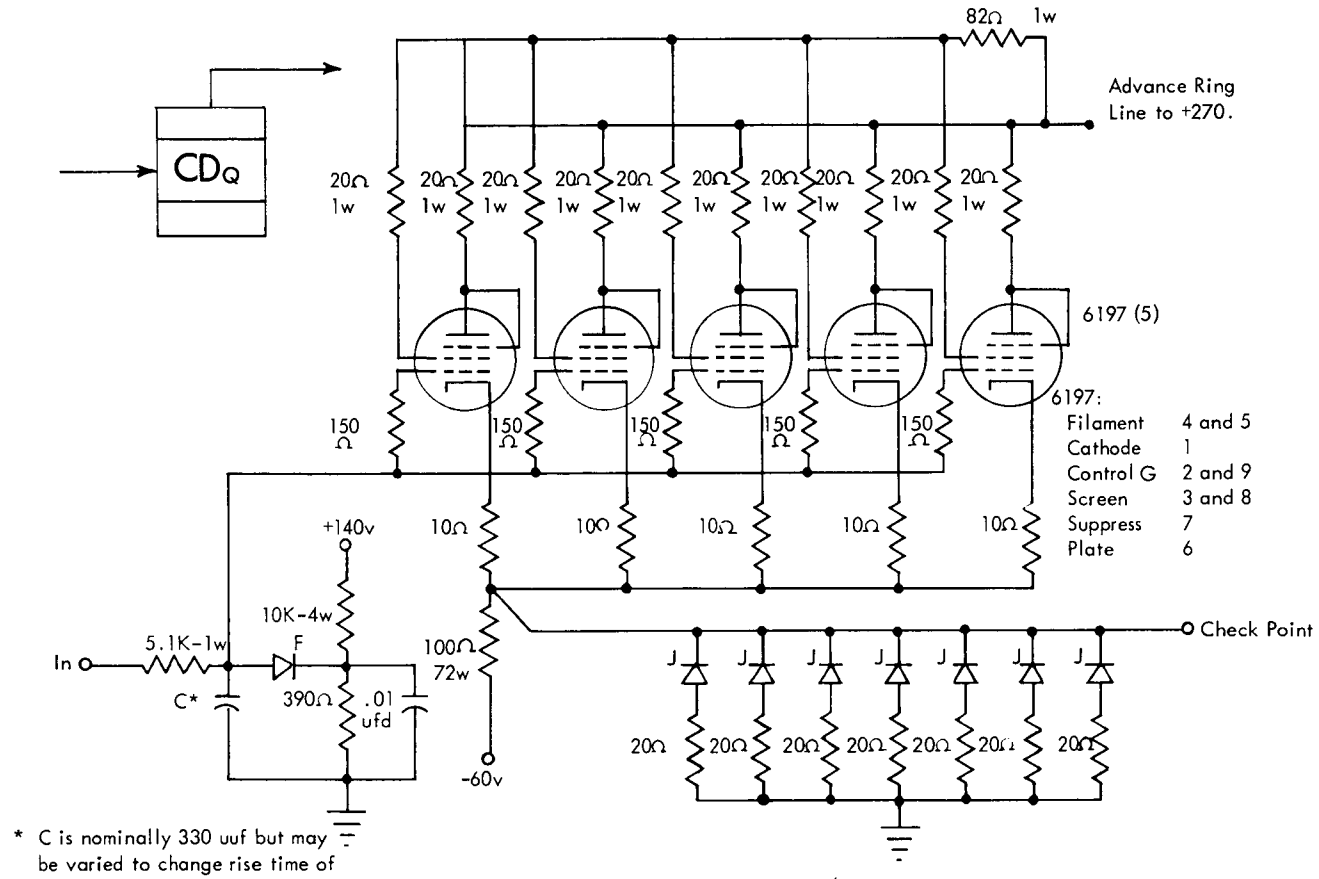


FIGURE D46. RING PRIME CURRENT DRIVER (CDp)



* C is nominally 330 uuf but may be varied to change rise time of output current pulse.

FIGURE D47. RING CURRENT DRIVER (CD_Q)

4.01.00 CURRENT DRIVERS

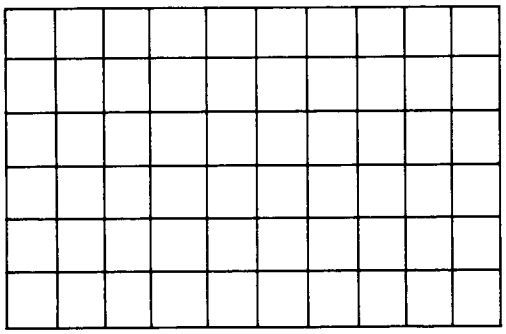
4.01.01 Ring Prime Current Driver (CD_P)

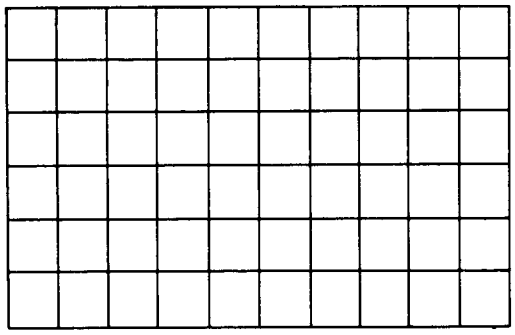
The CD_P is used in the 774 to prime the home position ring core at the beginning of the reset-before-run-in operation and again at the very end of the reset-before-run-in operation. At all other times, the home position ring core is primed with its own TH_H through a normally closed carry-relay point.

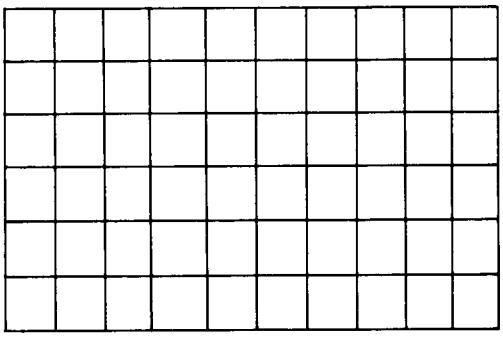
The CD_P consists of two 6197 tubes coupled in parallel with their cathodes tied together. The 17-turn winding of the home position ring core is in series between the common cathodes and ground potential. When a -30v signal is applied to the parallel-grid circuit, the tubes are cut off and the circuit has no affect on the ring core. When a +10v signal is applied to the grid circuit, the tubes are brought into conduction, causing about 200 ma of current to flow through the ring core. This current is of sufficient magnitude and polarity to set or prime the home position core. In each plate circuit is a 1170-ohm resistor to limit plate current. The grid circuit is returned to -60 volts through a one-megohm resistor to prevent the grid from floating in case the driving circuit is removed.

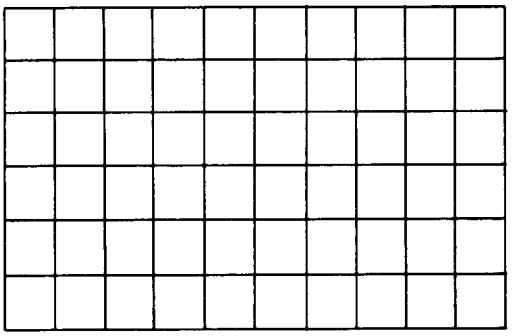
4.01.02 Ring Current Driver (CD_Q)

The ring current driver, CD_Q, is similar to the ring current driver CD_R (section 2.04.16, Book C). The important difference is in the grid circuit, which, in the CD_Q, is clamped at +5 volts to reduce the effect of noise on the output.









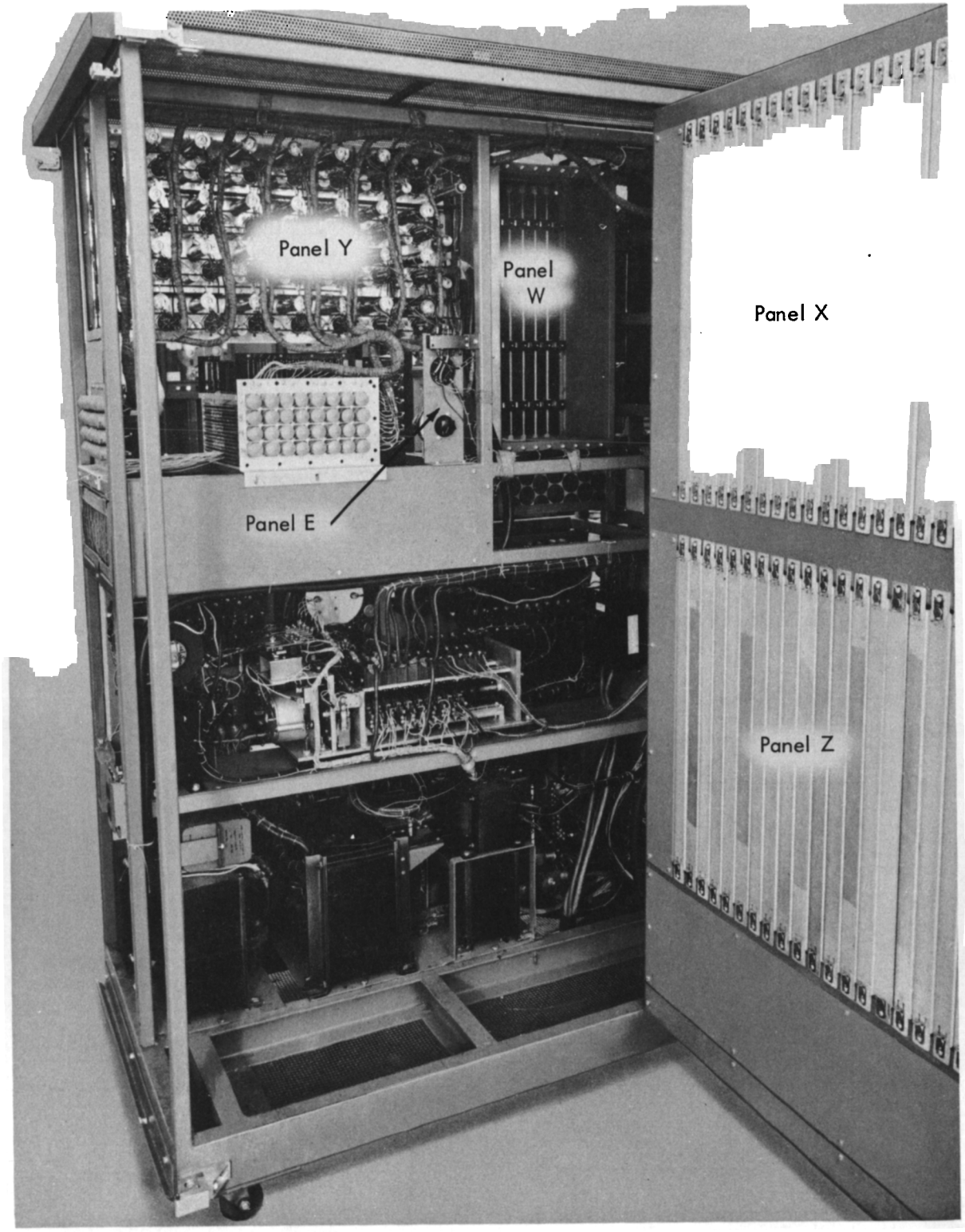


FIGURE D48. 777 PLUGGABLE UNIT PANEL
(Machine Front View)

5.00.00 TAPE RECORD COORDINATOR (777)

The tape record coordinator has five panels designated E, W, X, Y, and Z as illustrated in Figure D48.

5.00.01 TRC Panel Layout

Panel E

Panel E contains the four-ampere filament transformer that supplies the -150v regulator tube on panel Y. The potentiometers used to adjust the -150v supply are also mounted on panel E. No pluggable units are mounted on panel E.

Panel W

Panel W is a 20-pluggable unit gate containing the select circuits of the TRC. Only six spaces of the twenty available are used.

Panel X

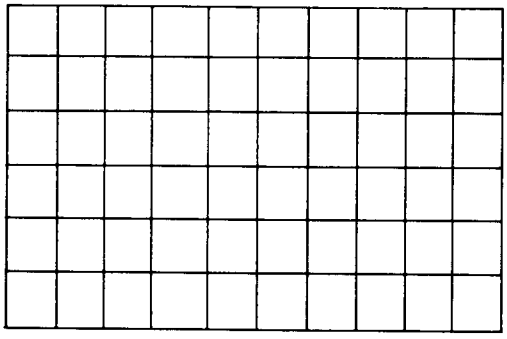
Panel X contains clock circuits, memory control circuits, sense amplifier circuits and CR1 and TC control circuits. Control sections of the -150v and -180v supplies are also on panel X.

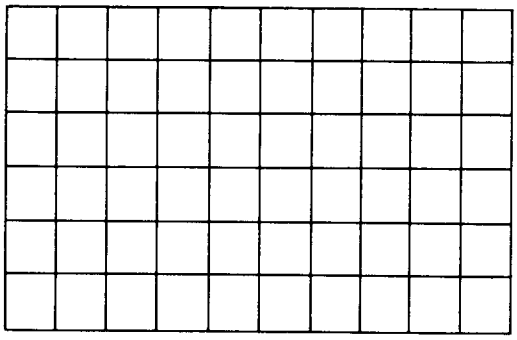
Panel Y

Panel Y contains the memory driver tubes and vector sockets. The regulator tube for the -150v supply is located on the Y panel at 8A.

Panel Z

Panel Z contains circuits for input switching to memory, final amplifier circuits and CR2A, CR2, tape and CPU control circuits.





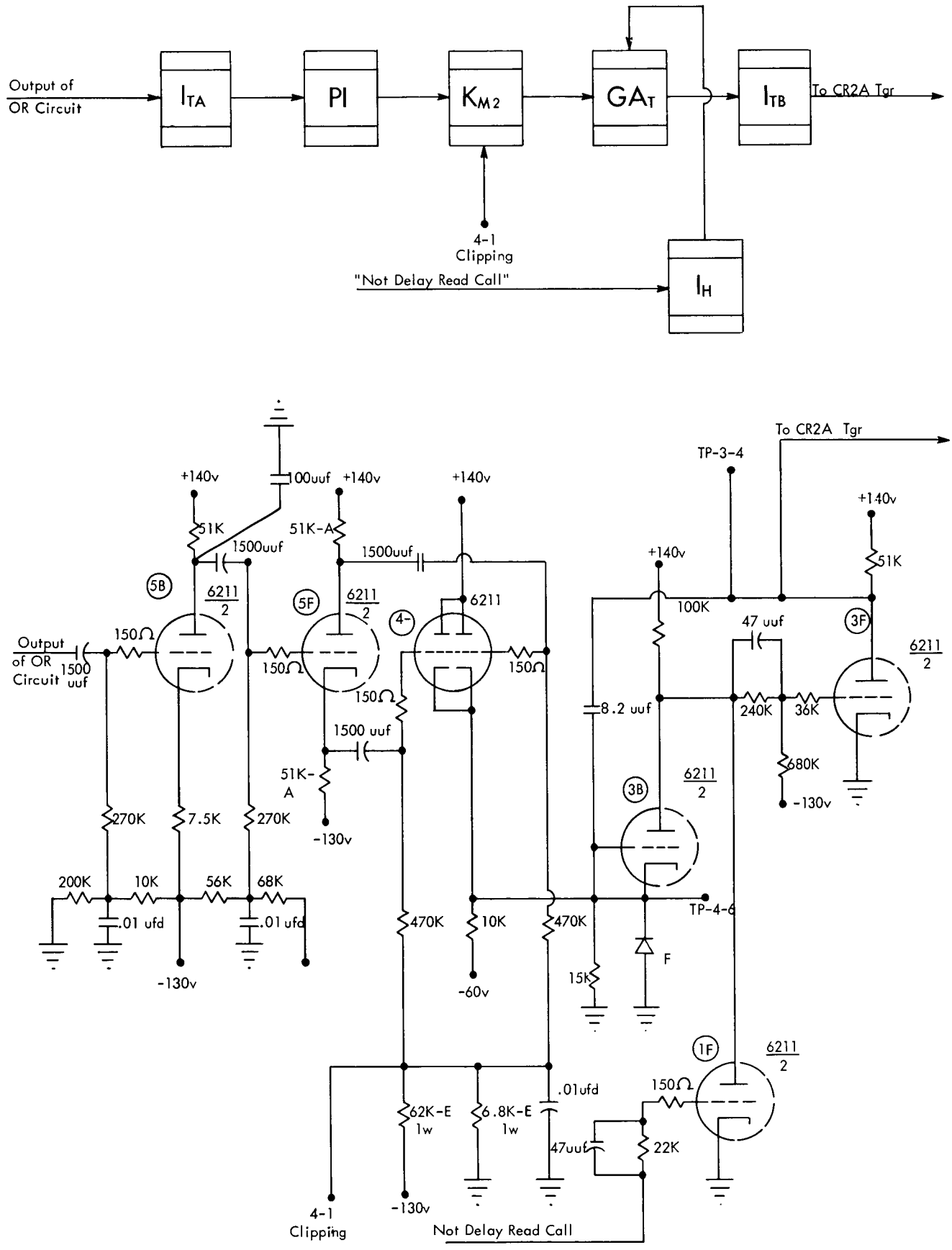


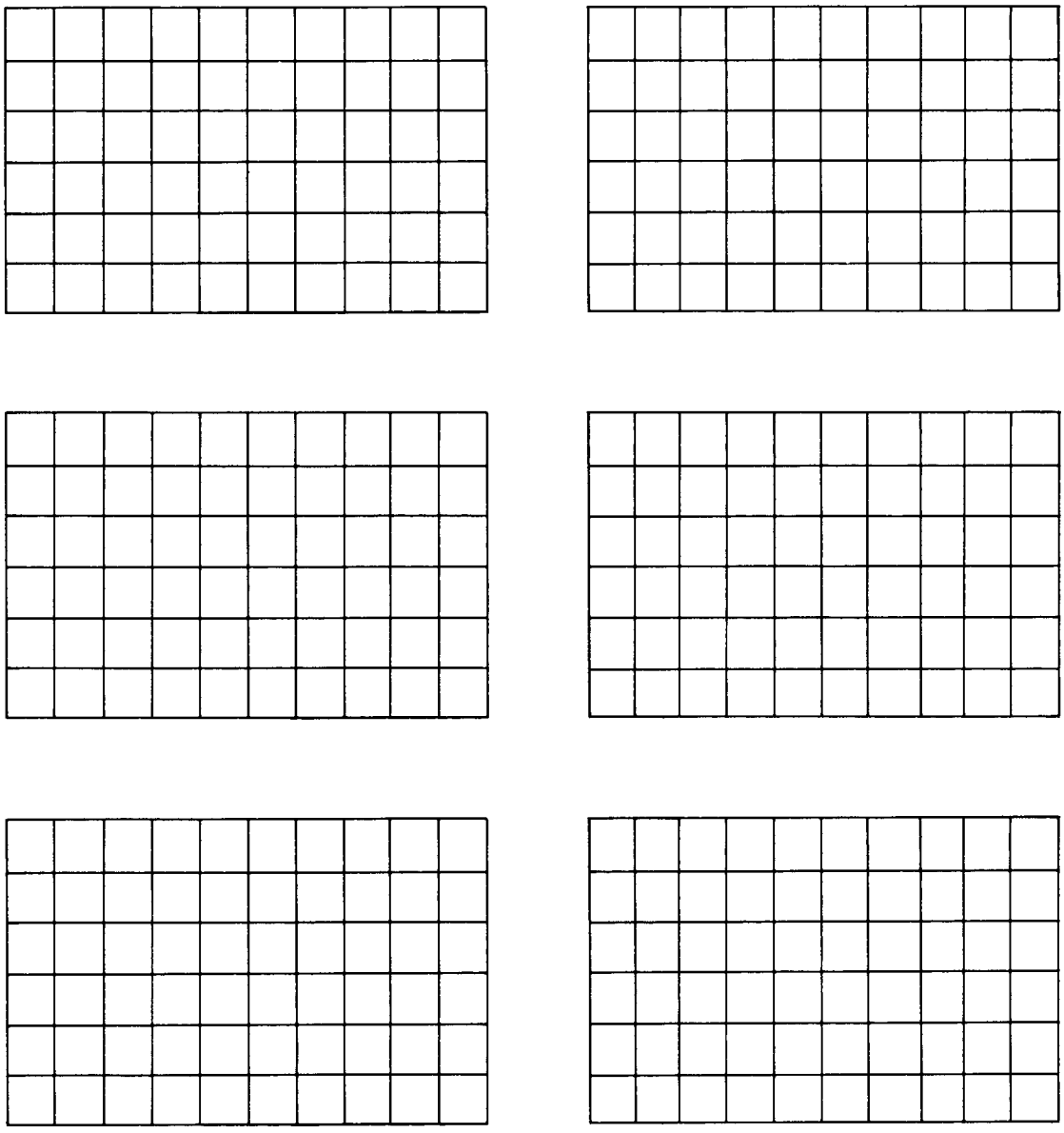
FIGURE D49. 777 FINAL AMPLIFIER (I_{TA}, PI, K_{M2}, GA_T, I_{TB}, I_H)

5.01.00 INVERTERS

5.01.01 777 Final Amplifier (I_{TA}, PI, K_{M2}, GA_T, I_{TB}, I_H)

The 777 final amplifier (Figure D49) is similar in operation to the final amplifier (section 2.01.20, Book C).

The cathode follower mixer is designated K_{M2} because of the different voltage divider network in the grid circuit.



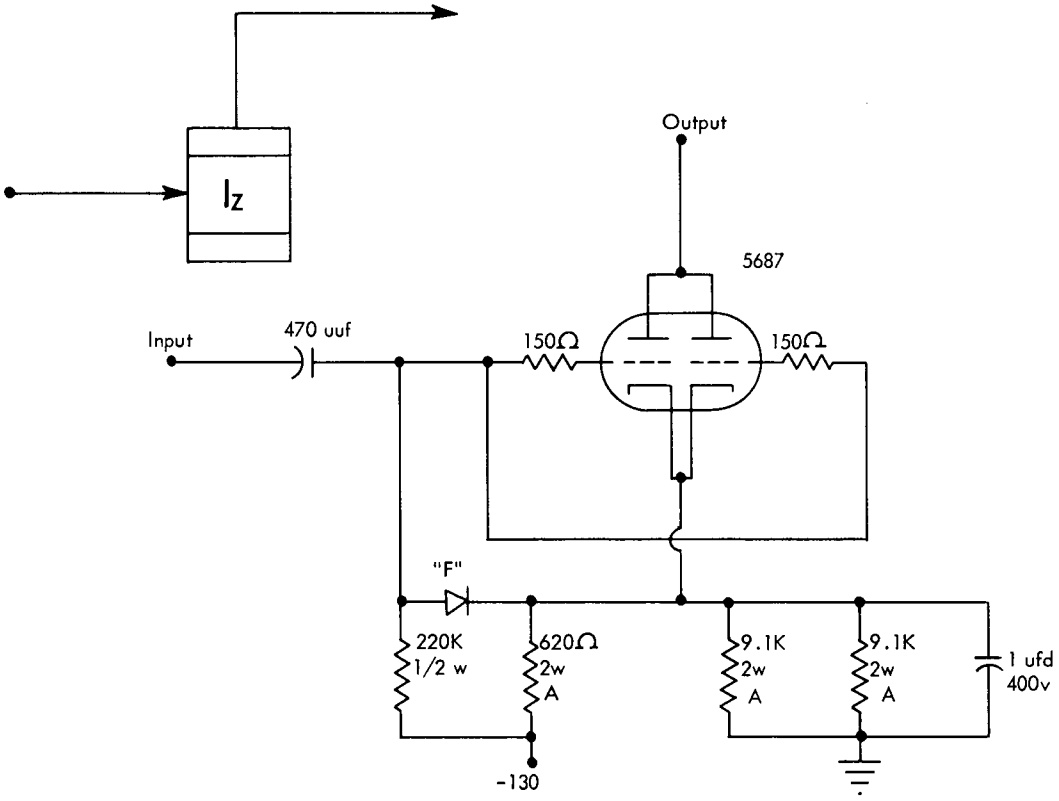
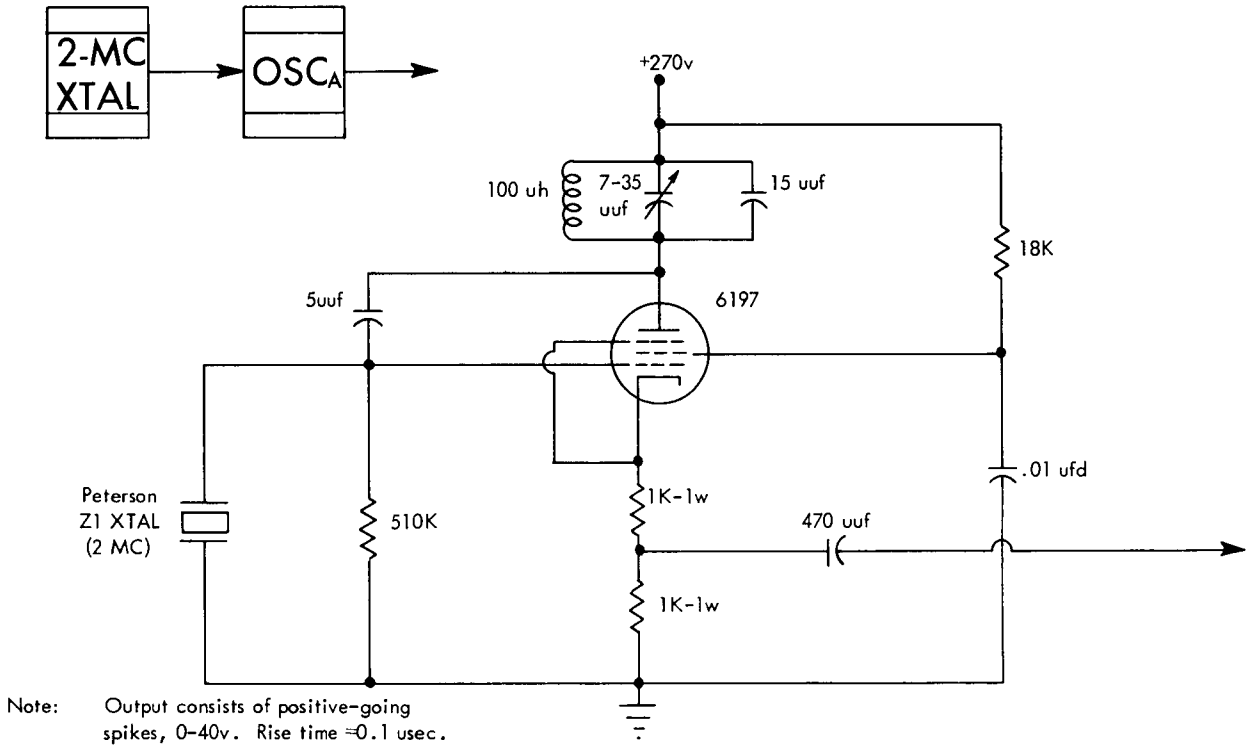


FIGURE D50. HIGH CAPACITY PULL-DOWN INVERTER (I_Z)



Note: Output consists of positive-going spikes, 0-40v. Rise time ≈0.1 usec.

FIGURE D51. 2MC OSCILLATOR FOR CLOCK (OSC_A)

5.01.02 High-Capacity Pull-Down Inverter (I_Z)

Circuit Description (Figure D50)

If the output is at -30 volts and the grid is quiescent, the tube does not conduct. If it is at -30 volts and the grid is pulsed, the tube conducts very minutely. If the grid is pulsed when the bus is at +10 volts, the tube conducts heavily and pulls down the bus voltage. The voltage divider network between ground and -130 volts holds the cathode at -112 volts to -115 volts. The grid stabilizes at about -130 volts. When conducting, the cathode rises to about -106 volts. The 0.1-ufd capacitor is used to damp bouncing effect at the cathode. The diode stabilizes grid bias.

TRC Operation

TRC and CPU operation must transfer characters in consecutive 9-usec cycles. Because of this, TRC does not operate with the delay (in fall time of the I/O read buses) caused by shunt capacitance to ground in the cable. The high-capacity pull-down circuit (I_Z) is used to reduce the fall time of the read buses during TRC operation. When a TRC is selected, the I_Z is pulsed every nine usec by an R2 (D2) pulse in CPU. The pulse comes after sample time and causes I_Z to pull the bus voltage down to -27 volts in approximately 2.2 usec. In actual operation the plate of the I_Z is tied directly to the I/O bus.

DS Operation

In the DS, the I_Z plate is tied directly to the tape write bus. The I_Z causes the tape write bus voltage to fall rapidly after write pulse time. This yanking action is necessary because of the short write interval of the 729 III tape unit (16 usec). The yanking assures that the bits are removed from the bus before the next write pulse.

5.02.00 PULSE GENERATORS

5.02.01 2MC Oscillator for Clock (OSC_A)

The oscillator OSC_A (Figure D51) is similar in operation to the oscillator OSC (section 2.13.00, Book A).

The signal on the grid of the OSC_A varies from +60 volts to -60 volts while the plate wave form, a slightly distorted sine wave of about 250 volts, varies from +100 volts to +350 volts. The output from this oscillator is a positive pulse of 40 volts from the divider network in the cathode circuit.

Component Circuits

Book E. Appendix

CONTENTS

1.00.00 GENERAL INFORMATION

1.01.00 BASIC ELECTRONICS

The following is a brief review of some of the basic concepts of electronics.

1.01.01 Definitions and Laws

Electricity is composed of charges and current.

Charges. The presence of an excess of free electrons or the absence of some or all of the free electrons normally on the charged body. An electric charge will be lost unless it is on a good insulator or an insulated conductor.

Current. The number of electrons flowing past a given point during a specified time interval. Currents usually encountered involve large numbers of electrons. (one ampere is defined as 6.2×10^{18} electrons per second).

The quantities usually measured are defined below.

Voltage. A measure of the relative excess (-) or deficiency (+) of electrons of a point. Some other point is always used as a reference. It also is a measure of the force with which electrons will travel between the two reference points if a conducting path is provided. Voltage is very nearly analagous to pressure in fluid mechanics.

Current (previously discussed). The rate of flow of electrons past a point (or along a wire). It is analogous to flow rate in fluid mechanics.

Current x Time = Charge

Charge (measured in coulombs). One coulomb = one ampere for one second or 6.2×10^{18} electrons.

Power (measured in watts).	One Watt	= 1/746 hp.
	Volts x Amperes	= Watts.
	(Pressure x Current Flow	= Power)

Resistance (and Impedance). Measured in ohms. It is the factor that determines the voltage required to produce a given current flow (just as the size and length of a pipe determines the pressure required for a given flow rate.)

Laws pertinent to this discussion are given below.

Ohm's Law: Voltage = Current x Resistance.

$E = IR$

also $I = E/R$

$R = E/I$

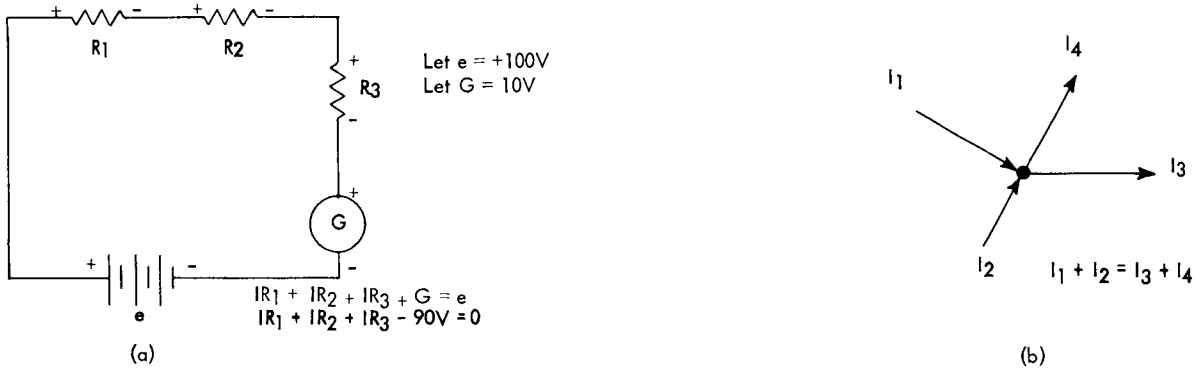


FIGURE E1. KIRCHHOFF'S LAW

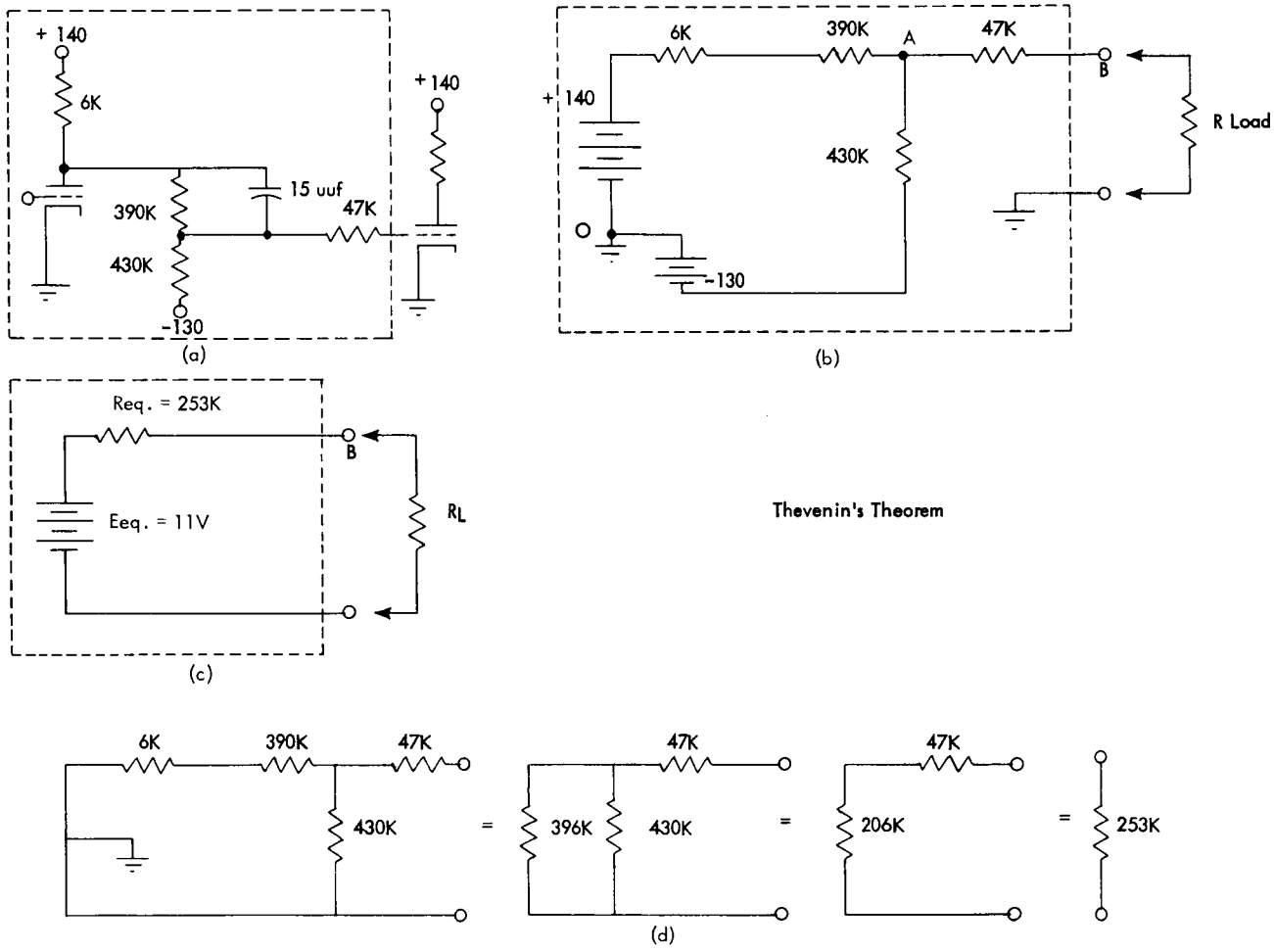


FIGURE E2. THEVENIN'S THEOREM

Power Relationships. From Ohm's Law and the power law, the following evolves.

Power = Voltage x Current

$P = EI$

$P = I^2R$

$P = E^2/R$

Kirchhoff's Laws.

1. The sum of all voltages around a closed loop (circuit) is zero (Figure E1a). Let R_1, R_2, R_3 be any three resistances. The voltage across them, $IR1 + IR_2 + IR_3 = E-G = 90v$, or $IR_1 + IR_2 + IR_3 - 90v = 0$.

2. The total current flowing into and out of a junction must equal zero (Figure E1b). This is true for any number of wires in a junction.

Resistances in Series (also Inductors). If two or more resistances are connected in series, the total resistance is $R_1 + R_2$, and so on (the sum of all resistances in the circuit). The total resistance of a series circuit is always more than the largest resistance in the circuit. Voltage division in a series circuit is shown in Figures E3b and E3c.

Resistances in Parallel (also Inductors). If two or more resistances are connected in parallel, the total resistance between the two wires is R, where $1/R = 1/r_1 + 1/r_2 + 1/r_3$, and so on. The total resistance of a parallel circuit is always less than that of the smallest in the group.

Capacitors in Series. When two or more capacitors are placed in series with each other, the total capacitance is found by the reciprocal sum method (same as resistors in parallel). The total capacitance is always less than the smallest capacitor value. Voltage division in a series circuit is shown in Figure E3a.

Capacitors in Parallel. When two or more capacitors are placed in parallel, the total capacitance is the sum of the individual capacitors. Note that the above rules are the reverse of the resistor rules for addition of values.

Thevenin's Theorem. Any linear network containing one or more sources of voltages and having two terminals may be replaced by one equivalent voltage generator with an equivalent series impedance. At the two terminals the current and voltage delivered to a load by the simple generator and series impedance can be made identical to the voltage and current of the original network, if the two rules given below are followed.

1. The voltage of the equivalent generator is the voltage appearing at the output of the original network, with all load removed.
2. The series resistor (or impedance in an AC circuit) is the impedance measured at the terminals of the original network, with any voltage sources replaced by short circuits.

An example of this theorem is shown in Figure E2. Figure E2a shows a typical 705 divider circuit and Figure E2b shows the equivalent circuit. The 15-uuf capacitor can be ignored when the DC case is considered. The equivalent circuit (by Thevenin's Theorem) of the part enclosed in the dotted lines is shown in Figure E2c.

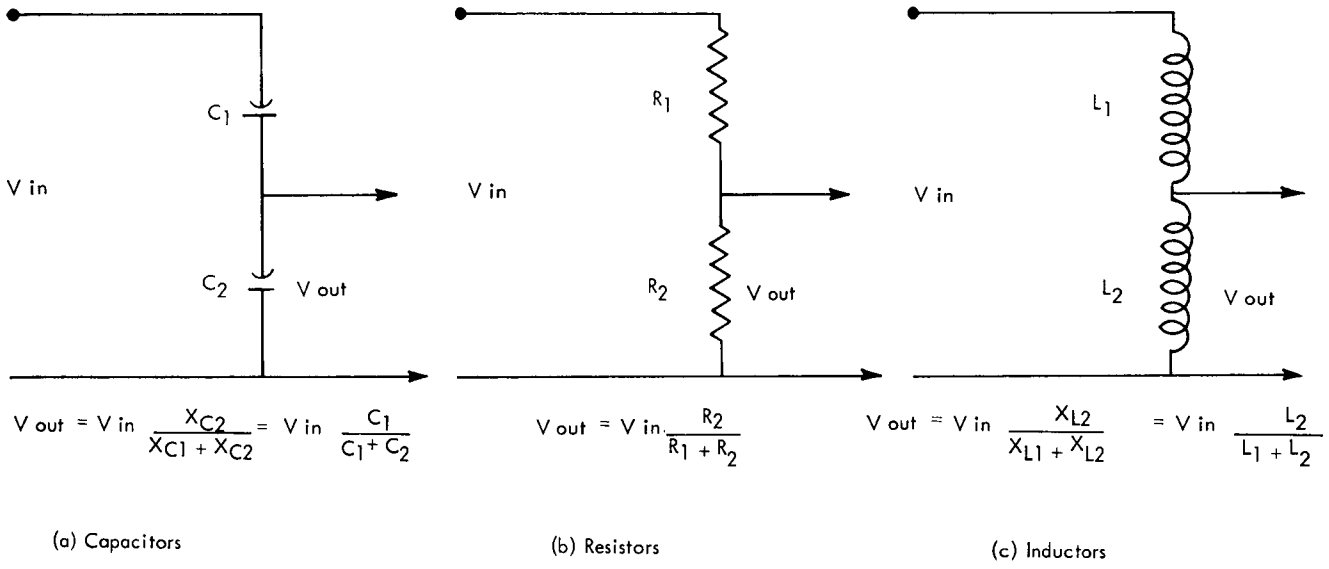


FIGURE E3. VOLTAGE DIVIDERS

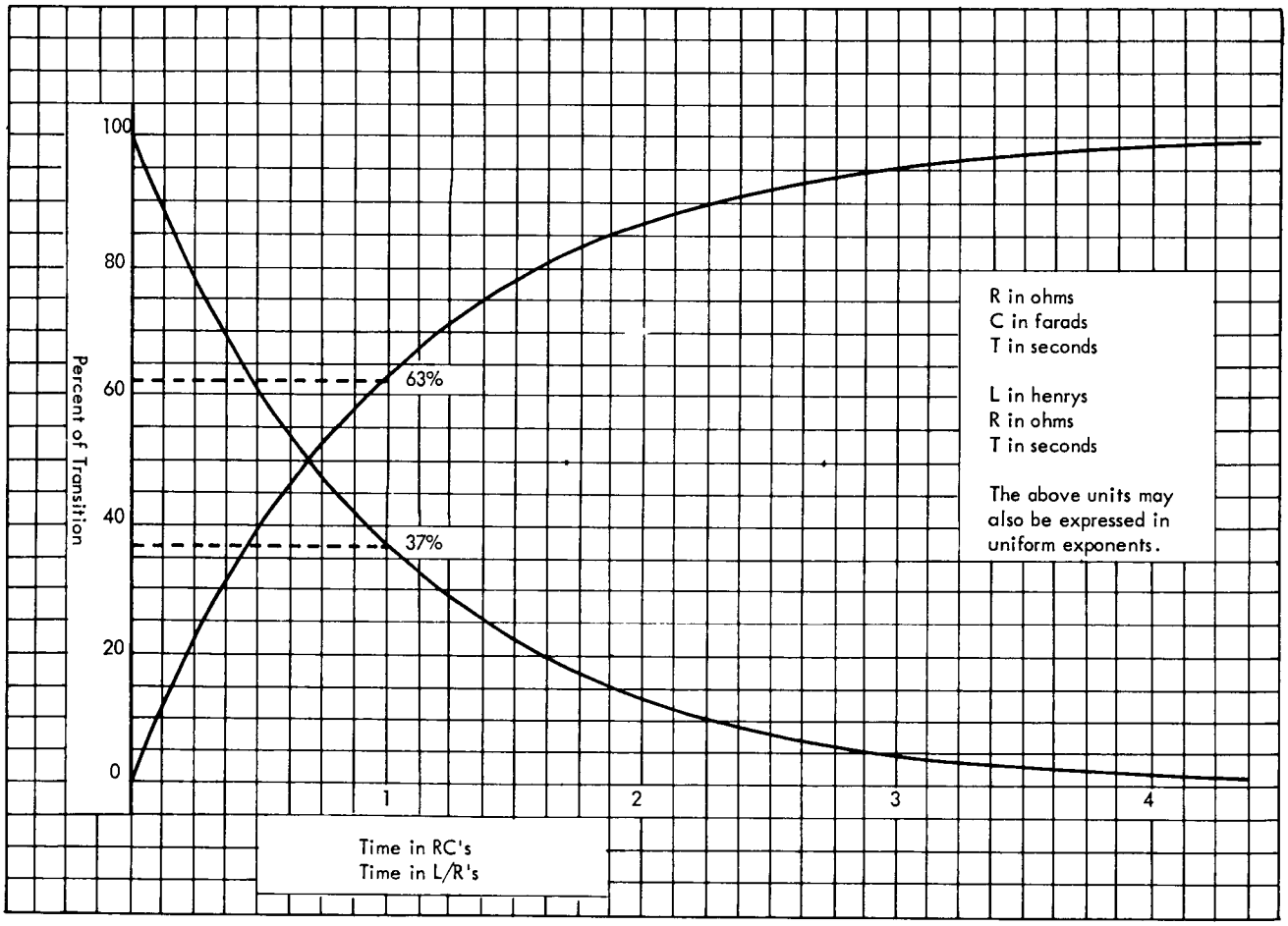


FIGURE E4. UNIVERSAL TIME CONSTANT CURVE

Equivalent voltage = output voltage of the original circuit with no load.

$$I = \frac{140 + 130}{(6 + 390 + 430) \times 10^3} = \frac{270}{826 \times 10^3} = 3.26 \times 10^{-4}$$

$$E_A = 140 - \left[3.26 \times 10^{-4} \times (390+6) \times 10^3\right]$$

$$E_A = 140 - 129 = 11v'$$

$E_B = E_A$ because the current through the 47K resistor is zero with no load.

Therefore, E equivalent = 11v.

To find R equivalent, replace the voltages with a short as shown in Figure E2d. Further simplifying gives R equivalent = 253K.

With these values, any load may be connected to the equivalent circuit and it will behave as the original. It has the advantage that E and I can easily be calculated in the load.

Sign Conventions. These signs are basically arbitrary. In fact, they are (in the case of current) slightly unreasonable because of ignorance of the nature of conduction when they were assigned.

Voltage must always be measured between two points. The plus terminal is the terminal with a deficiency of electrons.

Current is conventionally thought of as flowing from plus to minus voltage. This direction of flow results in a voltage drop through the impedance that connectes the terminals of the generator or battery. Note two confusing results of this sign convention: current flows from minus to plus inside a generator or battery, and electrons always move in the opposite direction to conventional current. In the application of Kirchhoff's laws, it is essential that the voltage sign convention be consistent.

1.01.02 Capacitance

A capacitance is formed whenever two conductors are separated with an insulator. A capacitance is capable of storing electricity as lump charge. As electrons are removed from one plate, electrons are attracted to the other plate. An electrical stress is set up in the dielectric between the plates. How much stress (measured in voltage) is set up, is determined by the size of the plates, the spacing between them, the material between them, and the number of electrons removed from one plate and put on the other.

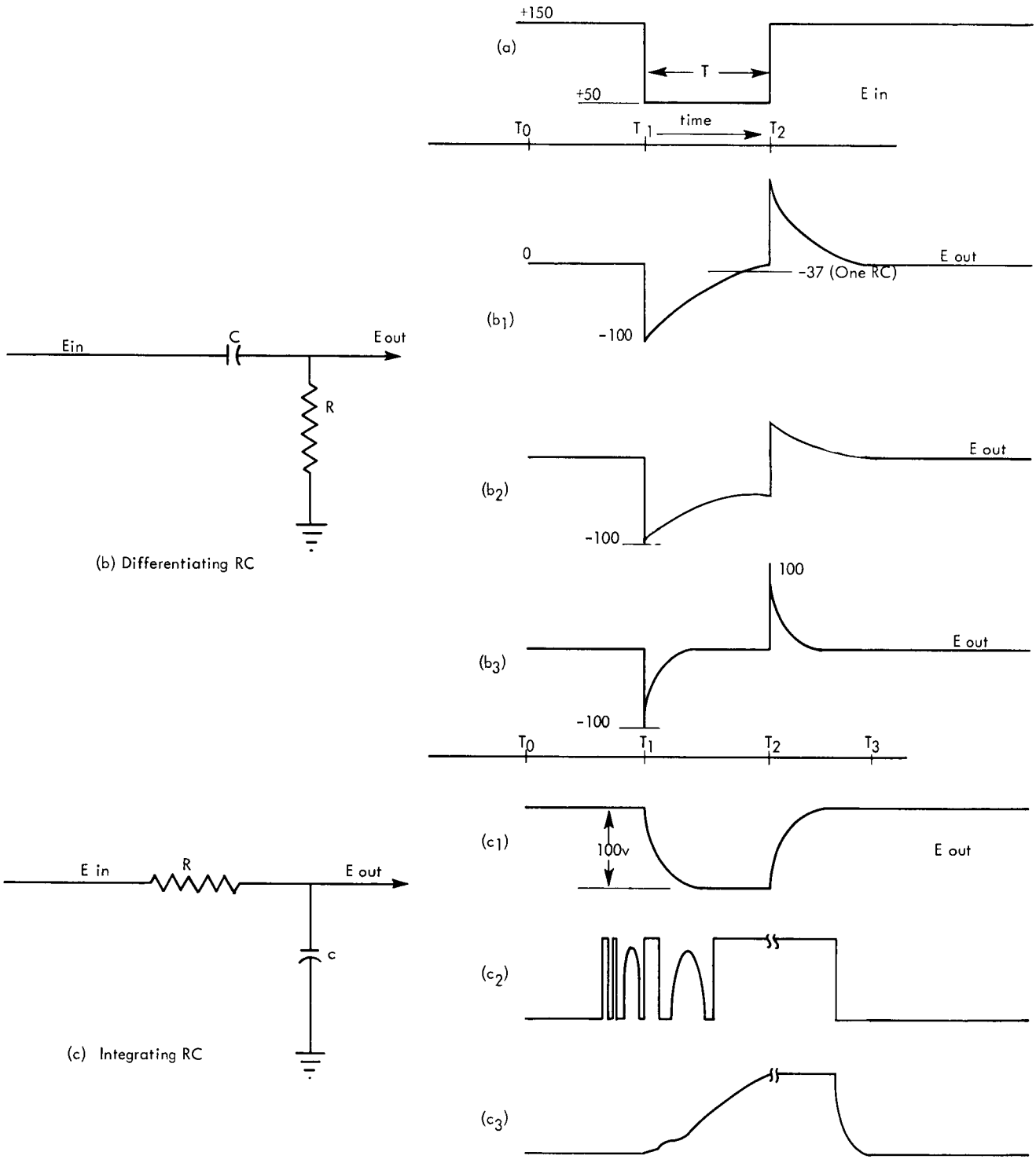


FIGURE E5. RC CIRCUITS, DIFFERENTIATING AND INTEGRATING

Capacitors are used in computer circuits:

1. To couple a sudden variation in voltage (signal) from one DC level to another.
2. To store energy. This includes by-passing, decoupling and filtering (practically synonymous) and use in resonant circuits.

Behavior of Capacitors

1. Maximum current flows at the time of minimum voltage across capacitor.
2. Voltage across the capacitor cannot be changed instantly.
3. Average (or DC) current through a capacitor is zero.

1.01.03 Time Constant

When a capacitor is placed in series with a resistance and a voltage change is applied to the combination, the initial voltage is all across the resistor and the final voltage is across the capacitor. The curve that represents the charge or discharge of the capacitor is a mathematical function and is shown in Figure E4. This curve is known as the Universal Time Constant Curve. Note that the curve is exponential and that for each unit of time, or each time constant, the voltage transition changes 63 percent of the distance remaining. Generally, the transition is said to be complete after four or five time constants. The unit of time (time constant) is defined as the time necessary for the voltage transition to be 63 percent complete. The time constant TC (in seconds) for any RC (or RL) combination is equal to the product of R (in ohms) and C in (farads). A more useful set of values, mathematically equal to the above formula, is TC (in microseconds) equals R (in megohms) times C (in micro-microfarads). The value of components being discussed usually dictates the preference of terms. For example:

R	= 5000 ohms, C = 470 uuf	R	= .005 megohm, C = 470 uuf
TC (sec)	= RC	TC (usec)	= RC
TC	= $5000 \times 470 \times 10^{-12}$	TC	= $.005 \times 470$
TC	= $2.35 \times 10^{6} \times 10^{-12}$	TC (usec)	= 2.35 microsecond
TC	= 2.35×10^{-6}		
TC	= 2.35 usec.		

Thus, both methods arrive at the same time constant of 2.35 usec. However, the microsecond-megohm-micro-microfarad formula eliminated the handling of exponents. In either case, the time constant of an RC combination is the same value. An example of the functions of RC circuits with different time constants is shown in Figure E5.

Figure E5b shows the circuit in question, an RC differentiating circuit. A circuit of this type is used to couple a sudden variation in voltage (signal) from one DC level to another. Assume E_{IN} to be +150 volts or +50 volts and it changes suddenly (Figure E5a). Starting at t_0, the following values can be measured:

E_{IN} = +150v
E_R = 0
I_R = 0
E_C = +150v
E_O = 0

Thus, the capacitor is charged to 150 volts and no current is flowing. At t_1 the input voltage suddenly changes to +50 volts. Because the voltage across a capacitor cannot change instantly, E_O instantly changes and the voltage across R = -100 volts. The initial discharge current of the capacitor is limited only by the size of R. Current continues to flow from the capacitor, discharging it to a final voltage of +50 volts with 0 current through the resistor.

The complete readjustment described above would occur if the time T were long enough. Suppose that at t_2, shortly after t_1, the input voltage shifts back to +150 volts. Instantly, E_O shifts +100 volts because the voltage across the capacitor cannot change instantly. C now has a voltage of less than 150 volts across it, but more than 50 volts. The exact amount is determined by how long the input voltage stayed at its lower value. If the input voltage is left at +150 volts for a long period of time, the voltage across C changes to 150 volts and the voltage across the resistor E_O drops exponentially to zero. Using the above statement, several rules follow.

The slope of the output pulse is determined by the rate of charge (or discharge) of the capacitance C through R. If T is less than one RC, the pulse at E_O looks reasonably like the input pulse (Figure E5b$_2$). Thus, in a coupling circuit, the values of R and C would be so chosen as to reasonably duplicate the input pulse.

Where only the voltage shift is needed (as in input circuits to triggers), T should be much greater than one RC. The resultant output for this type of circuit is shown in Figure E5b$_3$. Clamping circuits are used to bleed off the unwanted portion of the output shift.

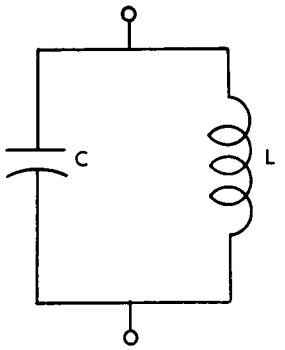
Another type of RC combination is the integrating circuit (Figure E5c). In this circuit, the output is taken across the capacitor. Charging and discharging of the capacitor still takes place through R. The circuit is used to remove sharp voltage variations (noise) from the input pulse. A change in voltage caused by a circuit breaker is desired but not the voltage fluctuations that are caused by contact bounce. Figure E5a shows the input and E5c shows the resultant output. The output voltage, taken across C, again cannot change instantly. The slope of the output pulse is again controlled by the values of R and C. The DC levels would be a function of the input and output circuits.

Figure E5c$_2$ shows a typical pulse from an emitter and illustrates the need for integrating networks. If this pulse were put directly onto the trigger grid, the tube would be turned on and off several times from the one circuit-breaker pulse. This is an undesirable condition. The key trigger (T_K) (Figure B27) makes use of three stages of integration in each input. The third stage consists of the 51K resistor and stray circuit capacities. Figure E5c$_3$ shows the pulse after integration.

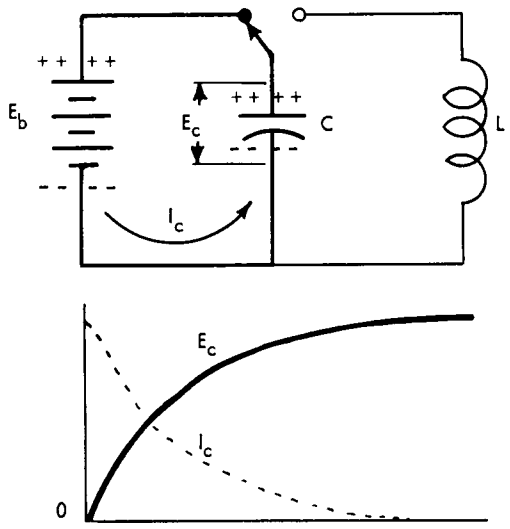
1.01.04 LC Tank Circuits

Primarily, capacitors C and inductors L are used individually throughout the system. However, a function of these two components is to serve together in a parallel resonant LC circuit. This type of circuit is known as a tank circuit because it can store high circulating currents. Tank circuits are used in the pulse-forming inverter, peakers and oscillators. Once excited or shocked, a tank circuit produces sinusoidal voltage, and current changes at a frequency dependent upon the values of L and C. In an LC circuit with zero resistance, these oscillations would theoretically continue forever. However, resistance is present in all circuits and the oscillations soon damp or die unless the circuit is repeatedly shocked (re-energized). The pulse-forming circuits use this principle of oscillation to produce an accurately timed pulse that is made up of one-half an oscillation cycle. The half-cycle that is not needed is usually damped by a diode.

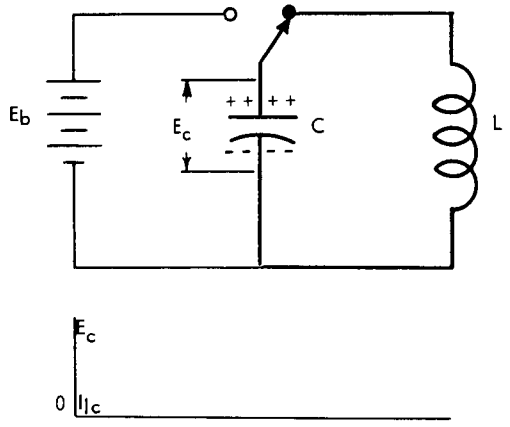
Remember that the voltage across a capacitor cannot change instantaneously. Charging a capacitor is a function of current and time; the capacitor can store a charge. The inductor resists any change in current through it. As current builds up through an inductor, the inductor resists the increase and flux lines build up around it. If the current through the inductor tends to decrease, the flux lines collapse, causing an induced voltage of such polarity as to maintain the original current flow. These properties of L and C are used in the tank circuit.



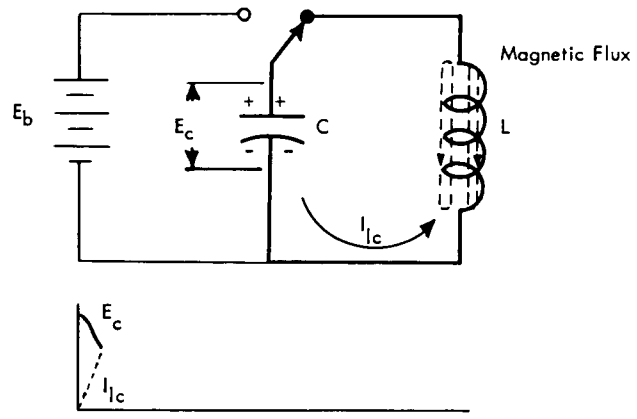
A tank circuit consists of a capacitor, C, and an inductance, L, connected as shown in the diagram. The name, tank, is derived from the storage action the circuit has on electrical energy.



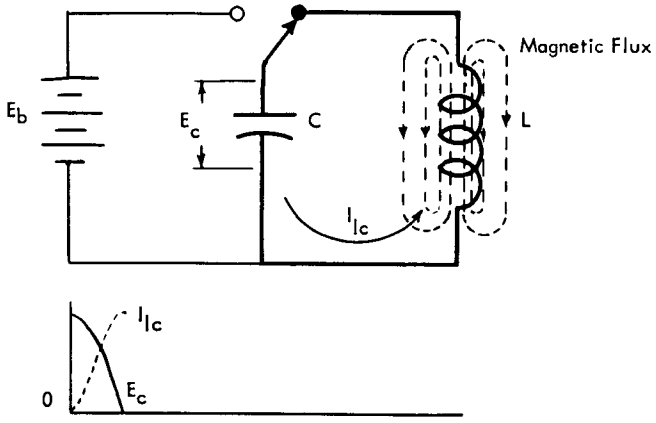
Before the operation of a tank circuit can be analyzed, the capacitor must be charged. This is accomplished in the circuit by operating the switch to make contact between the battery and the capacitor. As illustrated in the curves above, the instant the switch is closed maximum current flows. At this same instant, the voltage across the capacitor E_c is zero. Over a period of time, as the capacitor charges, the current diminishes to zero and the voltage E_c rises to the value of E_b, the battery voltage. To illustrate, a full charge is indicated by four plus signs on the top plate of the capacitor and four minus signs on the bottom plate.



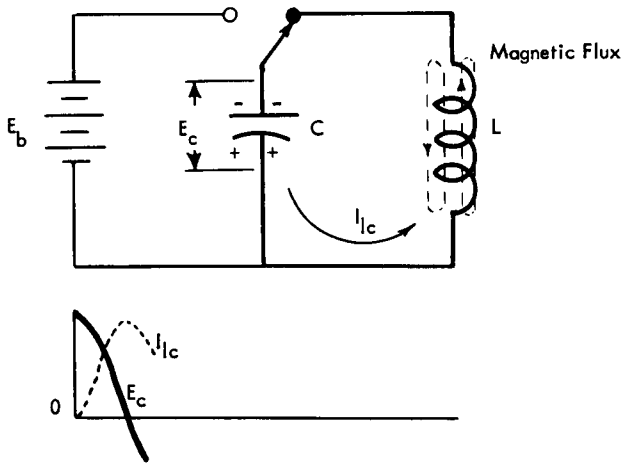
Now, with the capacitor fully charged, the switch is transferred as shown above. At the instant the switch is transferred, the coil offers maximum resistance to any current flow. Therefore, as shown on the curve, E_c is still at its maximum value and the current flow I_c is zero.



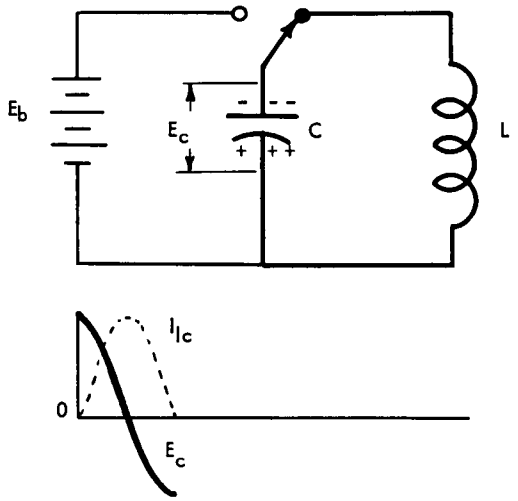
Immediately after the switch is transferred, a magnetic field starts building up around the coil. (See above.) At the same time, less resistance is offered by the coil and the current flow I_{1c} starts to increase. This, of course, puts a drain on the capacitor's charge and its voltage begins to drop. This is indicated in the circuit diagram by showing only two plus and two minus signs on the plates of the capacitor.



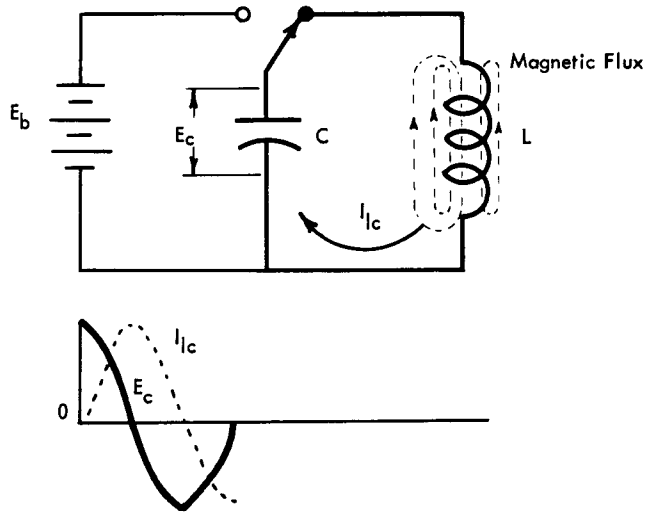
As the action continues, a condition is soon reached where three situations exist (see above): (1) the current flow I_{1c} is at its maximum value, (2) the magnetic field about the coil is at its maximum value, and (3) the charge on the capacitor is completely dissipated. See curves. For this condition, the capacitor can no longer support the current flow. At this time the magnetic field begins to collapse, and in so doing, attempts to sustain the current flow.



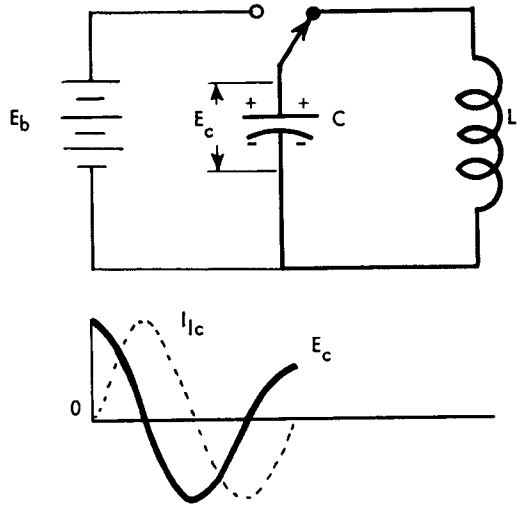
The sustained current flow causes the coil to appear as a generator charging the capacitor in an opposite direction from its initial charge. (See above.) As the capacitor charges, the current I_c is diminishing. This continues as the magnetic field dissipates.



Soon, a state is reached where the current I_c ceases to flow. At this time there is no magnetic field left around the coil; the capacitor is charged to a value somewhat less than its initial charge. The smaller charge is illustrated by three minus signs on the upper plate, and three plus signs on the lower plate of the capacitor. The curve above shows the relationship of the voltage E_c and the current I_{1c} at this time.

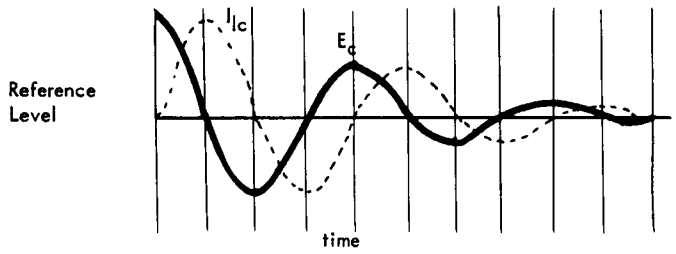


When the current ceases to flow, the opposite charge on the capacitor initiates a flow of current in the opposite direction. This, in turn, builds up another magnetic field about the coil which is opposite in polarity to the one originally discussed. The figure above illustrates the condition of maximum current flow, maximum magnetic field, and no charge left on the capacitor. Note that this current and magnetic field are both somewhat less than the previous values reached. This is borne out by the curves shown with the circuit diagram. The decay of values is caused by inherent resistance of the coil, capacitor leakage, and so on.



Illustrated above are the conditions which exist after the magnetic field and current once again play out. A charge (of the same polarity as it was initially) is now on the capacitor (with the amplitude reduced considerably).

This oscillatory action continues until the circuit losses use all the electrical energy initially stored in the capacitor.



Illustrated above is the complete transient curve resulting from the actions previously discussed. Note that although the values of current and voltage continually decrease, the elapsed time (t) between the points where E_c or I_{1c} cross the reference line remains fairly constant. This time factor is determined by the value of the capacitor and the inductance of the coil.

1.01.05 Point Contact Rectifier--the Crystal Diode

The materials used for most point-contact rectifiers are either silicon or germanium contacted by a sharply pointed tungsten wire. The whole device is enclosed in a ceramic or glass shell as shown in Figure E10a. These devices are more commonly known as crystal diodes or crystal detectors.

In the manufacture of germanium crystals, germanium dioxide is reduced by heating to an uncrystallized, gray, powdery form of the pure metal. This powder is then melted, along with the proper amount of impurity, to form the desired type of semiconductor. If an n-type is being made, the impurity is an element such as arsenic or phosphorus. When the semiconductor has cooled, it is sliced into wafers about two or three mm (millimeters) square and 0.5-mm thick. The wafers are then ground and polished on one side to form the active element. The unpolished side is then soldered to a large-area base electrode. The sharply pointed wire makes contact to the polished side.

The complete theory of operation for point-contact rectifiers is too complex to give here in its entirety. However, an approximate, and necessarily incomplete, explanation helps in understanding the characteristics of these devices. When two dissimilar metals are put in good electrical contact, a potential difference is found to exist between them. This potential difference is known as the contact potential difference. It is numerically equal to the difference between the work functions of the two metals when expressed in electron-volts. Work function is defined as the amount of energy necessary to force an electron from its normal orbit to a new energy level (conduction band). Electrons can pass from the material of low work function to that of the high work function more easily than in the reverse direction.

The high work-function material then becomes negatively charged, and electrons find it increasingly difficult to pass from the low to the high work-function material. The charge builds up until the net transfer of charge is zero, and at this point the high work-function material has a negative potential relative to the other material.

In the case of an n-type semiconductor contacted by a tungsten wire, the tungsten has the higher work function and becomes negative with respect to the crystal. However, unlike a metal, the semiconductor has a limited number of free electrons available for current conduction. Therefore, when the semiconductor reaches an equilibrium potential, there is a layer in the semiconductor around the point of contact from which all electrons have been removed. Other electrons from the semiconductor cannot enter this layer because of the repulsion by the negative charge accumulated on the tungsten point. This layer is known as the blocking layer and is about 10^{-4}mm thick. It is this blocking layer that causes the crystal rectifier to have a unilateral (one-way current) characteristic.

When voltage is applied between the contact wire and the semiconductor, the device can pass or it may block current, depending upon the polarity and magnitude of the applied voltage. If the semiconductor is made negative with respect to the contact wire, electrons flow from the tungsten to the external circuit and thus remove the negative charge from the contact metal (that repelled the free electrons in the semiconductor). This action wipes out the blocking layer, and a current can flow. The current is impeded only by the bulk resistance of the semi-conductor. If the semiconductor is made positive with respect to the tungsten contact wire, electrons flow from the external circuit to the tungsten and hence they increase the negative charge in this metal at the point of contact. This charge increases the thickness of the blocking layer. Because there are no free electrons in the blocking layer, there can be no current flow through it unless electrons in the metal have enough energy to overcome the restraining forces and pass from the metal to the semiconductor. The thickness of the blocking layer increases with potential difference and the voltage required to cause conduction in the reverse direction is quite high. Thus, point-contact rectifiers have relatively low resistance in one direction and an extremely high resistance in the reverse direction. When the germanium diode is used as a detector, the forward resistance is considerably lower than that of the usual vacuum tube. Its back resistance is not as great as that of the vacuum tube.

1.01.06 The Load Line

In analyzing tube circuits, it is often necessary to know what current is flowing through the tube. With a given set of values such as plate voltage, grid voltage and load resistance, a load line can be drawn on the family of plate characteristic curves for any tube. Figures E16, E17, E18, and E19 are the characteristic curves for the 6211, the 5965, the 5687, and the 2D21, respectively.

A straight line is used to represent the linear characteristics of a resistive load. The starting point, usually used to draw the load line, is the point where the load line intersects the X axis (applied voltage). Since the load line represents circuit conditions from no current to full current, the point on the X axis that represents the applied voltage is one point of the load line (no tube current). The current value on the Y axis is equal to the supply voltage divided by the load resistance. (By Ohm's

law, this is maximum current with the tube replaced by a short circuit.) This represents the second point. The load line for the given load is drawn between the two points.

If the full current point is beyond the limits of the graph (for example, 30 ma on Figure E16), another point must be chosen for use with the no-current point. A new voltage value of E' (less than the supply) is used to compute the current through the load. By going E' volts to the left of the supply voltage point on the X axis and by going up the number of current units just calculated, the second point can be located. For example, if the load for a given circuit were 3K, the full current point would be about 47 ma. This point, on the Y axis, is beyond the limits of the graph. Use a smaller voltage, 60 volts. This voltage gives a current value of 20 ma (I = E/R). At 80 volts on the X axis (E_P -60), go up to the 20 ma hoizontal line. This point and the no current point (E_P) can then be used to draw the load line.

An example of a load line is shown in Figure E16. A plate supply of +140 volts and a load of 6K is used. In most applications, a tube in full conduction has sufficient grid current flowing to set the grid voltage at zero volts or slightly positive. Thus, in the example, the load line intersects the full conduction operating point and gives a value of plate current of 11.7 ma; a tube drop of 71 volts and the voltage drop across the load are the balance of the supply, or 69 volts. The load line method of calculation is only an approximation; it is not mathematically exact.

The load line gives (at the operating point) the tube current, the voltage drop across the tube, and the voltage drop across the load. With the proper load line drawn, the change in tube current (and tube-load voltage drops) can readily be seen without the use of mathematics. The load line can be used, also, to determine the above values for any value of negative bias.

Cathode Follower Load Line. The load line for a cathode follower is drawn in the same manner as above. However, the operating point cannot be found at the same zero-bias intersect. In section 2.09.00, Book A, it was shown that a cathode follower will stabilize at a slight negative bias for any normal input voltage. Because of this cathode bias, a trial and error method can be used to establish the operating point of the circuit.

In Figure E17, a load line is shown for a standard cathode follower (5965 tube) with a load resistor of 6K. For example, use an input of -30 volts to the cathode follower. Because a cathode follower does not amplify a signal, an output level of -30 volts (zero bias) can be assumed for the first trial. It was shown in section 2.09.00 that a positive bias cannot exist. At the E_C = 0 intercept, a current value of 16 ma is read on the plate current axis. A current of 16 ma through 6K gives a voltage drop of 96 volts or a cathode level of +36 volts. The cathode level (output) does not agree with the original assumption of -30 volts.

Assume an output of -28 volts (-2 volts bias). The current value at this intercept is about 7.7 ma. This current gives a voltage drop of 46.2 volts (cathode level of -13.8 volts); again this value does not agree with the assumed output of -30 volts. However, the calculated output level is approaching the assumed value. With this fact in mind, assume for the third trial an output of -27 volts (-3 volts bias). This intercept indicates a current of about 4.8 ma and would result in a cathode level of about 31.2 volts. Notice that on this trial the effective bias has swung positive and

the output level just calculated is nearly the assumed level. Thus, the proper operating point lies somewhere between -2 and -3 volts bias. It is safe to assume that the effective bias at the stable operating point is about -2.5 volts (-27.5 volts output) with a tube current of about 5.4 ma. Although -30 volts was used as an input, any normal value of input voltage can be used and the method still holds.

The above method is only as accurate as the interpolation of the graph. However, the information gained, although not 100 percent accurate, is valid and no lengthy mathematics was needed. The accuracy involved is more than sufficient for most applications both in basic design and general information about any particular circuit.

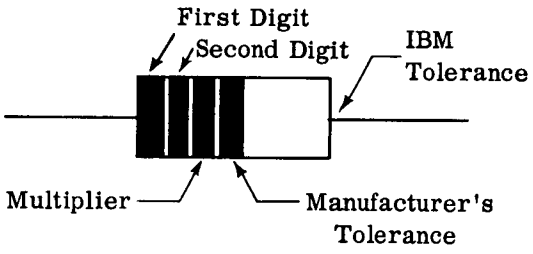
1.02.00 PLUGGABLE UNIT COMPONENT ASSEMBLY DATA

1.02.01 Resistors

Resistors having matched group usage as described below are bridged into 2-1/2 percent tolerance groups and are color coded as shown in Figure E6. The color marking is on the end opposite the standard RMA color code marking.

In certain applications, it is necessary that the ratio of one resistor to another be held to close limits, although the absolute value of resistance is not critical. This occurs notably in signal-voltage divider circuits. Such applications are identified on the wiring diagrams by the fact that the resistors are always connected in series, and each resistor in such a group has a letter (A, B, C, and so on) adjacent to its value, the same letter being used for all resistors in the group. One or more of the resistors in such a group may be paralleled by a capacitor, and the junctions between resistors may be connected to other points in the circuit. In all applications of this type, the resistors in any one group must be selected from the same 2-1/2 percent tolerance bracket. In some cases, the same identifying letter has been applied to two or more such matched groups on one wiring diagram. This does not imply that the resistors in all groups identified by the same letter must come from the same tolerance bracket.

All resistors not designated by an alphabetic notation are ± five percent unless otherwise specified. All 150-ohm parasitic suppressor resistors are ± 20 percent. (The 150-ohm parasitic suppressor resistors dampen oscillation.)



No Color ± 20%
Silver ± 10%
Gold ± 5%

Color	First and Second Digit	Decimal Multiplier	IBM Tolerance
Black	0	10^0	
Brown	1	10^1	
Red	2	10^2	- 5% to - 2 1/2%
Orange	3	10^3	- 2 1/2% to 0
Yellow	4	10^4	0 to + 2 1/2%
Green	5	10^5	+ 2 1/2% to + 5%
Blue	6	10^6	-20% to +20%
Violet	7	10^7	
Gray	8		
White	9		- 5% to + 5%

Note: Resistance is expressed in ohms.

FIGURE E6. RESISTOR COLOR CODE

1.02.02 Capacitors

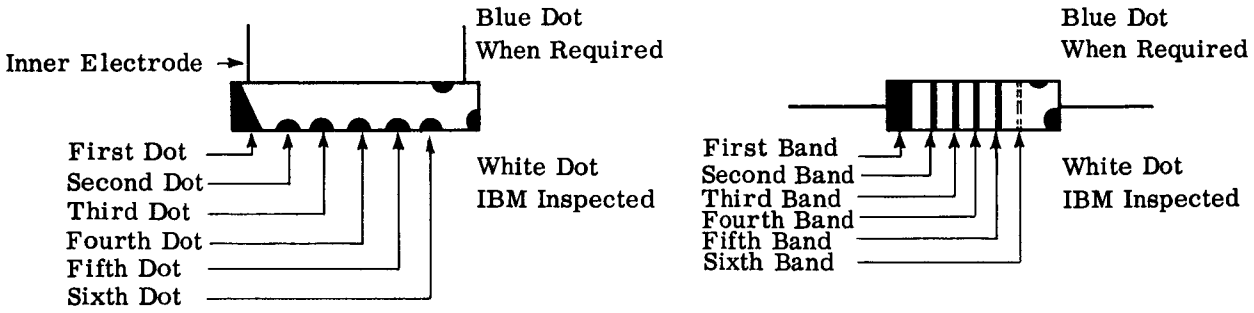
The notation for values of capacitance is: uuf for micro-microfarads, and ufd for microfarads.

A capacitor is represented in drawings as a straight plate and a curved plate, the latter denoting the outside foil or the negative terminal, when either of these is important.

Capacitors that are large enough physically to have the capacitance value printed. on the jacket have it there. Some special capacitors are identified by part number and values printed on the body. For the smaller mica and ceramic capacitors, color coding in the form of dots or bands is used; it expresses capacitance in micro-microfarads.

A white dot, appearing apart from any other marking or color coding, signifies that an additional IBM inspection has been made. This was done on a spot check basis and has now been discontinued.

Radial and Axial Ceramic Capacitors



The six place coding system (Figure E7) is used to further identify capacitors as to their characteristic, if the five place system is inadequate.

"Characteristic" refers to the temperature-capacitance relationship and its associated temperature range. It is expressed in parts per million of capacitance change for each degree centigrade of temperature change. Units U2M, S2L, S3N, S3P, Y5Y, and Z5Z have broad limits of PPM change for temperature variation.

The blue dot signifies restricted range capacitors. "Characteristic restricted-range" capacitors do not vary in capacitance more than plus or minus 6 percent from the actual value measured at 25°C, as the ambient temperature is varied from +15° C to +55° C.

Examples:

Dot -	1st	2nd	3rd	4th	5th	6th
Y5Y - 2200 uuf ± 20%	silver	red	red	red	black	
-750 PPM/°C - 100 uuf ±5%	violet	brown	black	brown	green	
S3N - 68-uuf ±10%	gray	black	blue	gray	black	white

Five Place System	First Position			Second and Third Positions	Fourth Position	Fifth Position	
Six-Place System (Note 1)		First Position	Second Pos.	Third and Fourth Positions	Fifth Position	Sixth Position	
Color	Characteristic (Note 3)	Characteristic (Note 3)		Nominal Capacitance uuf		Tolerance	
				First and Second Significant Figures	Multiplier (Note 2)	Nominally 10 uuf or less	Nominally more than 10 uuf
Black	0	0.0	-1 (S3N*)	0	1	±2.0 uuf	±20%
Brown	-33	--	-10	1	10	±0.1 uuf	± 1%
Red	-75	1.0	-100 (S3P*)	2	100	--	± 2%
Orange	-150	1.5	-1000	3	1000	--	±2-1/2%
Yellow	-220	2.2	-10000	4	10,000	--	--
Green	-330	3.3	+1	5	100,000	±0.5 uuf	± 5%
Blue	-470	4.7	+10	6	-----	--	+100% -0%
Violet	-750	7.5	+100	7	-----	--	+80% -20%
Gray	U2M	S3N*	+1000	8	.01	±2.5 uuf	--
White	S2L	S3P*	+10000	9	.1	±1.0 uuf	±10%
Silver	Y5Y	--	--	--	--	--	--
Gold	Z5Z	--	--	--	--	--	--

NOTE: Capacitance is expressed in micro-microfarads.

Note 1: Six place system may be used for identifying characteristic S3N or S3P units.

Note 2: Use lowest possible numerical multiplier.

* : Both positions must be so colored for S3N or S3P units.

Note 3: Temperature coefficient of capacity (parts per million of change per degree centrigrade change)

$$\text{Temp. Coeff.} = \frac{C_T - C}{C\,(T-25)} \times 10^6$$

C_T = Capacitance measured at test temperature

C = Capacitance at 25°C

T = Test temperature in degrees centigrade

FIGURE E7. RETMA CERAMIC CAPACITOR COLOR CODE

Example of Computing Temperature Effect on Capacitance

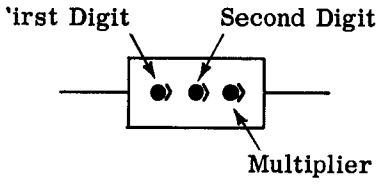
$$T.C. = \frac{C_T - C}{C\,(T-25)} \times 10^6$$

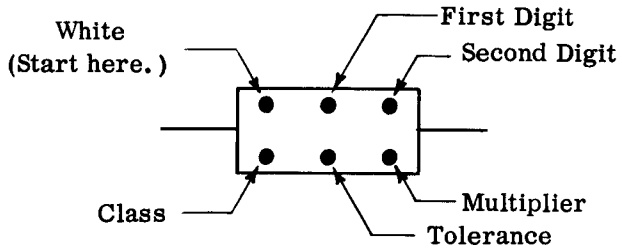
$$C_T = \frac{(T.C.)\,C\,(T-25)}{10^6} + C$$

$$C_T = \frac{(-750)\,100\,(26-25)}{10^6} + 100 = \frac{-75000}{10^6} + 100 = 99.925 \text{ uuf}$$

T (Test Temperature) = 26^oC
C (Capacitance at 25^oC) = 100 uuf
T.C. (temperature coefficient) = -750
C_T = capacitance at test temperature

Three-Dot and Six-Dot Mica Capacitors





"Class" refers to temperature coefficient, Q, insulation resistance and capacitance drift. (See Figure E8.)

Color	Digit	Decimal Multiplier	Tolerance	Class
Black	0	10^0	±20%	A
Brown	1	10^1		B
Red	2	10^2	± 2%	C
Orange	3	10^3	± 3%	D
Yellow	4	10^4		E
Green	5		± 5%	
Blue	6			
Violet	7			
Gray	8			I
White	9			J
Gold				
Silver			±10%	

Note: Capacitance is expressed in micro-microfarads.

FIGURE E8. RETMA MICA CAPACITOR COLOR CODE

Examples:

Three Dot
15uuf — Left to Right: Brown, Green and Black

Six Dot
Class B-1000 uuf ±10% — Clockwise: White, Brown, Black, Red, Silver and Brown

Class E-680 uuf ±20% — Clockwise: White, Blue, Gray, Brown, Black and Yellow

1.02.03 Inductors and Reductors

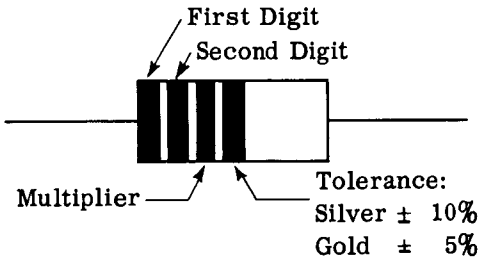
The notation for inductance is: uh for microhenrys and MH for millihenrys.

Inductors are encased in a jacket of non-combustible material. This package materially improves dielectric strength, resistance to change (in value) from humidity and temperature variations and better lead strength. The value of inductance (in microhenrys) and the tolerance are to be color coded with RETMA significance. The size of the casing will vary with the smallest being slightly larger than a two-watt resistor.

The old style of inductor comes in different shapes and sizes. Physically, most inductors are bobbins of wire mounted serially on an insulated core. Because of discrepancies in marking and color coding, identification should be made by part number.

Reductors. Also forthcoming, in the same casing as the inductor, is a component called a reductor. In a reductor, the inductive winding is wound on an insulated carbon-composition resistor with the leads of the winding and resistor tied together. It is a parallel LR circuit and can be used in pulse forming networks. Reductors are not color coded. All information pertaining to the inductor and resistor components is printed on the reductor jacket.

Inductor Color Coding



Former Inductor Color Coding

White Dot	50 uh
Gray Dot	100 uh
Yellow Dot	250 uh
Violet Dot	500 uh
Black Dot	750 uh
Orange Dot	2 mh

1.02.04 Varistors

A varistor is a component whose resistance varies with the applied voltage. It is made of a silicon-carbide ceramic material that has nonlinear resistance characteristcs (the current varies as a power of the applied voltage). The material consists of resistive particles separated by thin insulating films of silicon dioxide which break down and conduct as the voltage is raised. (The insulating film reforms as soon as the applied voltage is removed.) The varistor shows high resistance to normal relay voltages. It shunts the relay coil for the currents induced by the high inductive voltage generated when the relay is deenergized and the electromagnetic field of the coil collapses.

1.02.05 Germanium Crystal Diodes

Because of the discontinuance of diode-classification color coding, diodes are to be identified by the vendor's marking. The table below is a list of common diodes used with the vendor, designation number, color strips and polarity identification.

Class	Vendor	Designation	Color Code or Designation Mark	Polarity Identification
F	Hughes	1N191	Brown, White, Brown	See note*
	Amperex	1N480	----------	White band on K end
	Sylvania	1N119	Stamped on diode	Diode symbol
G	Hughes	1N192	Brown, White, Red	See note*
	Sylvania	1N120	Stamped on diode	Symbol
		1N490		
J	Transitron	S152G	Brown, Green, Red	See note*
M	Transitron	S335	Orange, Orange, Green	See note*
P	General Elec.	1N92	Stamped on diode	Diode Symbol
R	Transitron	T13G	Black, Brown, Orange	See note*

Note*: Color code starts on the K end.

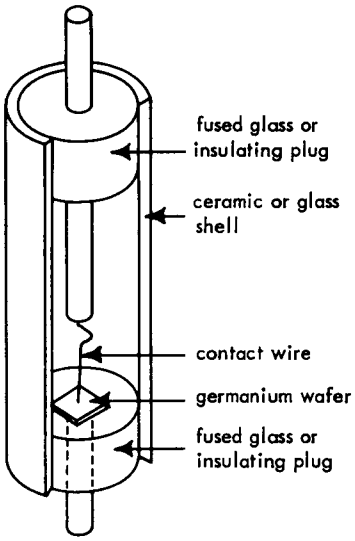
F(S) and G(S) are Hughes F and G diodes where the application calls for the size restriction. (The Hughes diode is the smallest physical size in the group.)

Figure E9a shows the general physical construction of a germanium diode. Figure E9b is a typical diode characteristic curve. The curve shows how the resistance of a diode varies with the polarity and amount of voltage impressed across it. Note how the back resistance breaks down when too large a back voltage is impressed across it. The -70v point implies that it is the maximum inverse voltage allowed in any application.

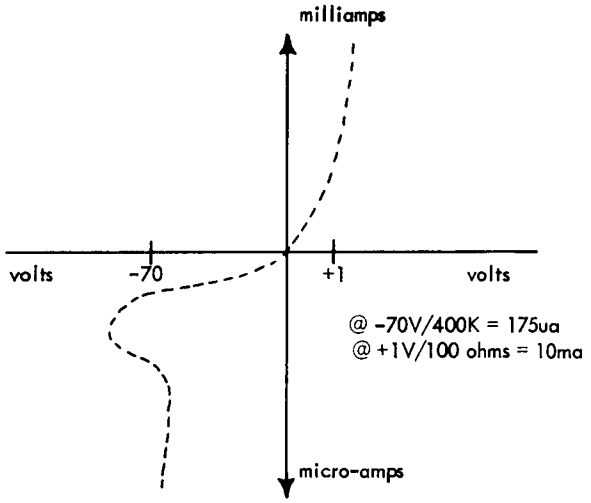
The three general types of diode construction are shown in Figure E9c. The point-contact type consists of a tungsten wire that is held under spring tension to the germanium wafer. A slight surge of current is run through the diode to weld the wire slightly to the germanium.

The micro-junction type can be an indium-coated wire. Again, a surge of current causes some of the indium on the wire to flow down and fuse to the germanium. A spot or small area of contact is thus produced. The micro-junction is a high conductance type of diode.

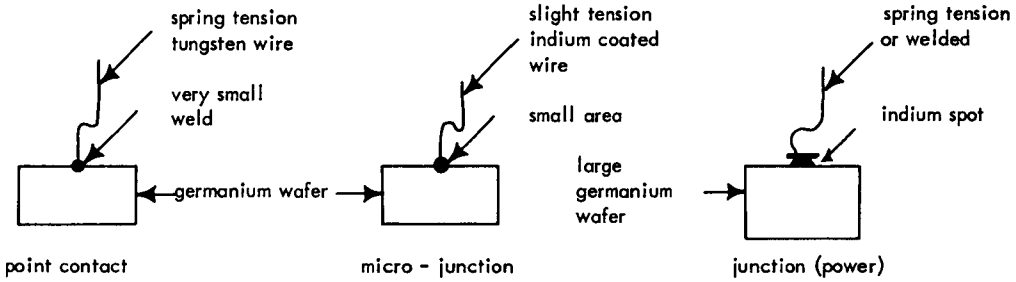
The junction type has a large spot of indium fused to the (larger) germanium wafer. A heavier wire with a large contacting surface is then brought into contact with the indium spot. The wire is either under tension or fused. The junction type is a power diode that can pass large currents and dissipate heat.



a. Physical Layout



b. Typical Diode Characteristic Curve



c. Types of Diodes

Forward Resistance	100 - 400 ohms	4 - 40 ohms	2 - 5 ohms
Back Resistance	400K min (F) 200K min (G)	600K -- up	100K (min)
Average Conduction	20 ma	60 ma	300 ma
Recovery Time	4.0 usec	1 - 2 usec	greater than 10 usec
Classifications	F,G	J,R,M	P

d. General Class Characteristics

FIGURE E9. THE GERMANIUM DIODE

Figure E9d lists some of the characteristics of diodes by class. Recovery time is usually the time necessary for the diode to stop conducting after it has been passing current in the forward direction. The recovery time is listed here for a comparison basis between diode types. Systems diagrams and pluggable unit wiring diagrams denote the class of diode that should be placed in any one circuit. General specifications guide the customer engineer as to why different diodes are selected for any particular application.

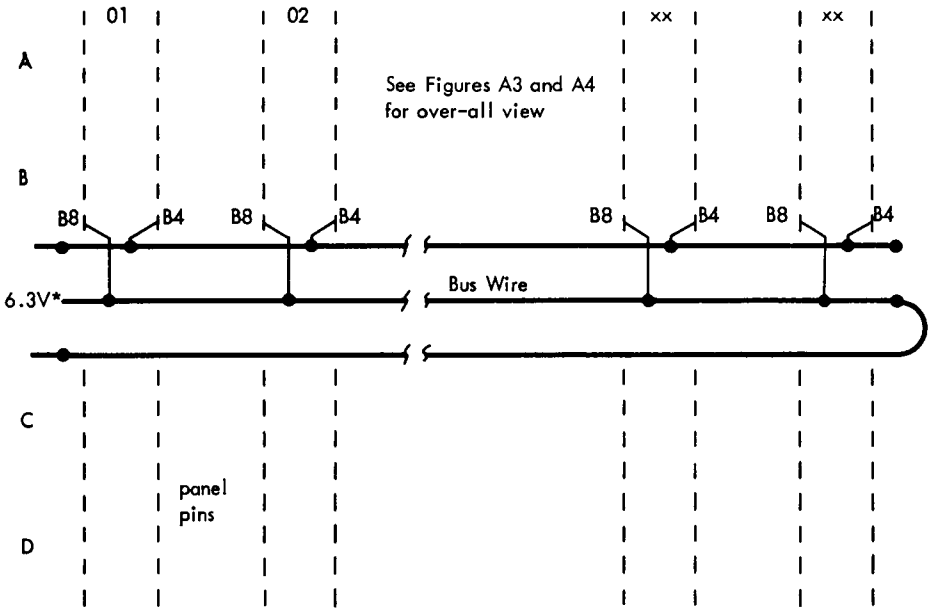
1.02.06 Service Wiring

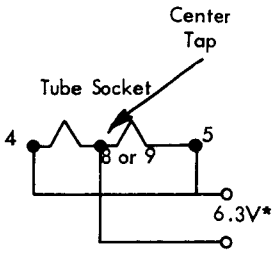
Service wiring is designated by a code number which indicates its voltage potential and color. The code numbers are written on the island pins through which the service wires pass (on pluggable unit wiring diagram). All service wires are #22, tinned copper wire with plastic insulation (under-writer approved to withstand 600 volts DC) and with hi-tensile rayon, lacquered cover. No bare jumpers may be used in service wiring.

704			705		
Code	Voltage	Color	Code	Voltage	Color
1	+220	Brown	12	+270	White/Black Tracer
2	+150	Red	1	+140(special)	Red/White & White Tracer
	+150(relay)	White/Red Tracer			
9	+15	White	2	+140	Red
3	+10	Orange		+140(relay)	Red/Green Tracer
0	Ground	Black		+72	White/Red Tracer (717, 722)
	-15	Not Color-Coded			
6	-30	Blue		+48(relay)	Brown (727)
5	-100	Green		+40(relay)	Several Colors Used
	-100(reset)	White/Green Tracer	0	Ground	Black
			11	-12(clamp)	White/Blue Tracer
8	-130	Slate	13	-12(reset)	White/Blue & Black Tracer
	-150(memory)	White/Blue & Black Tracer			
	-160 "		6	-60	Blue
	-200 "		5	-130	Green
7	-250	Violet		-140(memory)	Green/White Tracer
11	-250(reset)	White/Blue Tracer	10	-150	
	Neon	White/Red Tracer		-180(memory)	Orange
			7	-270	Violet
				Neon	White/Green & Black Tracer
			4	Signal	Yellow
				(Low Capacity)	Yellow/Black Tracer
			X, Y, Z	Filament	White/Yellow Tracer
			X', Y', Z'	6350 Filament	White

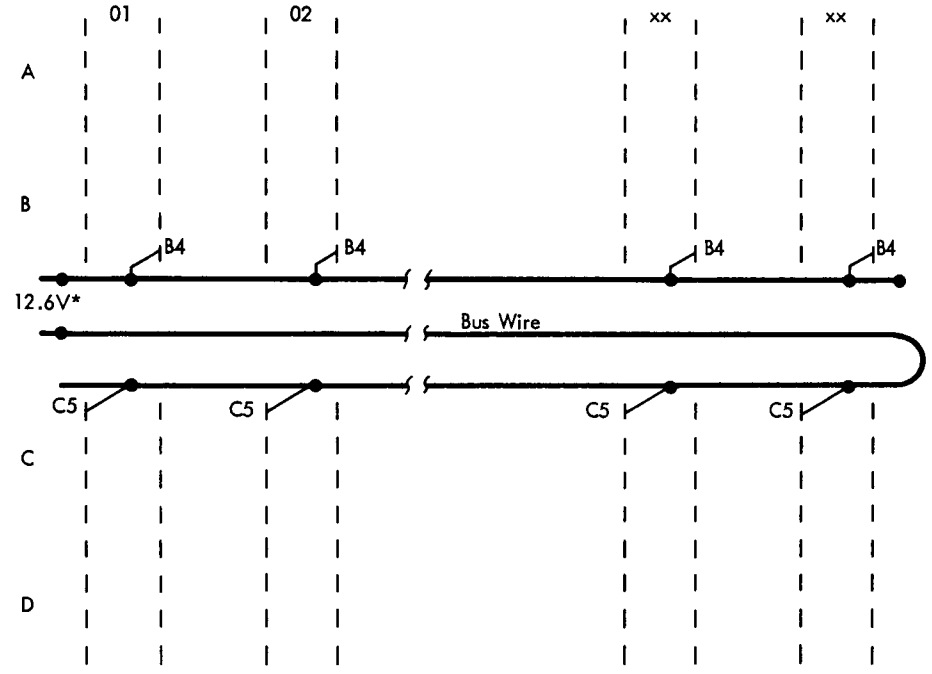
1.02.07 Signal Wiring

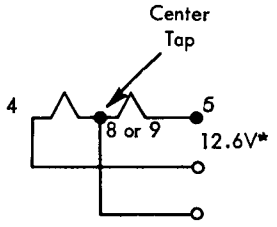
Signal wiring (color coded yellow or yellow/black) has the same specifications as service wire with the exception that bare, solid #20, tinned copper wire may be used between island pins directly above one another. However, bare signal wire may not be used between top island and tube sockets or between the bottom island and the





a. Filament and bus connections - 6.3 volts*





(For 12-volt center tapped tube filaments, center tap is returned to transformer center tap.)

* 6.3 or 12.6 volts AC at either zero, -60, -130 or -180 volts DC. This procedure minimizes filament to cathode potential. See filament transformer wiring diagrams (systems) for correct DC level.

b. Filament and bus connections - 12.6 volts*

FIGURE E10. TUBE FILAMENT WIRING

base. Bare signal wire may not be run through holes in islands or between island pins on opposite sides of the unit.

1.02.08 Filament Wiring

Filament wiring shall be solid, #20, tinned copper wire with plastic insulation approved to withstand 600 volts DC. Filament wires are designated X, Y, and Z, and color coded white with a yellow tracer. The X, Y, and Z are the legs of a 12v AC transformer with Y as the center tap for 6 volts. The center tap of the 12v tubes is returned to the transformer center tap on machines now in production. One half of the tube will still function if the other half of the filament opens. The unbalanced condition will cause current to flow through the center tap. This current flow is being used to detect and locate open filaments as a service aid.

Figure E10 shows the methode of wiring the 6.3v and 12.6v filament supply to the pluggable units. Note the different panel pins used for the entry to the individual pluggable units. This procedure insures that a 6.3v unit is inoperative in a 12.6v socket.

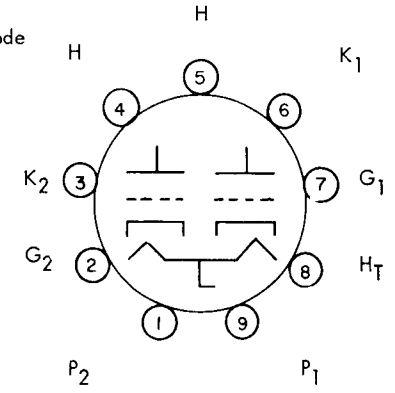
1.02.09 Copy of Assembly Specifications

1. Pluggable units shall be wired exactly as shown on wiring diagrams.
2. No wiring passes between island pin jumpers and island phenolic.
3. Wiring is to be kept as short as practical.
4. Service wiring which runs horizontally in the space between two islands shall lie just under the upper island.
5. Signal wiring which runs horizontally in the space between two islands is on top of the lower island.
6. Jumper wiring between tube socket pins shall lie as close to the tube socket plate as possible.
7. Wires shall extend through the island pins a minimum of 1/16" before being soldered. They shall not be wrapped around the island pins.
8. All jumpers passing through island pins must be soldered to those pins.
9. Tube socket pins shall be flared out so that there is a minimum of 1/8" clearance between adjacent pin tips.
10. One-sixteenth inch shall be considered the minimum clearance between uninsulated components or wires.
11. Wiring and/or components shall not project beyond the outside boundaries of the frame of the pluggable unit.
12. Where insulated wires are soldered to terminals, the insulation shall be stripped so that after soldering there is a minimum of 1/16" and a maximum of 1/8" clearance between the wire insulation and the terminal.

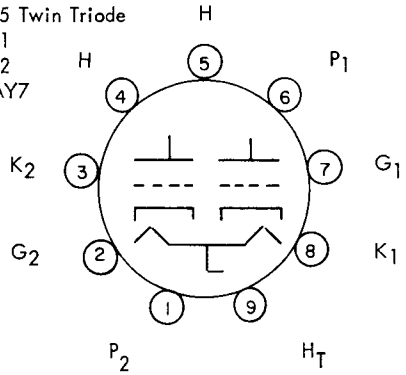
1.02.10 Copy of Soldering Specifications

1. The joints must be held electrically conductive and not moved until the solder has hardened.
2. The soldering iron should not be removed until the solder flows freely and evenly around the joint. The solder shall be applied directly to the joint, not to the iron, to avoid decomposing the flux.
3. Avoid using excessive amounts of solder.

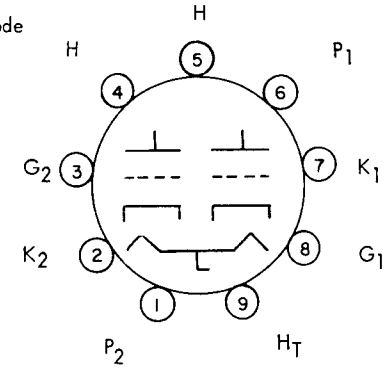
5687 Twin Triode



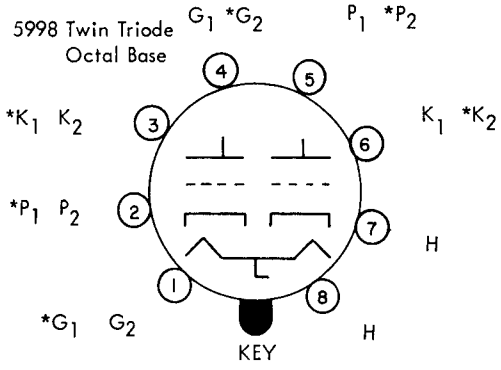
5965 Twin Triode
6211
6072
12AY7



6350 Twin Triode
6463

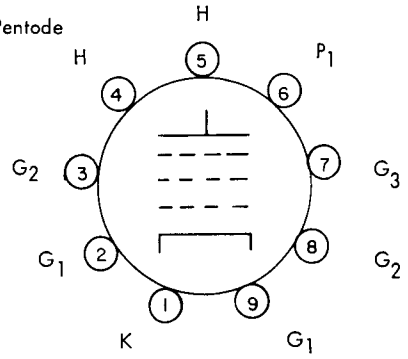


5998 Twin Triode
Octal Base

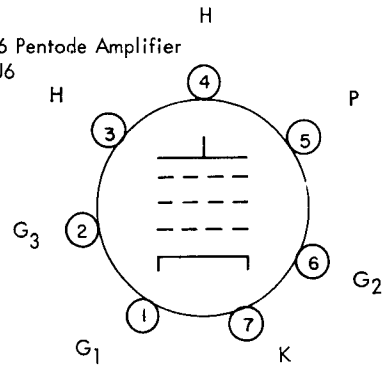


*6325

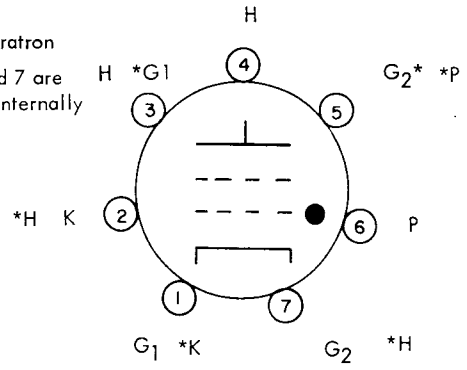
6197 Power Pentode
6CL6



6136 Pentode Amplifier
6AU6



2D21 Thyratron
Pins 5 and 7 are common internally



*6012
Pin 8 - G2

1680 Pentode Switch

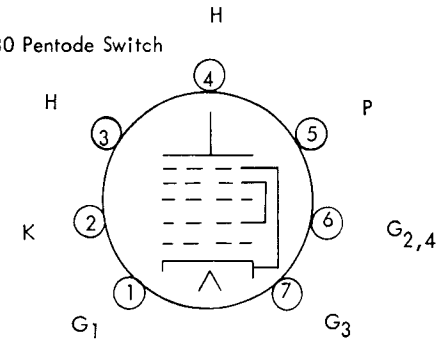


FIGURE E11. BASE PINS OF COMMON TUBE TYPES USED IN 700 SERIES

4. Care should be taken not to overheat the circuit components. This is particularly applicable when soldering the diode terminal leads to the island pins. The approved heat shunting tools shall be used to prevent damage to the diode.

1.02.11 Tube Socket Pin Connections

Figure E11 shows the pin connections for some of the tubes used in the machine. Several tubes have the same pin layout and are listed with the proper schematic. All 12v tubes have center tapped filaments.

1.02.12 Electron Tube Design Data (All data refer to values per section.)

	Tube Type				
Specification	6211	5965	5687	5998	6528
Maximum Plate Dissipation (Watts) (Design Value)	1.5	1.67	2.5	13	30
Heater Voltage (Volts)	6.3	6.3	6.3	6.3	6.3
Heater Current	300ma	450ma	900ma	2.5amps	5.0amps
Interelectrode Capacity: C_{gp} (uuf)	2.2	3.1	4.0	14	24
C_{gp} (uuf)	0.5	0.38	0.6	—	—
C_{gp} (uuf)	2.9	3.8	4.0	—	—
Maximum Plate Voltage	200	200	330	250	400
Maximum Average Grid Current (ma)	3.0	—	6.0	—	—
Maximum I_c for E_c = Iv (ua)	—	—	2 (E_b=100)	—	—
Maximum Cathode Current (ma)	14	17.5	—	125	300
Maximum Heater Cathode Voltage	±90	±90	±100	±90	±300
Amplification Factor (u)	27	46	18.5	—	—
Plate Resistance (ohms)	7500	8000	1680	—	—
Transconductance (umhos)	3600	5800	11000	—	—
Dynamic Grid-Cathode Resistance (ohms, approx.)	500	600	400	—	—
Cut-Off Bias with E_b = 140v	-8.5 (i_b=100ua)	-6.5 (i_b=150ua)	-13 (i_b = 200ua)	—	—

1.03.00 DIODE CIRCUIT DESIGN PROCEDURES

This material is included here for those who feel the need for a full understanding of how diode circuits are designed. The material included in this section was used in the design of the AND/OR circuits described in sections 2.01.00, 2.02.00, 2.03.00, and 2.04.00, Book A.

1.03.01 General Procedure

Diode circuits should generally be limited to two stages between cathode followers. The design should start at the final level setter (inverter, grounded grid amplifier or DC trigger input) or final cathode follower driven by the diode circuits, and proceed back toward the initial level setter. For convenience and standardization of design, nominal signal levels of + 10 volts and -30 volts are assumed.

1.03.02 Diode Back-Resistance

This discussion includes the effects of diode back-resistance, where a low back-resistance would hinder the operation of the circuit and considers the back-resistance infinite where low back-resistance would aid the operation of the circuit. Therefore, when computing rise times, all back-resistances returned to +10 volts are ignored. When computing fall times, back-resistances returned to -30 volts are ignored.

Back resistance values to be used for design purposes are as follows:

Class F diode	200K
Class G Diode	100K

1.03.03 Circuit Capacities

Some circuit and wiring capacities are listed below as a guide to estimating capacities for rise and fall time calculations. The figures listed for wiring capacity are given with the assumption that reasonable care has been taken in laying out the diode circuit to minimize capacity. A cathode follower or other tube circuits must always be inserted between a diode circuit output and the output of a pluggable unit.

Cathode-follower input capacity (5965, 6211, 5687)	6 uuf
Inverter input capacity	40 uuf
Diode capacity	1 uuf
Approximate pluggable-unit wiring capacity	3 to 5 uuf

1.03.04 Two-Stage Circuits

A simple rule of thumb can be used to get a first approximation of the first-stage load resistors. For a +AND circuit driving a +OR circuit, do the following:

Compute the OR circuit resistor with the OR circuit fall time formula (section 2.02.00, Book A). Then choose a value for R (AND) to set the DC voltage at the junction between the AND circuit and the OR circuit to +20 volts. Compute the

equivalent resistance effective during the rise and compute the rise time. Comparison between the rise time thus computed and that required in the circuit shows whether the AND circuit resistor should be increased or reduced. The largest possible resistor should be used.

Similarly, for an OR circuit driving an AND circuit, R (OR) can be chosen to set the voltage at the junction of the two circuits to -40 volts. Checking the fall time (using this resistor) shows in which direction R (OR) must be changed.

1.03.05 Diode Cascading to Reduce Back-Resistance Effects

The back-resistances of the diodes in a diode AND or OR circuit act as a load on the driving circuit. The driving circuit may be another diode circuit or a cathode follower as listed below.

	Driving Circuit	Diode Circuit in Question
Case 1	+AND	n way +OR
Case 2	Cathode Follower	n way +AND
Case 3	+OR	n way +AND
Case 4	Cathode Follower	n way +OR

In case 1 above, the AND circuit resistor must be small enough to hold up the OR circuit resistor returned to -130 volts and the back resistance of (n-1) diodes returned to -30 volts. For a given set of speed and signal level requirements, and increase in the number of diodes in the OR circuit requires that the AND circuit resistor be decreased to maintain the speed of rise. This, in turn, requires that the cathode resistor in the cathode follower driving the AND circuit be reduced to maintain the down signal level. This eventually requires that an additional half-tube be paralleled with the original cathode follower to handle the smaller cathode resistor.

In case 2, the cathode follower must be able to hold down the AND circuit resistor returned to +140 volts and the back resistance of (n-1) diodes returned to +10 volts. An increase in the number of diodes in the AND circuit produces a loss in signal down level unless the cathode resistor is reduced, in which case an additional half-tube may be required in parallel with the original cathode follower. In both cases, the effect of back resistance is seen as an increase in up-pulling or positively returned load on the driving cathode follower, when the cathode follower input is down.

In a similar manner, the effect of diode back resistance in cases 3 and 4 is seen as an increase in negatively-returned load on the driving cathode follower when the cathode follower input is up. In many circuits, this increase in load can be compensated for simply by increasing the size of the cathode resistor with only a small attendant loss in signal down-level. However, if the cathode follower is driving both AND circuits and OR circuits, the effect may be equally as serious as in cases 1 and 2.

The effect of back resistance can be reduced substantially by cascading diodes. It is obvious when a circuit is being designed where cascading will save tubes and where cascading would simply represent a waste of diodes. An example of the effect of cascading on back-resistance and circuit capacity is shown below. The notations apply to the six-way +AND circuit in Figure A8 and section 2.04.00, Book A.

$R = 0.428\ R_B$

$C_R = 1.83\ C_D$ (R_B and C_D are the values of one diode.)

$C_F = 2.33\ C_D$

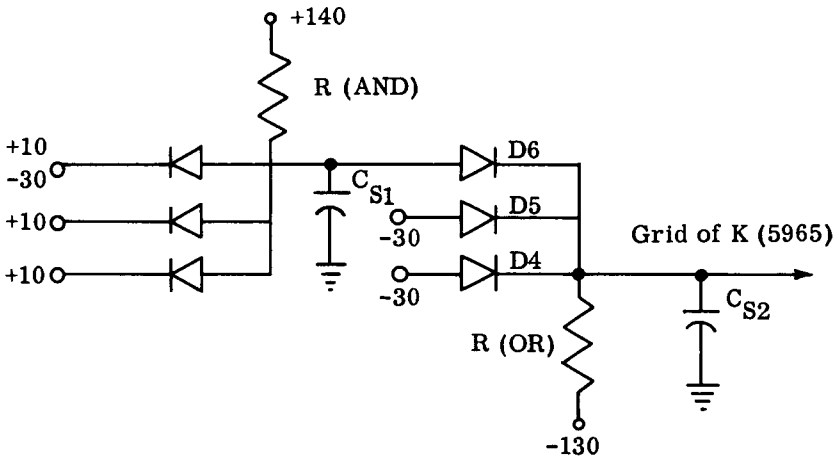
Where:

R = Effective back resistance seen by driving circuit.

C_R = Diode capacity effective during rise.

C_F = Diode capacity seen by driving circuit during fall.

1.03.06 Example--Design Three-Way AND Driving Three-Way OR



C_{S1} and C_{S2} represent wiring capacity only.

Design for 5-usec fall and less than 1.5-usec rise. Assume class F diodes for D4, D5, and D6.

1. Estimate capacity effective during fall.

K-input	6 uuf
D4 + D5	2 uuf
C_{S2}	4 uuf
	12 uuf

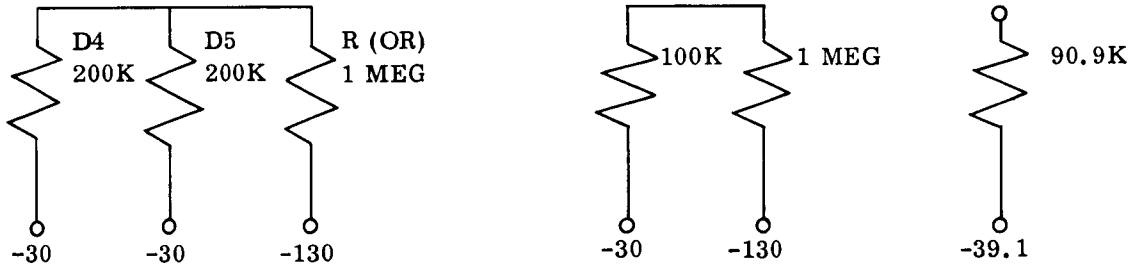
2. Compute R (OR) for 5-usec fall.

$t = 0.34\ RC$ (from section 2.02.00, Book A)

$R = \frac{5}{0.34C} = 1.23$ megohms

Use 1 MEG.

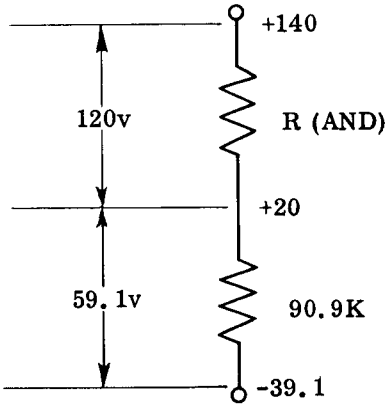
3. Compute equivalent load seen by R (AND).



$$E_{eq} = -130 + \frac{1000}{1100} \times 100 = -130 + 90.9 = -39.1v$$

$$R_{eq} = \frac{100 \times 1000}{1100} = 90.9K$$

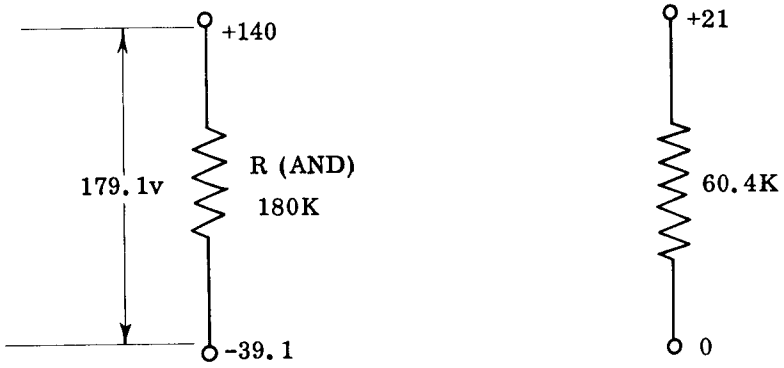
4. Compute R (AND) to give +20 volts at junction of AND circuit and OR circuit.



$$R\ (AND) = 90.9 \times \frac{120}{59.1} = 184.5K$$

Try 180K.

5. Compute equivalent voltage and resistance effective during rise.



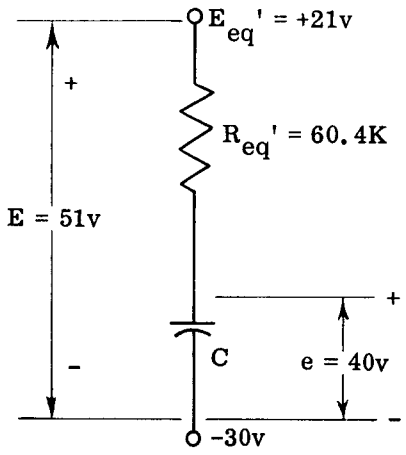
$$E_{eq} = 140 - \frac{180}{270.9} \times 179.1$$
$$= 140 - 119 = 21v$$

$$R_{eq} = \frac{180 \times 90.9}{270.9} = 60.4K$$

6. Estimate capacity effective during rise.

CF input capacity	6 uuf
D2, D3, D4, D5	4 uuf
C_{S1}	4 uuf
C_{S2}	4 uuf
	18 uuf

7. Check rise time with R (AND) = 180K. (See section 2.03.02, Book A.)



a. $40/(E_{eq}' + 30) - 40/51 = 0.785$
b. t/T from universal curve = 1.55
c. $R_{eq}' C = 0.0604 \times 18 = 1.088$
d. Rise time $t = RC \times t/T = 1.088 \times 1.55 = 1.69$ usec

180K is too large.

8. Repeat steps 5 and 7 using smaller value for R (AND).

Try 150K.

$$E_{eq}'' = 140 - \frac{150}{240.9} \times 179.1 = 140 - 111.5 = 28.5$$

$$R_{eq}'' = \frac{150 \times 90.9}{240.9} = 56.5K$$

$40/(E_{eq}'' + 30) = 40/58.5 = 0.684$
$t/T = 1.15$
$R_{eq}'' C = 0.0565 \times 18 = 1.018$
$t\ (RISE) = R_{eq}'' C \times t/T = 1.018 \times 1.15 = 1.17$ usec

150K is small enough.

Summary:

R (AND)	=	150K
R (OR)	=	1 MEG
t (RISE)	=	1.2 usec
t (FALL)	=	5.0 usec

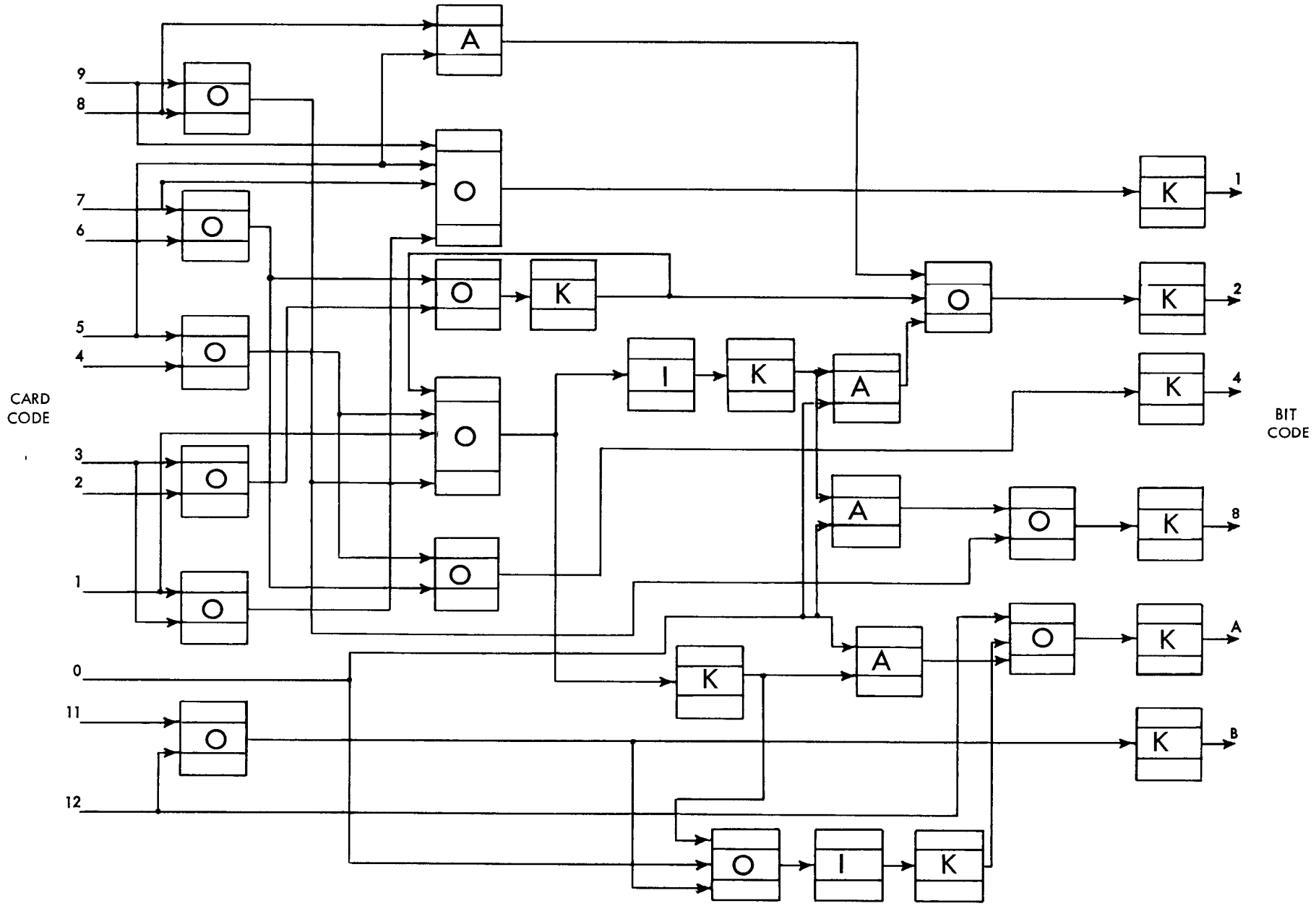


FIGURE E12. 12-to-6 TRANSLATOR

1.04.00 SAMPLE LOGIC CIRCUITS

In order to see how individual logic blocks are tied together to form a useful circuit, several sample circuits are included here. Each of the following sections refers to a specific figure and contains the description for that circuit.

1.04.01 AND/OR Circuit--12-to-6 Translator

The combination of AND/OR circuits and associated cathode followers is the actual circuit used to translate the IBM card code (alphabetical and numerical) into the 702-5 bit code (Figure E12). Allowing for normal circuit delays, the bit configuration lines are up (at +10 volts) as soon as the input lines are up. This allows for immediate decoding. The input lines represent the outputs from a trigger register. The register stores the card information (one column at a time) for as long a time as is necessary to decode and use the information.

Using the rules for AND/OR circuit operation, any input line or combination of lines can be followed through the logic blocks to bring up the proper bit-code lines. Thus a 5 (card code) brings up the 4- and 1-bit code lines and a 0 (zero) brings up the 8- and 2-bit lines. All legitimate character combinations are provided for in this circuit.

1.04.02 Minus AND Circuits for Negative Logic

Minus AND circuits are used exclusively to decode negative logic (Figure E13). This circuit is a portion of the 705-operation decoder in CPU. In this case, the minus AND circuits are used to see that all but the proper bit lines are down. The upper -AND circuit has a minus output if all the inputs are down. They would be down whenever the digit 2 is in the register (as indicated by -0010 or no 8, no 4, a 2 and no 1). The lower -AND circuit has a minus output if there are no zone bits in the register. The presence of both down-levels is checked by the third -AND circuit and, if inputs are down, the output is down. The down level output is inverted to bring up "select."

1.04.03 Binary Input Triggers

The triggers are tied together to form a binary counter. All triggers are initally reset off (Figure E14). As any one trigger is turned off (other than reset), the resultant negative shift from the right-hand output changes the status of the adjacent trigger. Because of the negative shift operation, each trigger accepts two input pulses before it impulses the next trigger. The sequence chart shows graphically the relationships existing between each trigger and the input. Note that the status of T_2 is changed when T_1 output falls and that the status of T_3 is changed when T_2 output falls. Thus, the final output would rise 16 usec after T_0 and fall 16 usec later. With this type of circuit, a one-megacycle pulse could be slowed down to any binary condition unit of time.

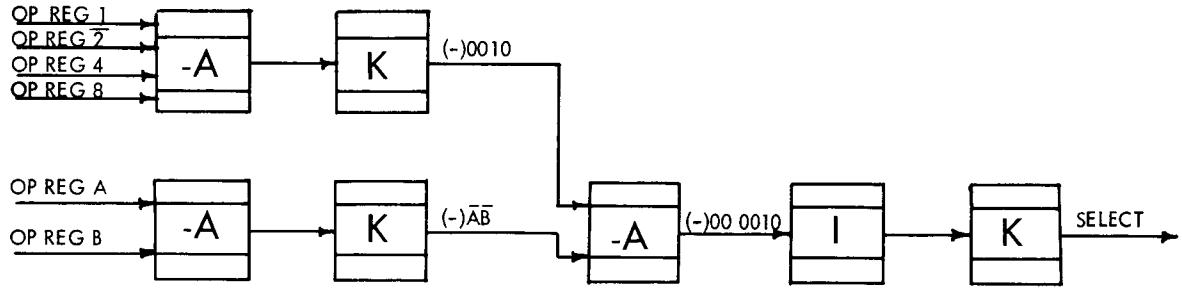


FIGURE E13. MINUS AND CIRCUITS FOR NEGATIVE LOGIC

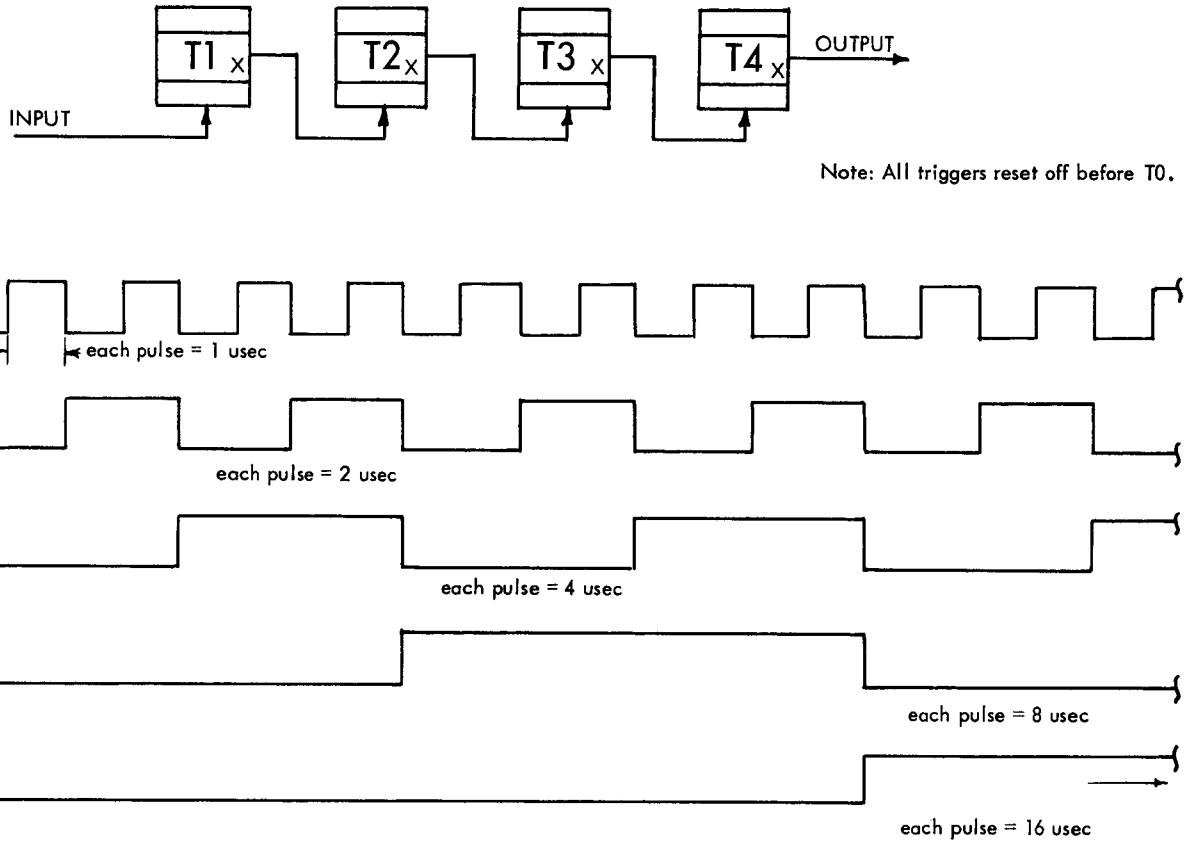


FIGURE E14. BINARY INPUT TRIGGERS AND ELECTRONIC SEQUENCE CHART

1.04.04 Sample Circuit and Sequence Chart

An electronic sequence chart is an important tool where the sequence of operation of a logic circuit needs to be illustrated graphically (Figure E15). The circuit used in this case does not exist in the machine. However, the circuit does show how individual component circuits are dependent upon the status of other component circuits. It also shows that, once the input pulses start, there is a definite time relationship between each circuit and the input.

The input consists of one-microsecond pulses. Each negative shift changes the status of T1. (See note in Figure E15 for initial trigger status.) The conditions necessary for the AND output to rise are T1-on and T2-off (T2-off down-level inverted to up-level). Note that when T1 is turning off, it provides the negative shift that turns T2 off. The AND output comes up when T1 turns on and falls when T1 turns off (circuit delay and distortion are not shown on the chart). The falling of the AND output turns T3 off. The resultant negative shift from T3 impulses the SS and its output rises. The I_{PF} is not impulsed until the SS times out (10 usec later). During the SS timing-out, the AND output comes up and falls but has no effect on T3. (T3 is off at this time.) When the SS times out, the I_{PF}, is impulsed and produces a two-usec pulse. The two-usec pulse, fed to the K_R, produces the reset pulse necessary to reset T2 and T3. The reset for T1 is independent of this circuit. The sequence then repeats itself.

Sequence charts of this general type are used extensively in instruction material to show sequence of operations. The customer engineer should familiarize himself with the mechanics of a chart of this general type and use it whenever the time sequence of a particular circuit is not readily understood.

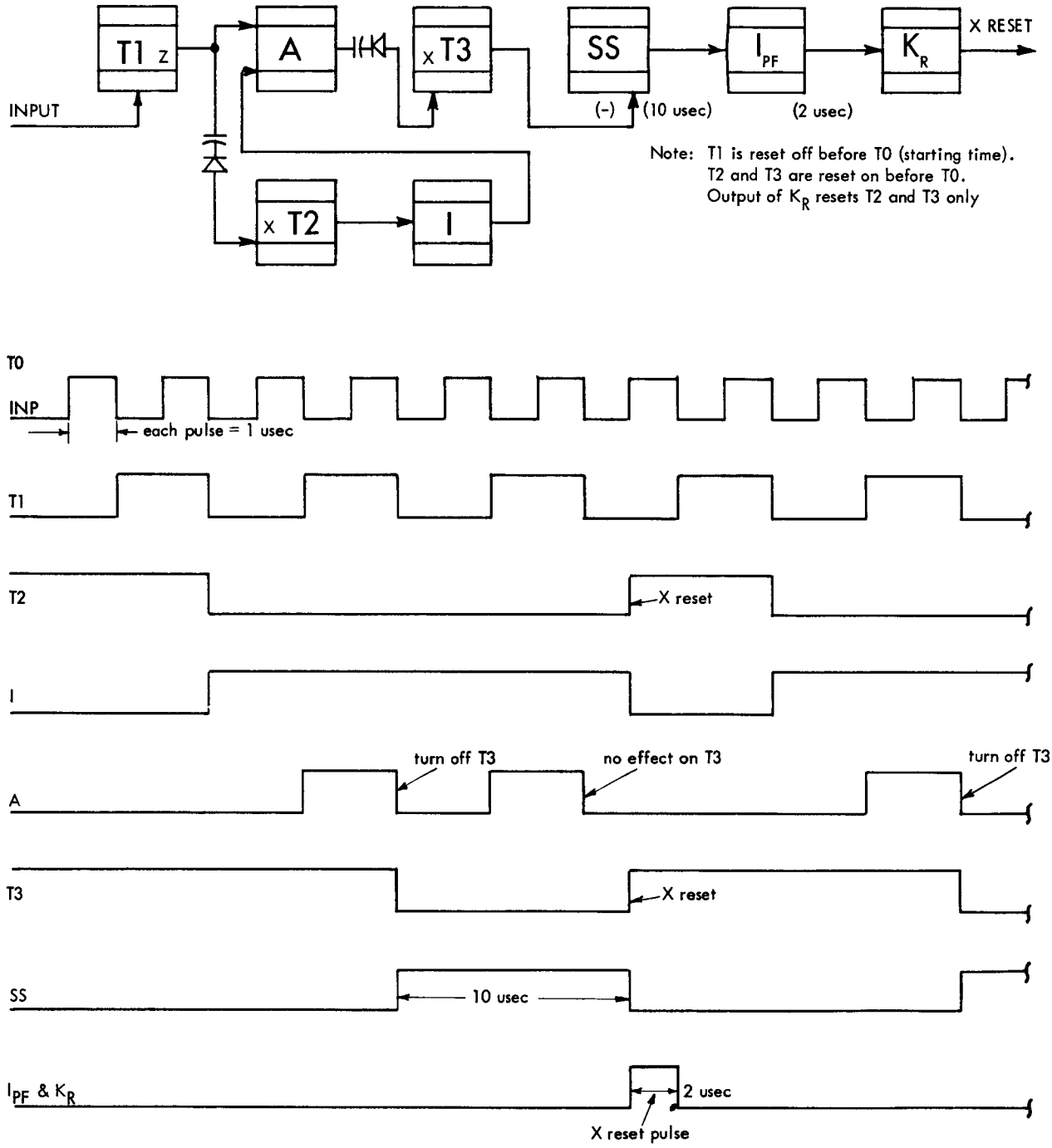


FIGURE E15. SAMPLE LOGIC CIRCUIT AND ELECTRONIC SEQUENCE CHART

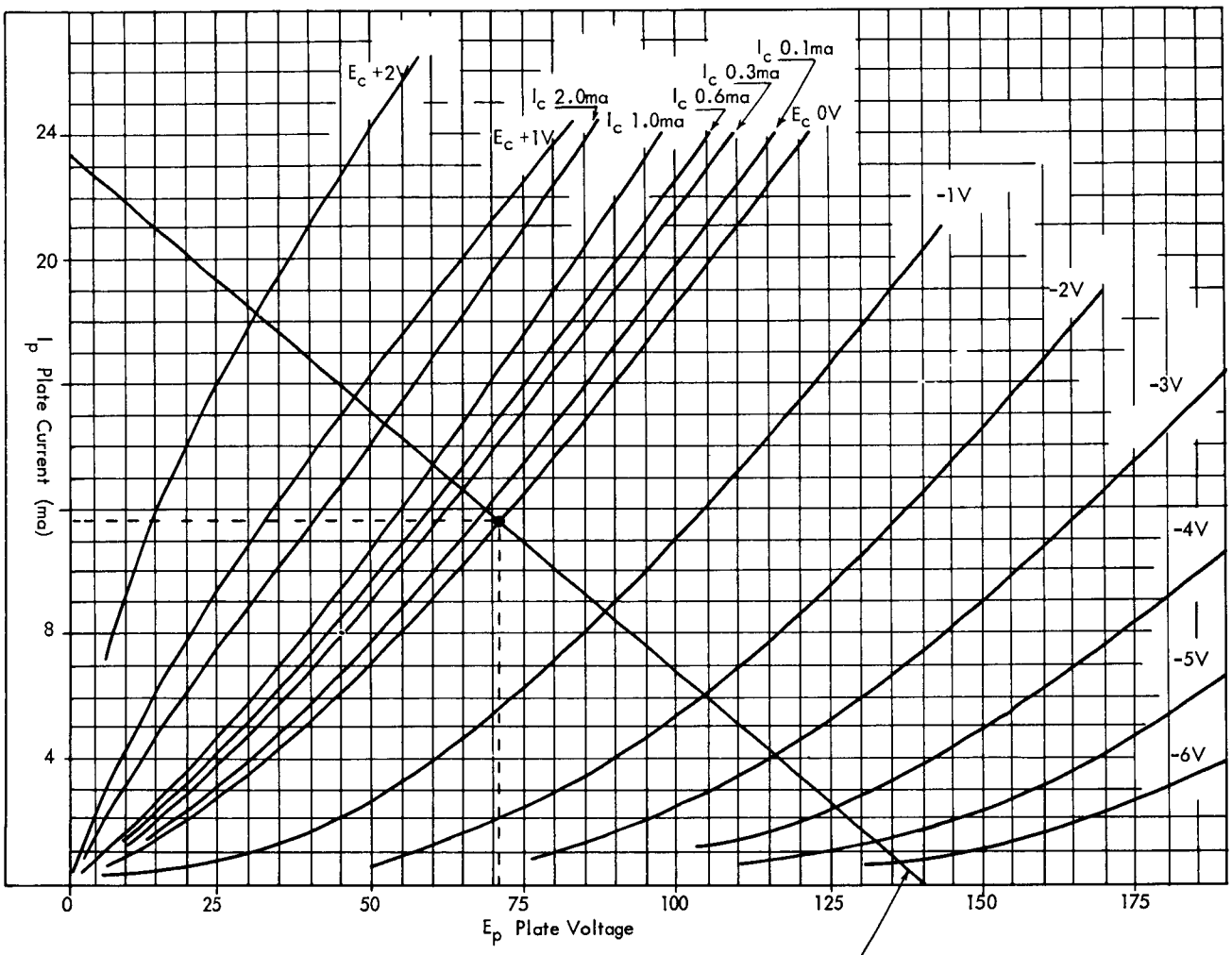
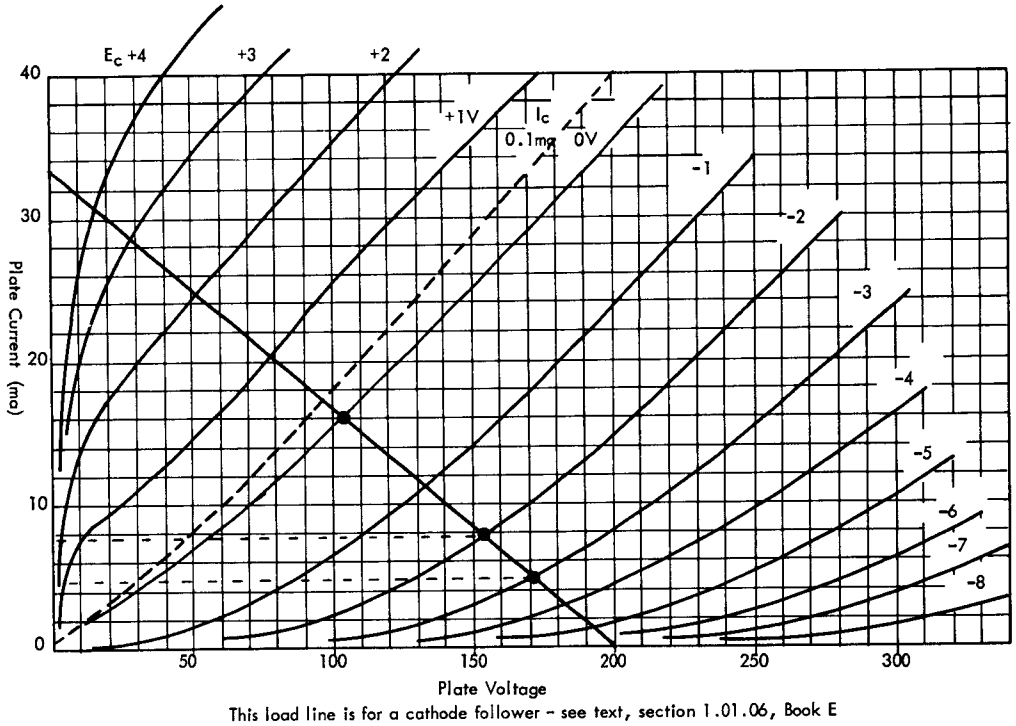


FIGURE E16. CHARACTERISTIC CURVES -- 6211



This load line is for a cathode follower - see text, section 1.01.06, Book E

FIGURE E17. CHARACTERISTIC CURVES -- 5965

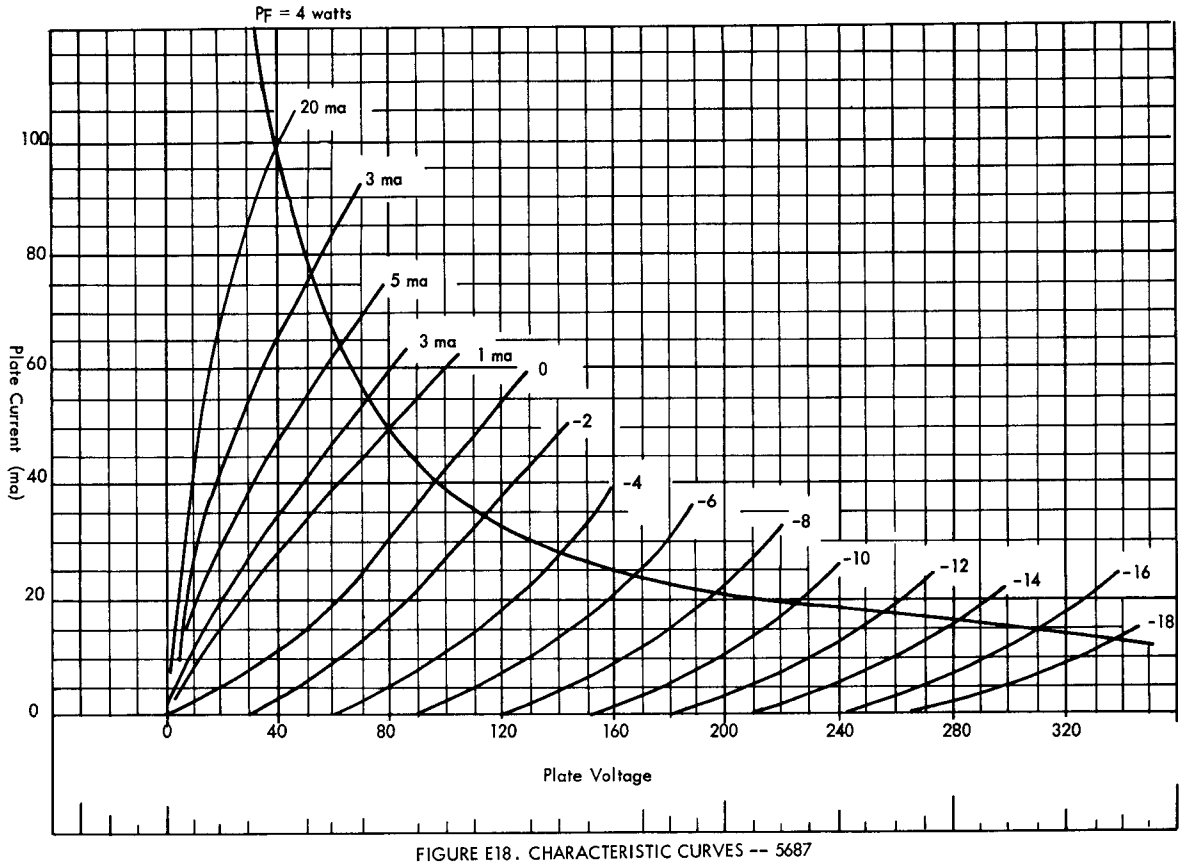


FIGURE E18. CHARACTERISTIC CURVES -- 5687

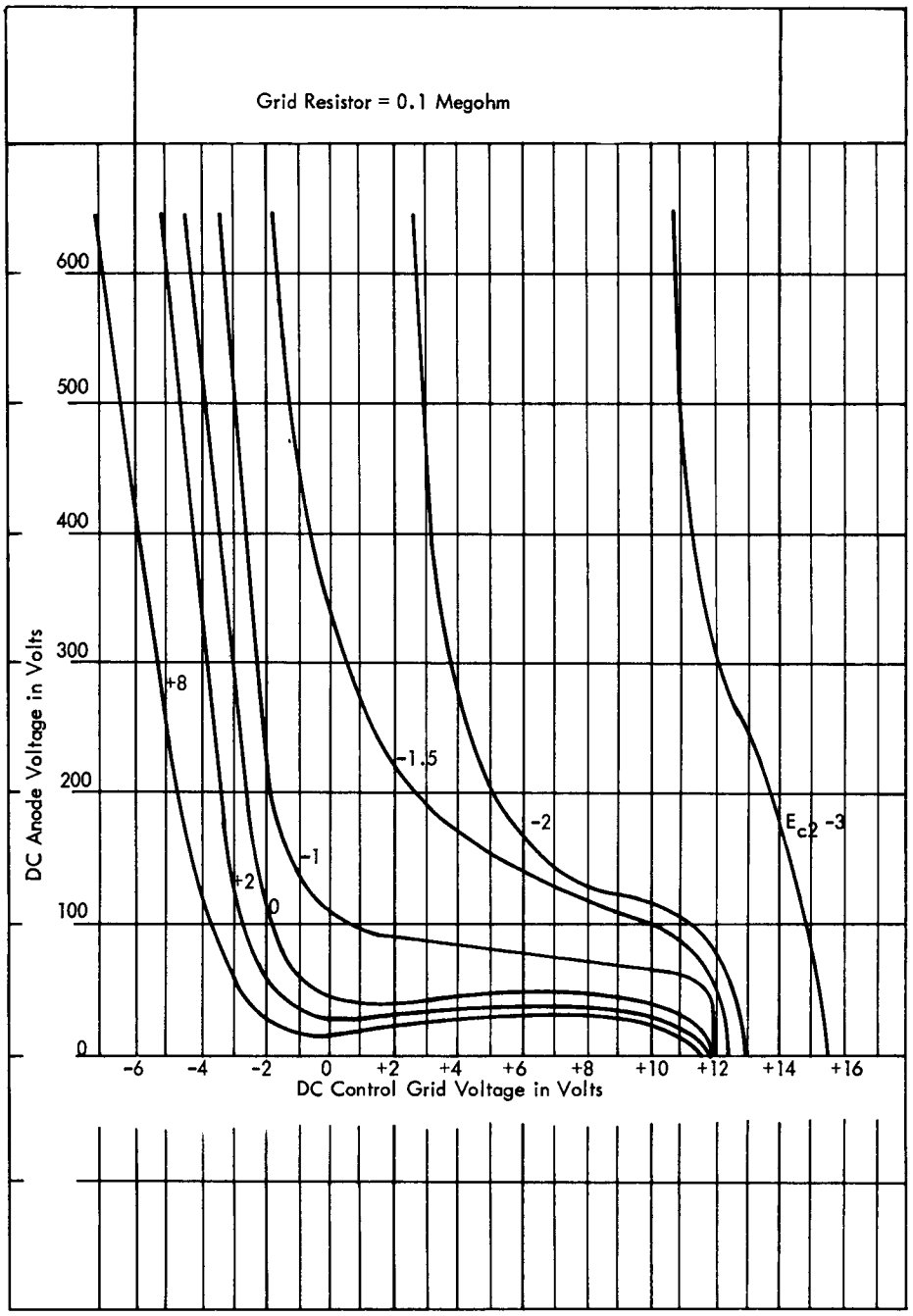


FIGURE E19. AVERAGE CONTROL CHARACTERISTICS --2D21